

P1149.6 Physical and Logical Layers

Discussion fodder : 12/17/01

Overview

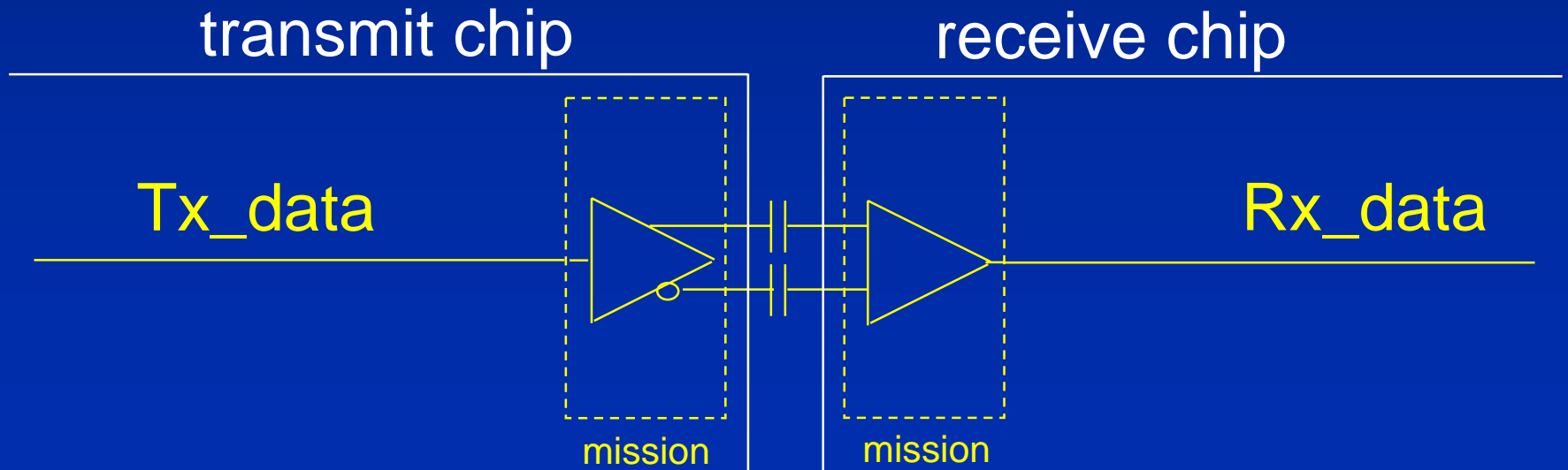
- Introduction to structure: “modes” and “layers”
- P1149.6 Physical Layer: Signaling options
 - Differential vs. Dual single-ended
- P1149.6 Logical Layer: Protocol options
 - Timing
 - Frequency
 - Edge
- Comparisons

Vocabulary and Structural Layers

- “Modes”
 - Mission mode (normal operation)
 - Boundary Scan Modes
 - DC Extest mode
 - AC Extest mode
- “Layers” (interface circuits)
 - Mission
 - Physical layer
 - Logical layer (== signaling == protocol)
 - Scan layer

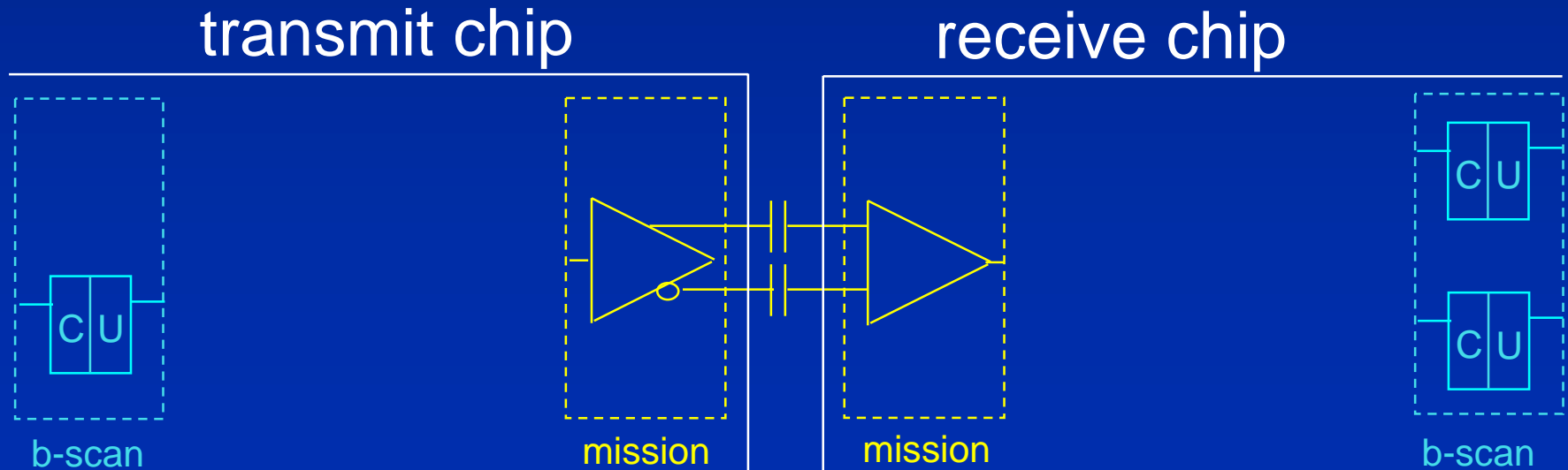
Mission Mode

- Single Tx wire becomes differential data
- AC- or DC-coupled differential interconnect
- Differential receiver produces single Rx wire



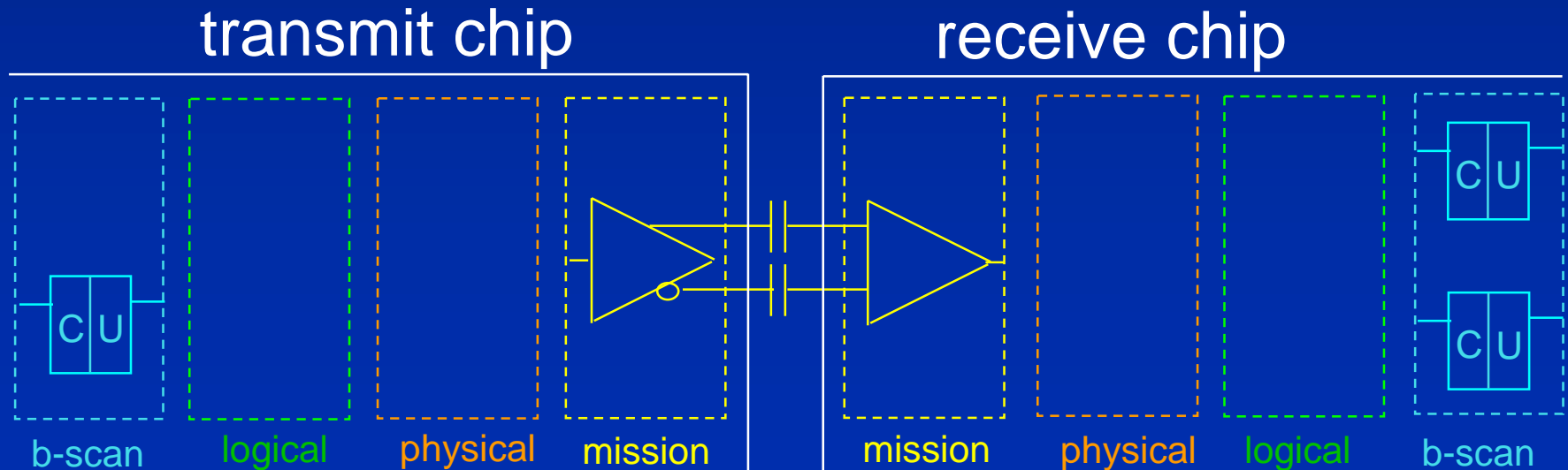
Boundary Scan Test Modes

- Data in transmit chip's Boundary Scan Register(s) must be mapped into (mission) channel data
- Channel data (mission) must be mapped into receive chip's Boundary Scan Register(s)



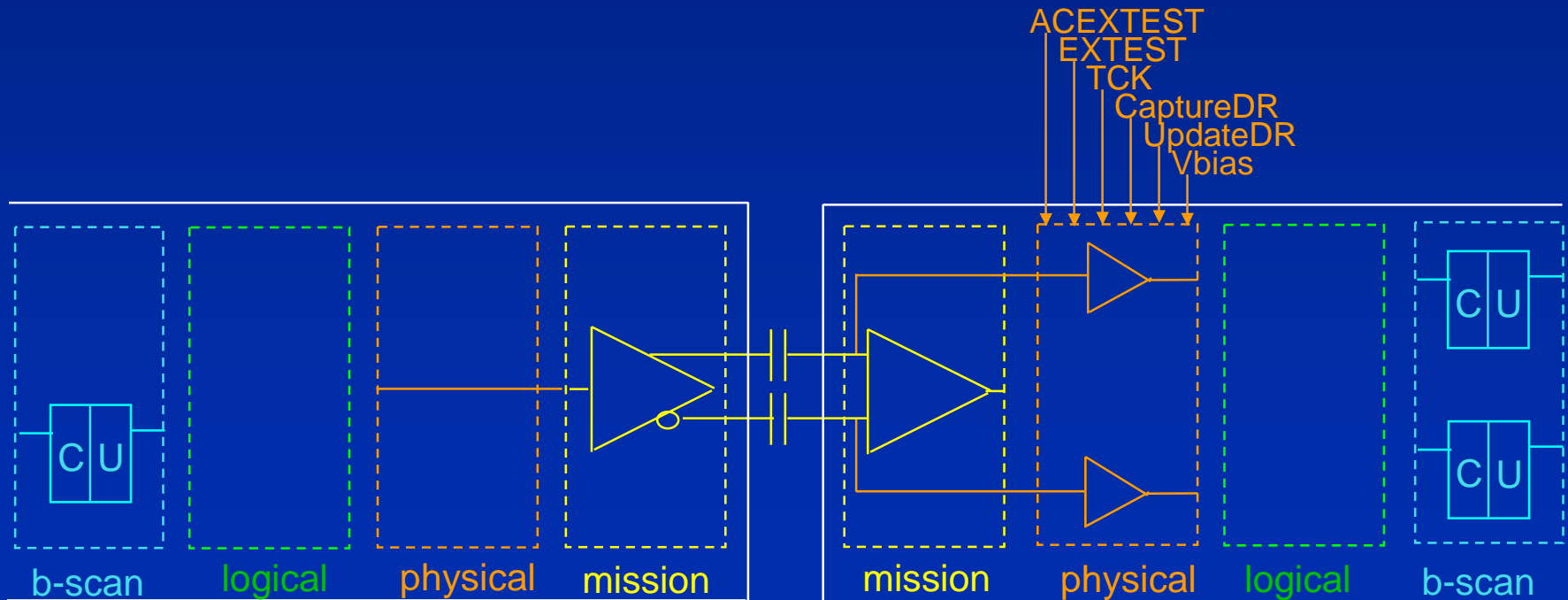
Schematic View of Layers (Interfaces)

- Mission: functional circuitry
- Physical: mission signals \Leftrightarrow test logic
- Logical: (implements protocol) : physical \Leftrightarrow scan
- Boundary scan : (1149.1) : test stim and response



P1149.6 Physical Layer : Example*

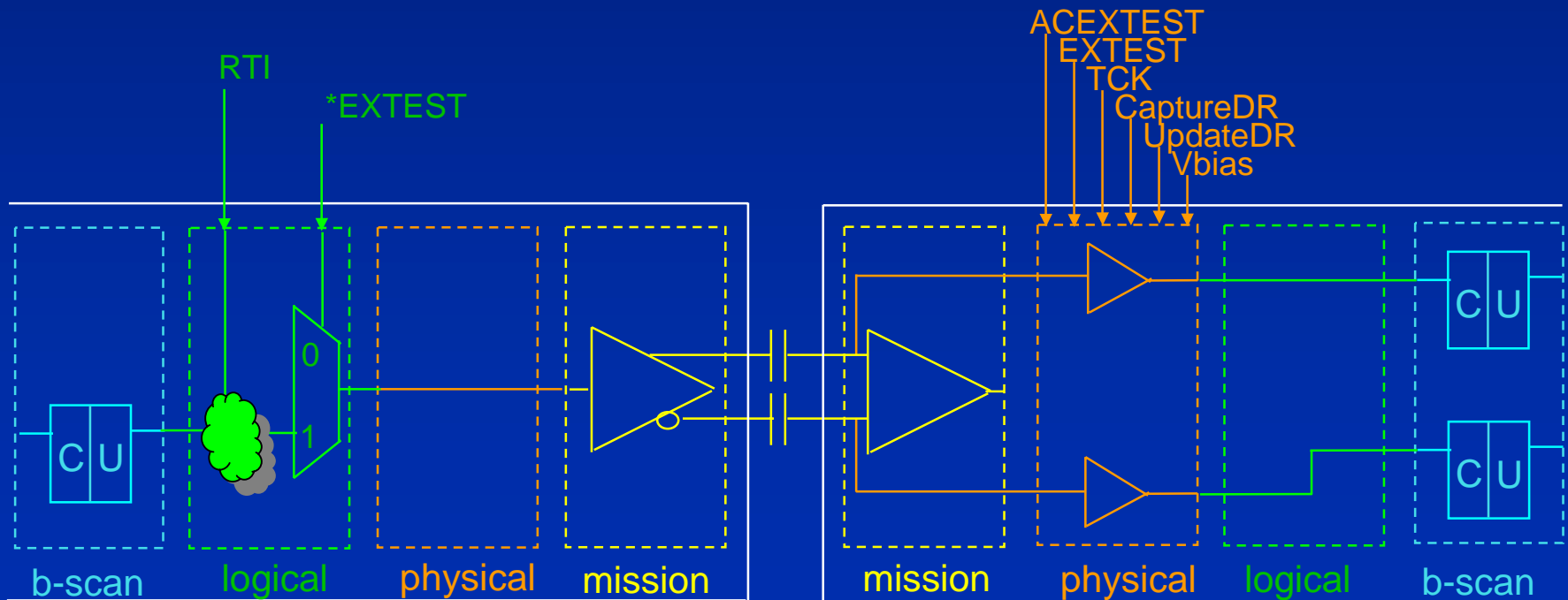
- Test Driver
 - Differential drive: use mission driver
- Test Receiver
 - Self-referencing hysteretic receiver



P1149.6 Logical Layer : Example*

*Throat-clearing driver;
Dual-Edge-based receiver

- Test Driver
 - Differential drive: use mission driver
- Test Receiver
 - Self-referencing hysteretic receiver

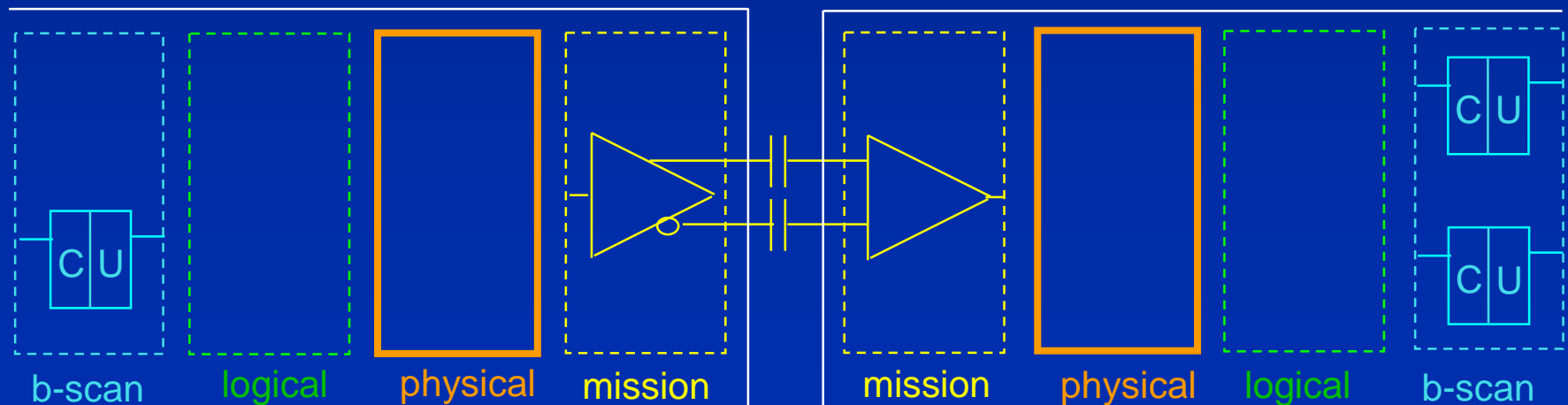


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Physical Signaling Options (6 total)

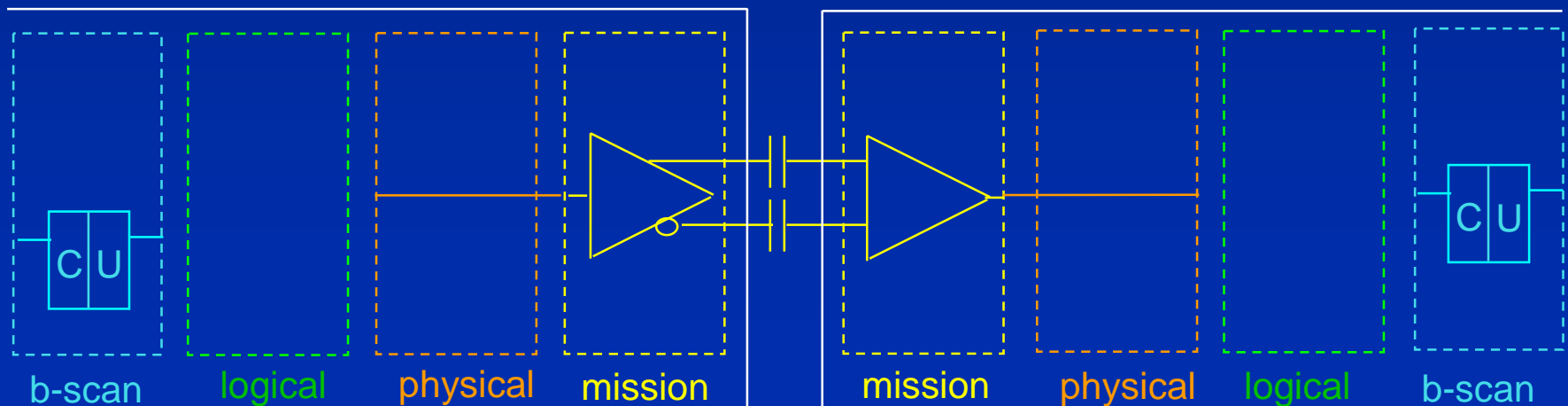
- Four options for signaling:
 - Differential drive, differential receive
 - Differential drive, dual single-ended receive
 - Dual single-ended drive, differential receive
 - Dual single-ended drive, dual single-ended receive
- Two types of differential receive
 - Mission
 - TestD



1: Diff Dr, Diff Rx (Mission Rx)

- + No driver modification
- + No additional driver noise
- Loss of diagnosability
- 1149.1 compliance issue

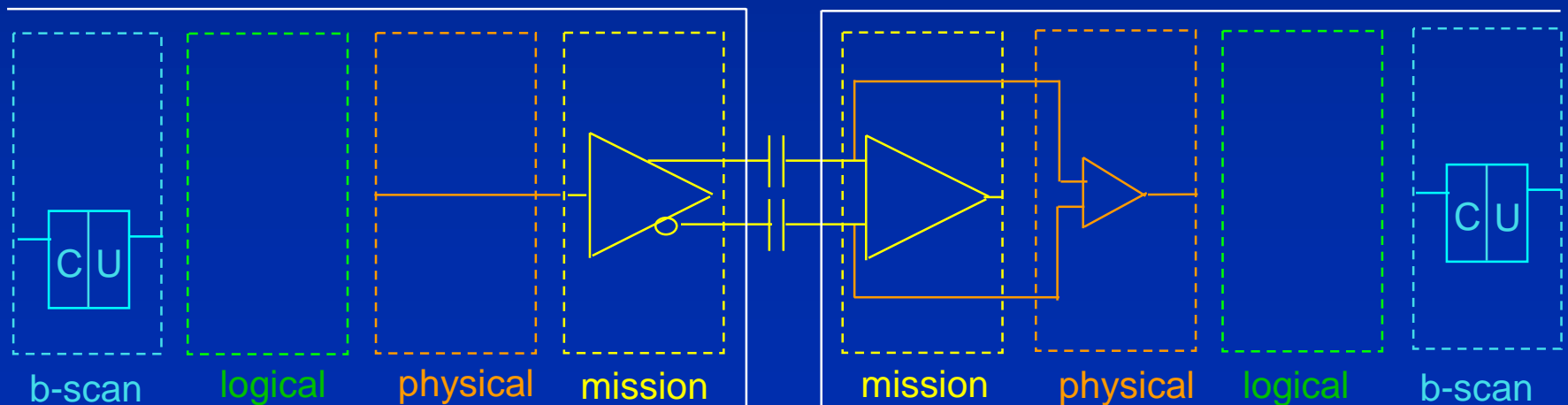
- + Leverage mission receiver
- Low diagnosability
- 1149.1 compliance issue



2: Diff Dr, Diff Rx, TestD Rx

- + No driver modification
- + No additional driver noise
- Loss of diagnosability
- 1149.1 compliance issue

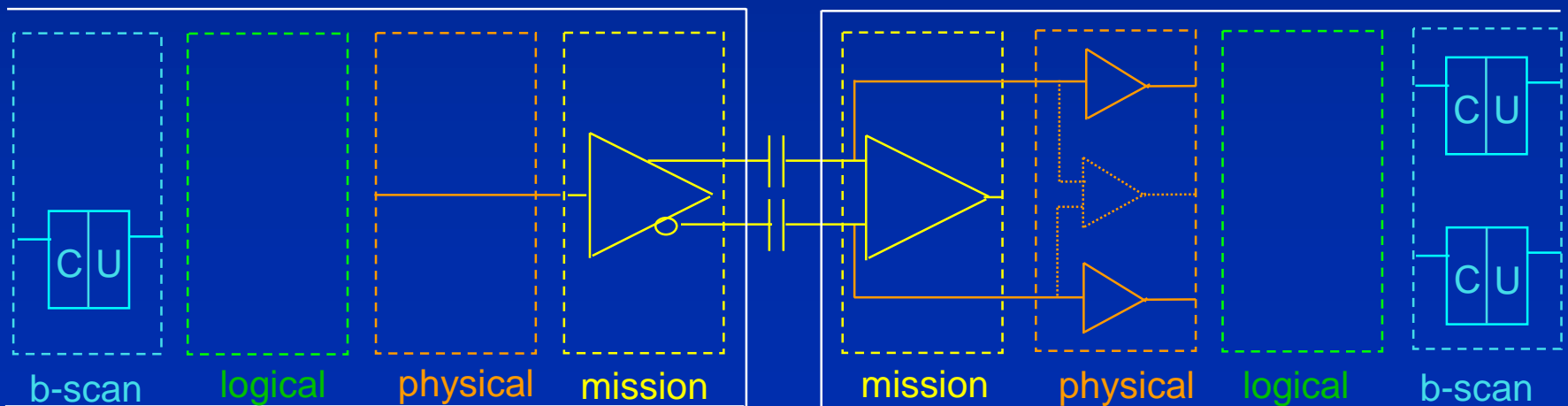
- Extra differential receiver
- Low diagnosability
- 1149.1 compliance issue



3: Diff Dr, Dual SE Rx

- + No driver modification
- + No additional driver noise
- Loss of diagnosability
- 1149.1 compliance issue

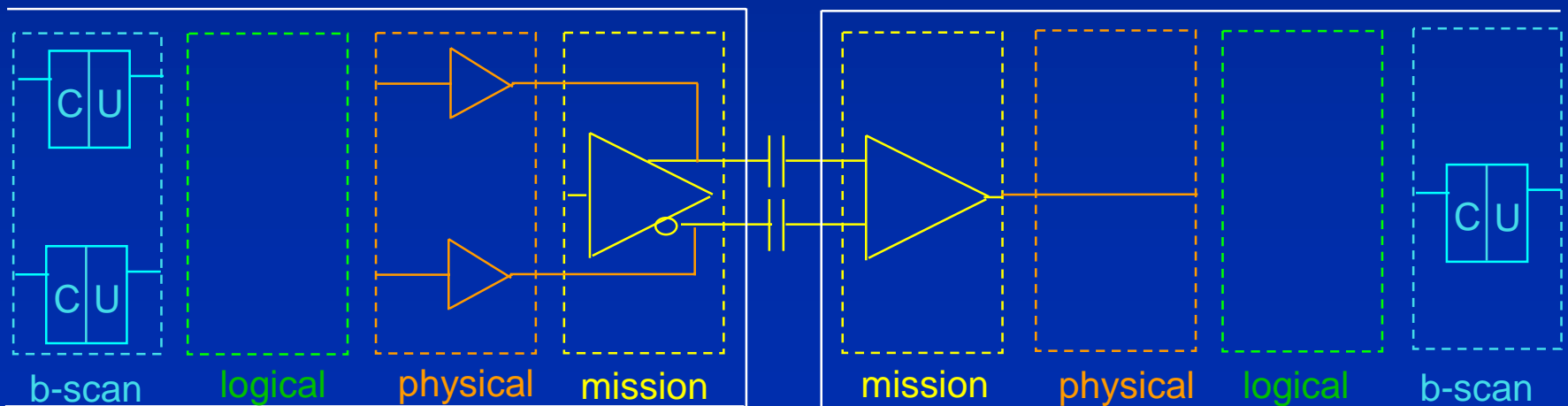
- Additional receiver circuits
- + Good diagnosability
- + 1149.1 compliant



4: Dual SE Dr, Diff Rx (Mission Rx)

- Driver modification required
- Driver noise likely
- + Good diagnosability
- + 1149.1 compliant

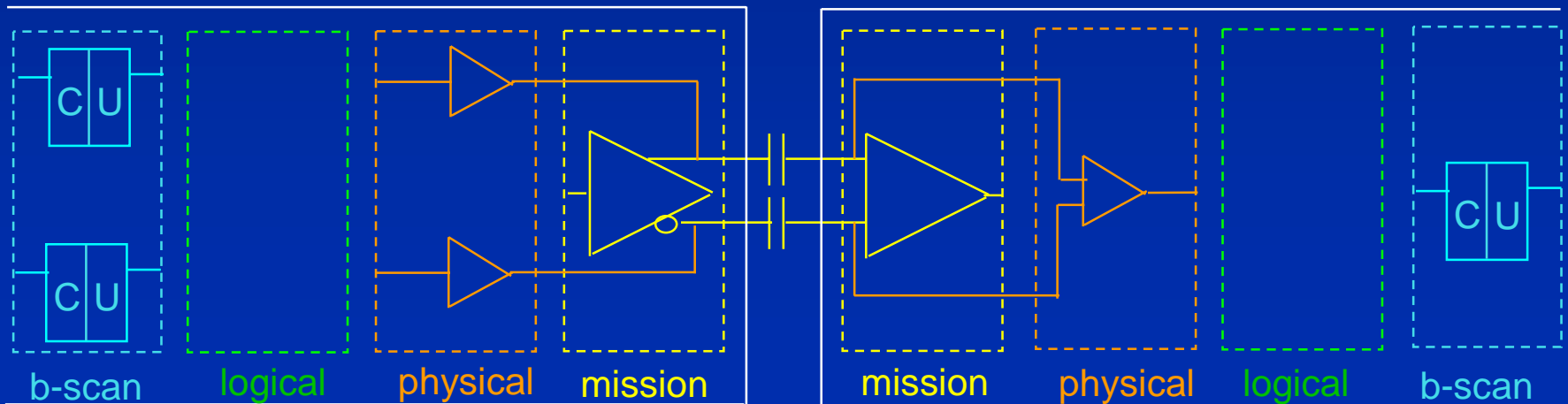
- + Leverage mission receiver
- Low diagnosability
- 1149.1 compliance issue



5: Dual SE Dr, Diff Rx (TestD Rx)

- Driver modification required
- Driver noise likely
- + Good diagnosability
- + 1149.1 compliant

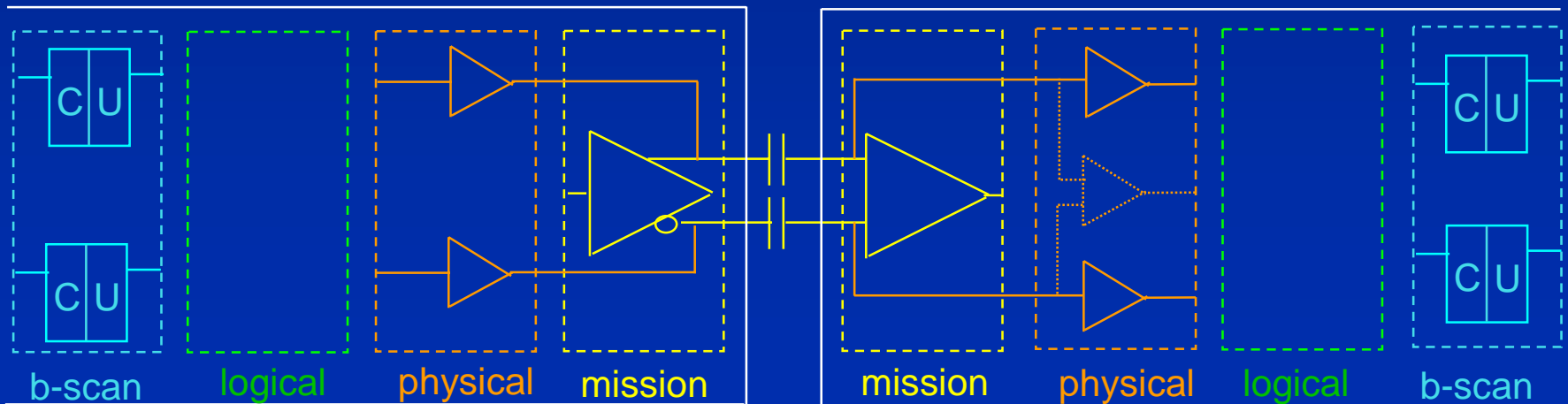
- Extra differential receiver
- Low diagnosability
- 1149.1 compliance issue



6: Dual SE Dr, Dual SE Rx

- Driver modification required
- Driver noise likely
- + Good diagnosability
- + 1149.1 compliant

- Additional receiver circuits
- + Good diagnosability
- + 1149.1 compliant



P1149.6 Physical Layer: Comparison

Signaling Technique

Full differential	<ul style="list-style-type: none">+ 1149.1 compliant+ mitigates ground bounce/noise- poor fault coverage and diagnosis
Diff drive / SE receive	<ul style="list-style-type: none">- 1149.1 compliance issues+ mitigates ground bounce/noise+ good fault coverage and diagnosis
Single-ended / single-ended	<ul style="list-style-type: none">+ 1149.1 compliant- impact on driver design: scalability+ best fault coverage and diagnosis

Overview

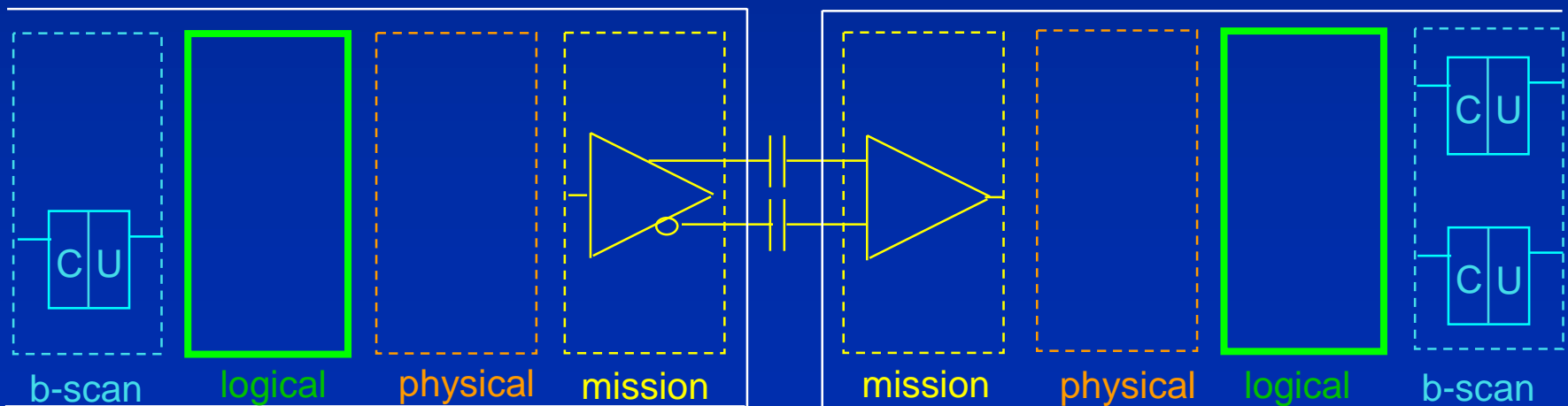
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P1149.6 Logical Layer : Purposes

- Connect physical layer to Bscan Register(s)
- Implement circuitry for EXTEST instruction
 - Must be compliant with 1149.1
- Implement circuitry for ACEXTEST instruction
 - Dependent upon protocol chosen (timing, freq, edge)
 - Also dependent upon physical layer (eg. # BSRs)

P1149.6 Logical Layer : Options

- Timing-based (== pattern-based) {MSA}
- Frequency-based {Agilent #1}
- Edge-based
 - Positive-trigger only {Philips}
 - Both edges {Agilent #2}



What's in the green box?

Insert extensive analysis of each proposal here...

AC EXTEST Technology Comparison*

*tentative

AC EXTEST Logical Layer

	Timing-based	Freq-based	Edge-based
New pins?	+ No	- Maybe ?	+ No
Test sig timing	-Skew mgmt	+Phaseless	+Phaseless
Overhead	+ Medium	- Large	+ Small
Scalability	- At risk	+ Best	+ Good
Noise	- At risk	+ Immune	- At risk

AC EXTEST Technology Comparison*

*tentative

AC EXTEST Logical Layer

	Timing-based	Freq-based	Edge-based
New pins	no	maybe	no
Si Area	medium	large	small
Power	?	?	?
Iddq testability	?	?	?
Noise immunity	physical	accumulates	physical
Max/Min TCK	f(skew)	none	none
Scalability	physical	physical	physical
Tool migration	?	?	?
1149.1 compl.	?	?	?

P1149.6 Logical Layer Issues

- Noise Immunity
 - Is any required beyond the Physical Layer?
- Coverage
 - Is there a need for TestD?
- Implementation
 - Scalability to higher frequencies, on-chip Cs
 - Area and extra pins requirements
 - Ease of use via TAP
 - Test time