

A Comparison of AC-EXTTEST Proposals

Overview

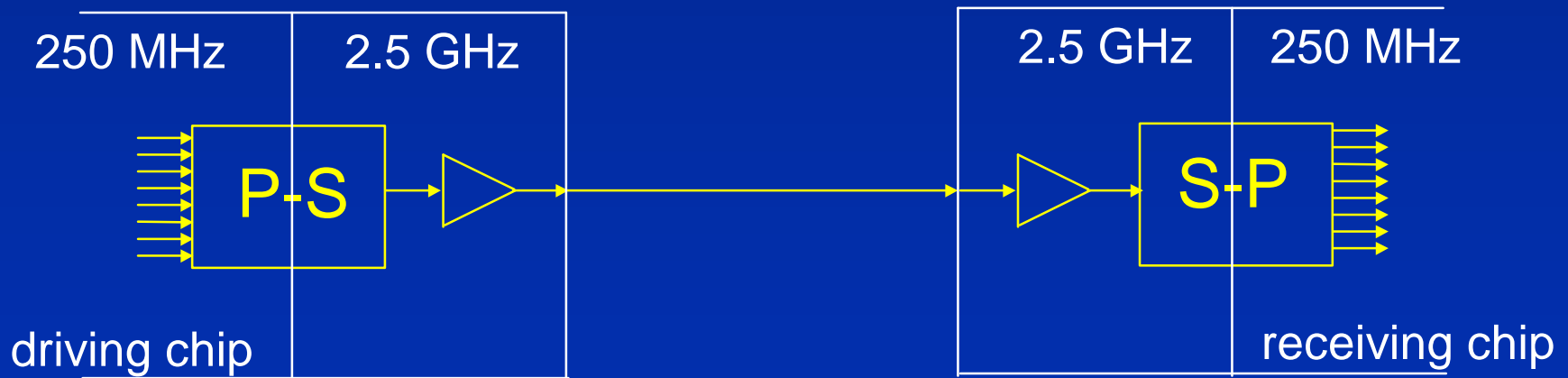
- Introduction and technical background
- Criteria for AC-EXTTEST solution
- Environments
- Defects and failures
- Taxonomy of possible solutions
- Detailed examination of alternatives
- Comparison, recommendation, and issues

Introduction

- Subject: PC board and system test
- Issue: IEEE 1149.1 boundary scan limitation
 - Intended for DC-connected nets only
- Fact: New high-speed signal pins are AC-coupled
- Problem: DC tests won't work
- Solution: Extend 1149.1 to allow AC tests
- Proposals: Several AC-EXTEST methods
- Purpose: Examine these alternatives

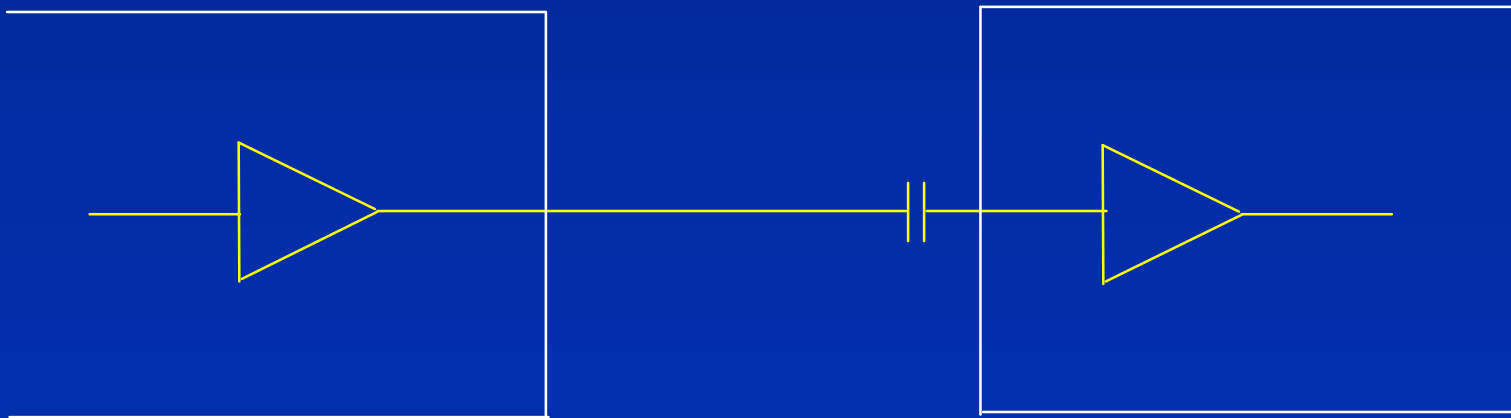
Background: SerDes Technology

- SerDes = Serializer/Deserializer
- Used for very high speed data transfer
- Parallel-to-serial and serial-to-parallel circuits
- Usually a 10:1 clock period ratio (parallel:serial)
- Clock embedded in serial coding



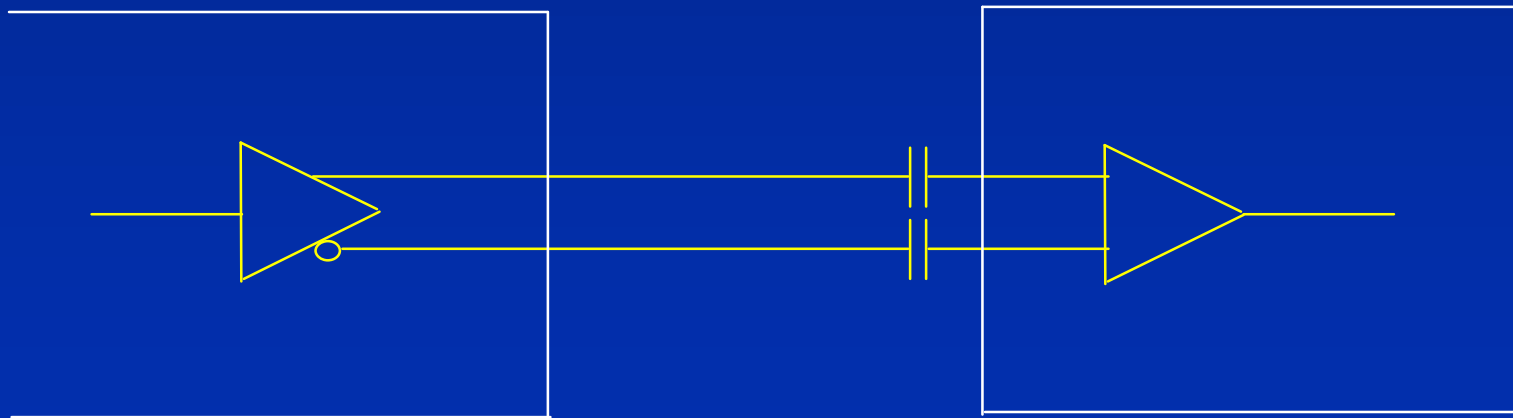
AC-Coupled Nets

- DC offsets vary between drivers and receivers
- Multiple vendor networks : different thresholds
- AC coupling (near receiver) solves this problem
- but introduces DC balancing problem: signal stream must contain distribution of 1s and 0s.



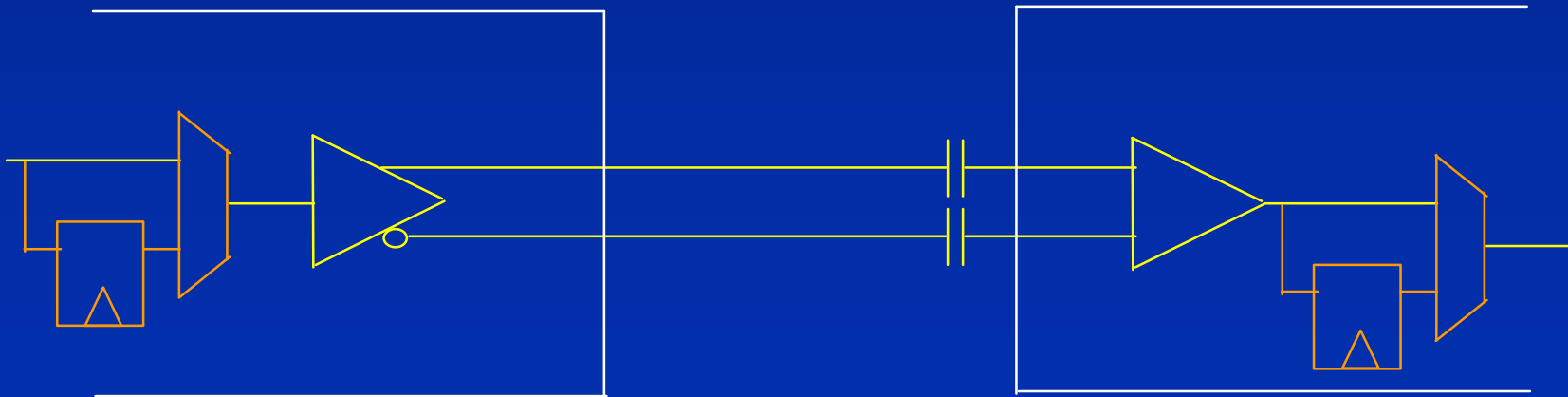
Differential Nets

- High speed circuits often differential
 - Faster logic value discrimination
 - Fewer problems with noise and coupling
- Single signal gets split into positive & negative copies



1149.1 Boundary Scan Testing Issues

- 1149.1 DC-based tests won't work through caps
- 1149.1 multiplexors in GHz domain non-trivial
- 1149.1 lacks rigor with respect to differential
- problem could be attacked with 1149.4
 - test times for myriad capacitor measurements are long
 - tools for .4 are not prevalent yet



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Criteria for AC-EXTEST Solution (1)

- Must accommodate coupling capacitors
- Must work for mixed AC/DC boards
- Must work for single-ended and differential
- Must not compromise SerDes performance
- Must detect/diagnose expected defect spectrum
- Must work in multiple environments:
 - Device-to-device
 - Device-to-tester
 - Tester-to-device

Criteria for AC-EXTEST Solution (2)

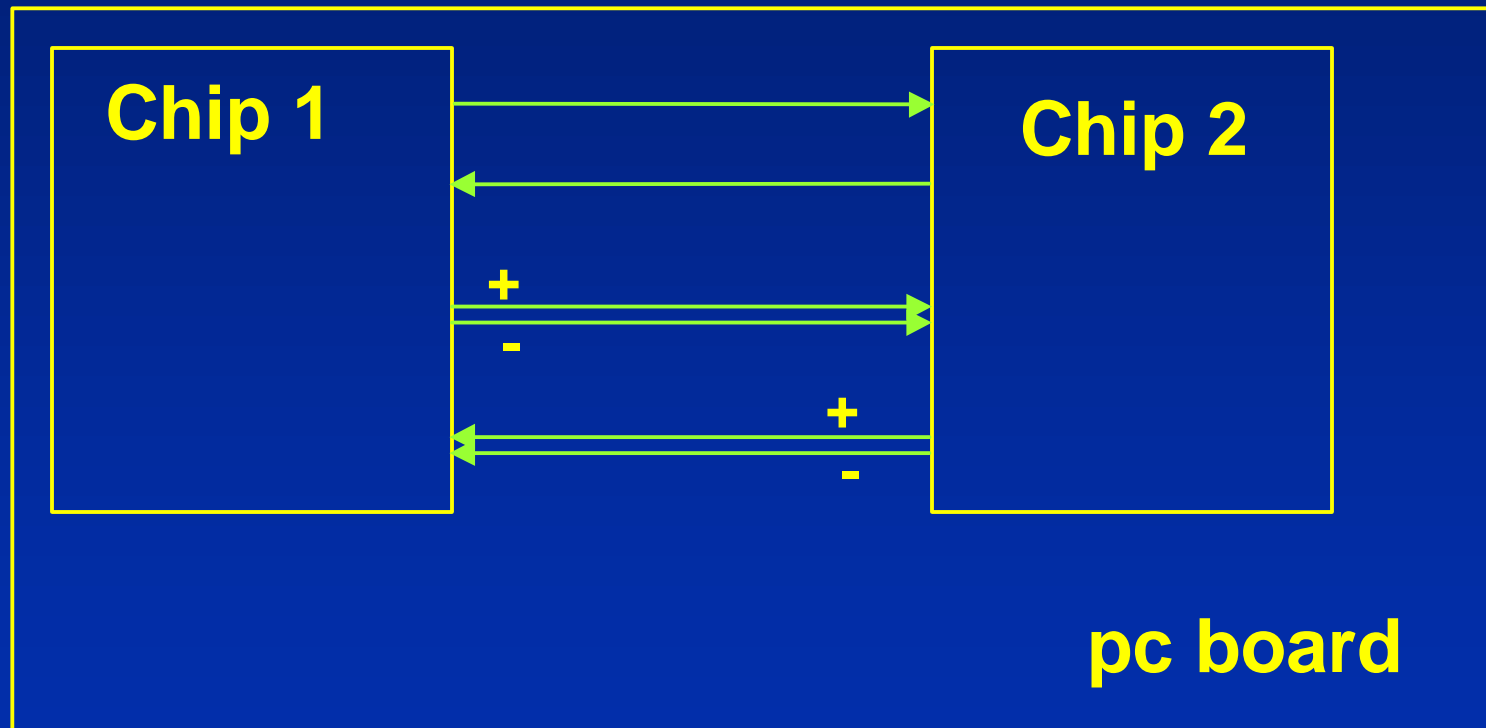
- Must work on common ATE
 - mainline board testers
 - PC-based Boundary-Scan equipment
- Must be independent of SerDes coding scheme
- Must be “1149.1-friendly” (utilize existing tools)
- Must be implementable on big-A little-D chips
- Must be scalable and interoperable:
 - IC Vendors
 - IC Processes
 - Rising Frequencies (2.5Gb, 3.125, 10, 40 ...)
 - Intra-package and On-chip capacitor integration (very small)

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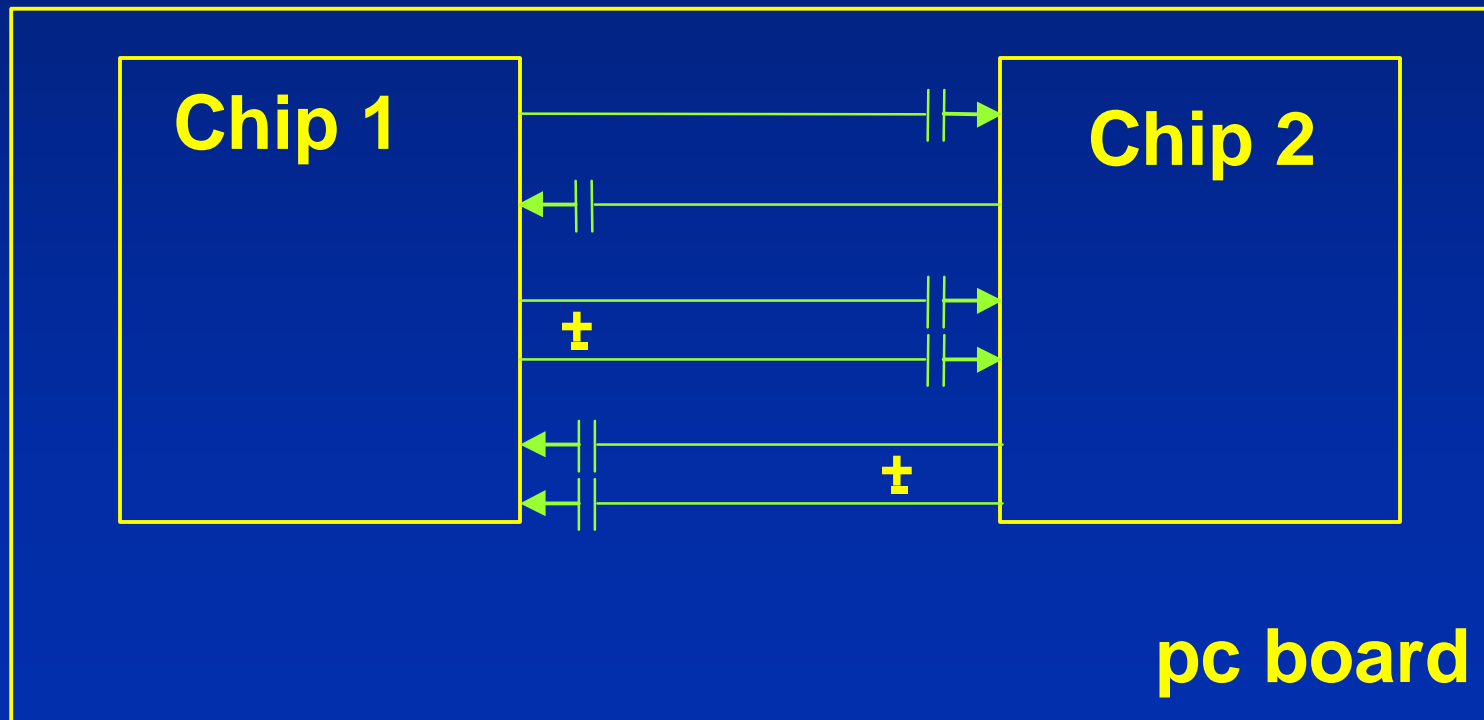
Env 1 : chip-to-chip DC interconnect

- Single-ended interconnect
- Differential interconnect



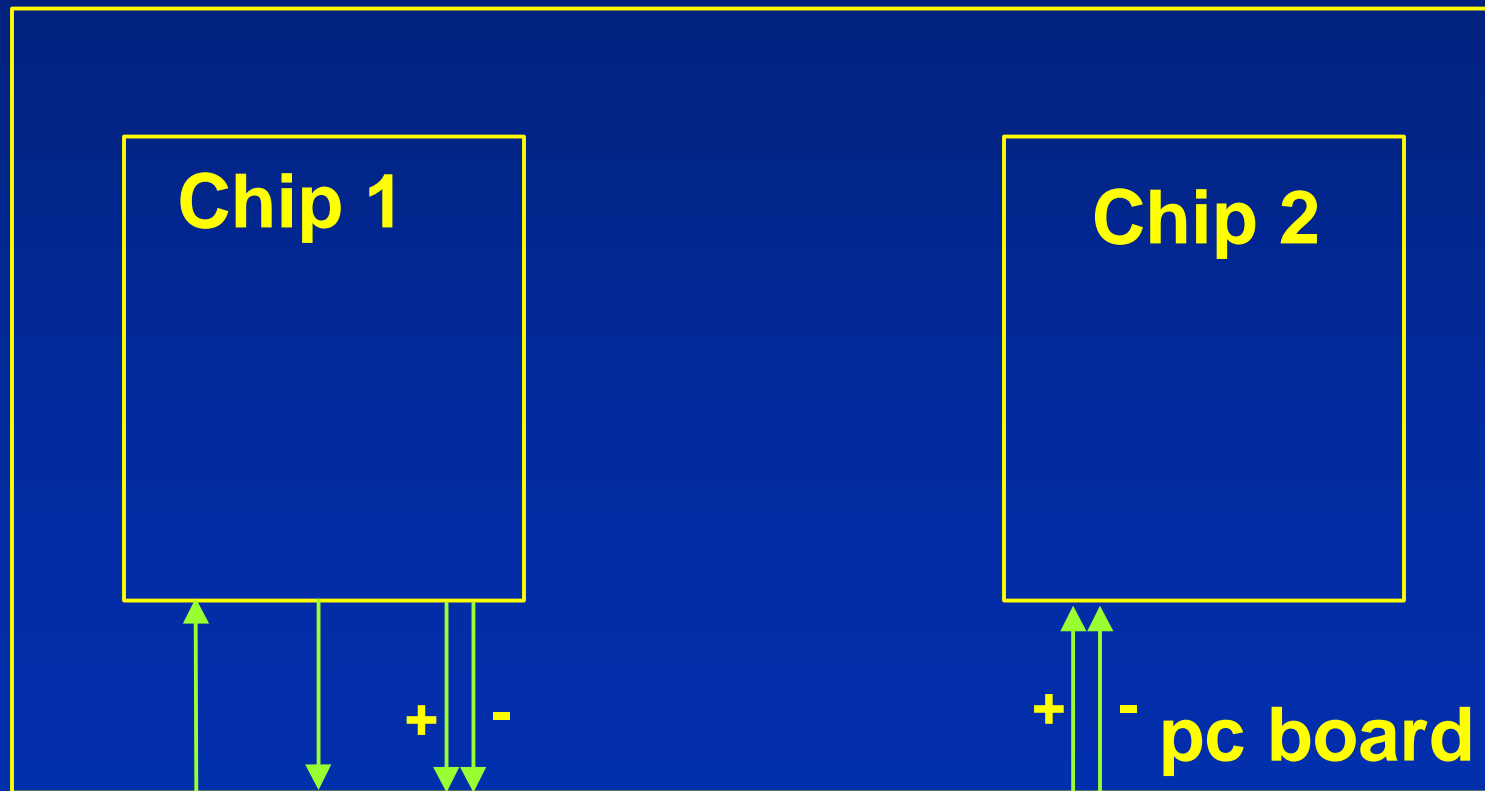
Env 2 : chip-to-chip AC interconnect

- Single-ended interconnect
- Differential interconnect
- Capacitors could be integrated in future



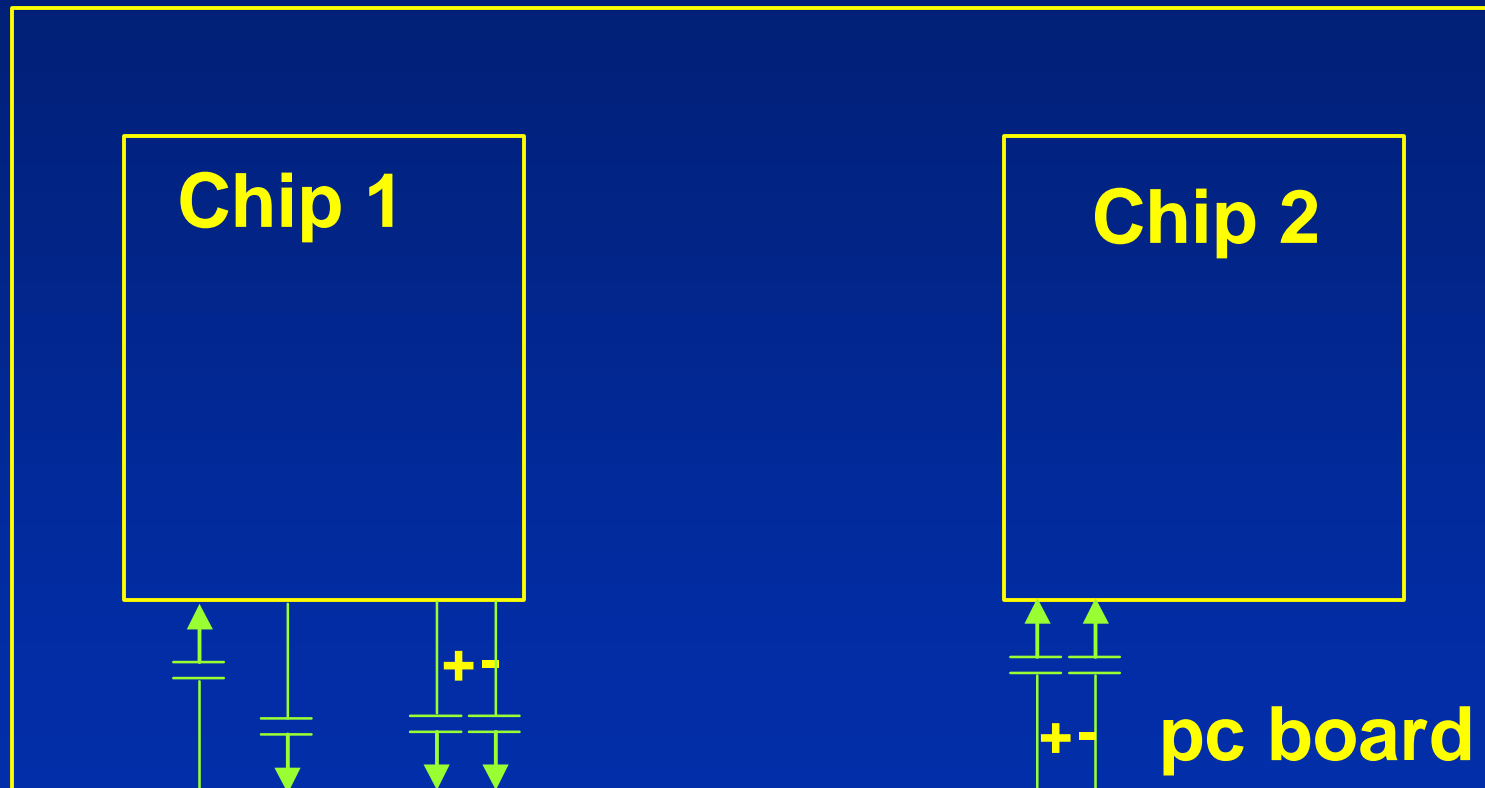
Env 3 : chip-to-edge DC connect

- Single-ended connections
- Differential connections



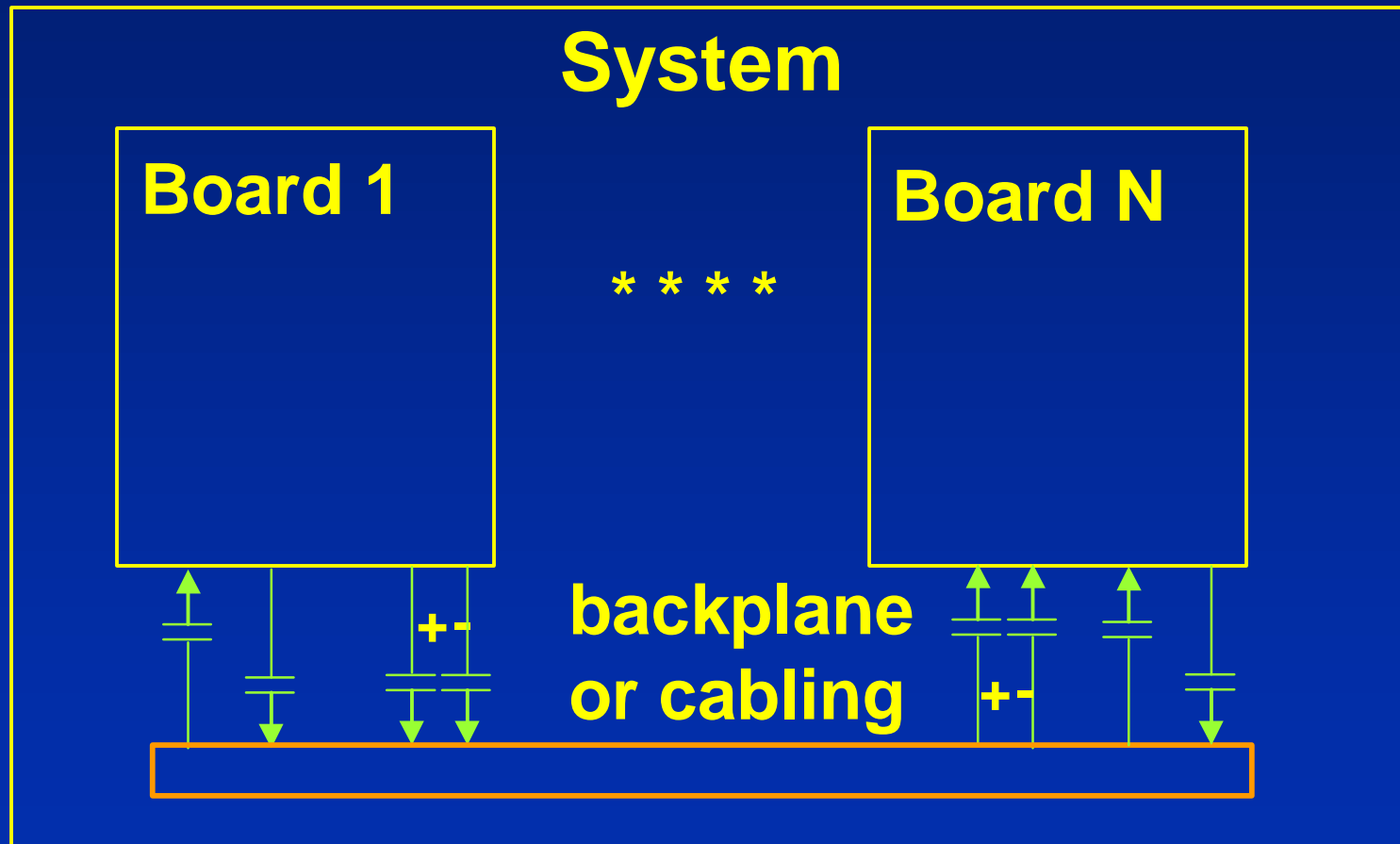
Env 4 : chip-to-edge AC connect

- Requires new tester or fixture-based capability



Env 5 : board-to-board AC connect

- System integration testing



Overview

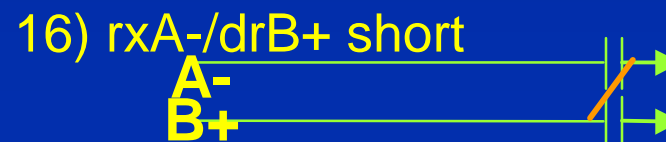
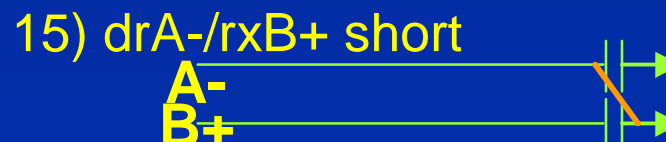
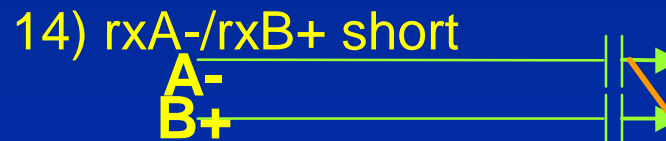
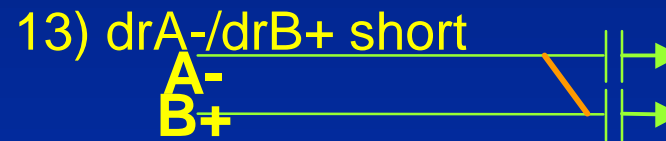
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Defects and Failures

- Defects are unwanted physical entities on improperly manufactured boards/systems
 - Extra or missing solder, missing device, cable etc.
- Failures are detected differences between good and defective circuits
 - Defects can be enumerated and prioritized
 - Failures can be correlated to defects
 - Good tests will 'cover' the most defects

Goal: Verify that defects are detected by tests

Defect Universe



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Taxonomy of AC-EXTEST Solutions

- 1149.1 Differential Signal Technique:
 - Full differential
 - Differential drive / single-ended receive
 - Single-ended / single-ended
- AC-EXTEST Technology:
 - Timing-based
 - Frequency-based
 - Edge-based

Forms a Taxonomy Matrix

AC EXTEST Technology

1149.1 Diff Technique	Timing-based	Freq-based	Edge-based
Full differential			
Diff drive / SE receive			
Single-ended / single-ended			

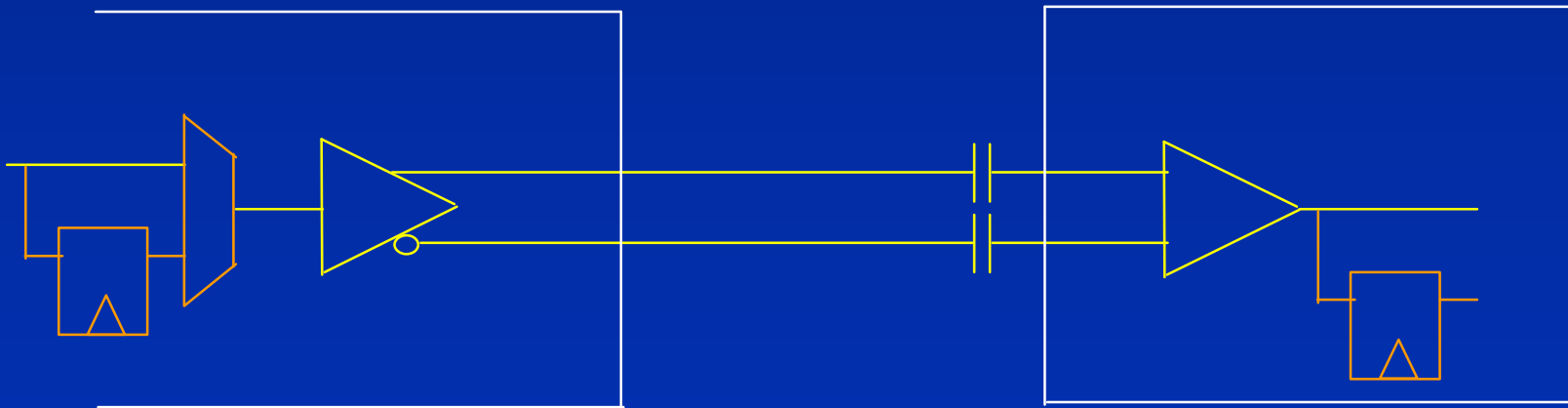
Differential Technique Comparison

1149.1 Diff Technique

Full differential	
Diff drive / SE receive	
Single-ended / single-ended	

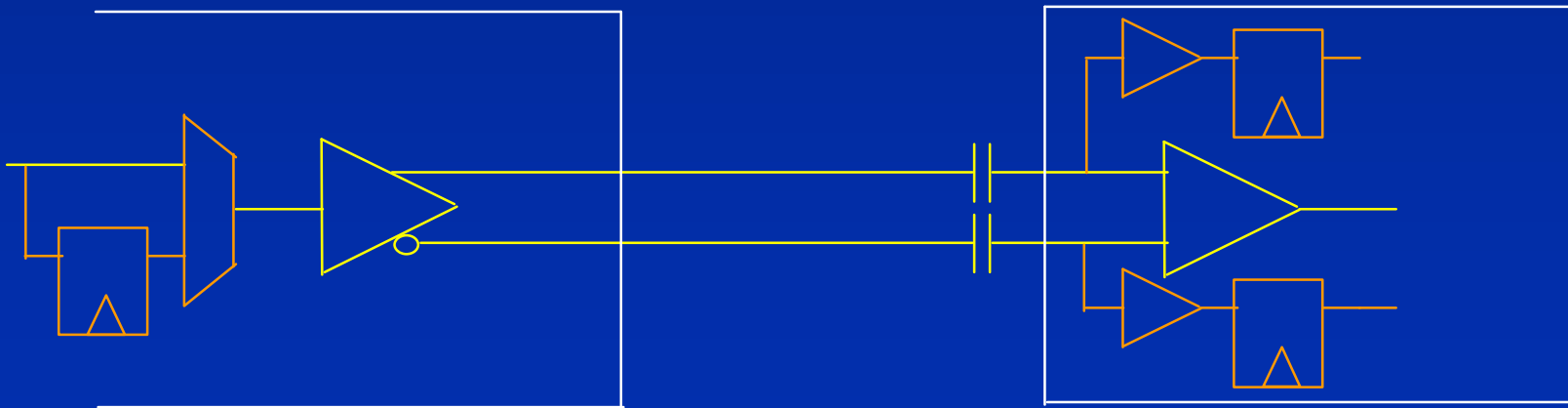
1149.1 Full Differential

- 1149.1 compliant (analog model)
- Effectively ignores the “-” line, poor diagnostics
- Provides poor detection/diagnosability
 - Can fail to detect open solder/missing caps
 - Can fail to detect some shorts
 - Yet these defects damage the parametric performance of path



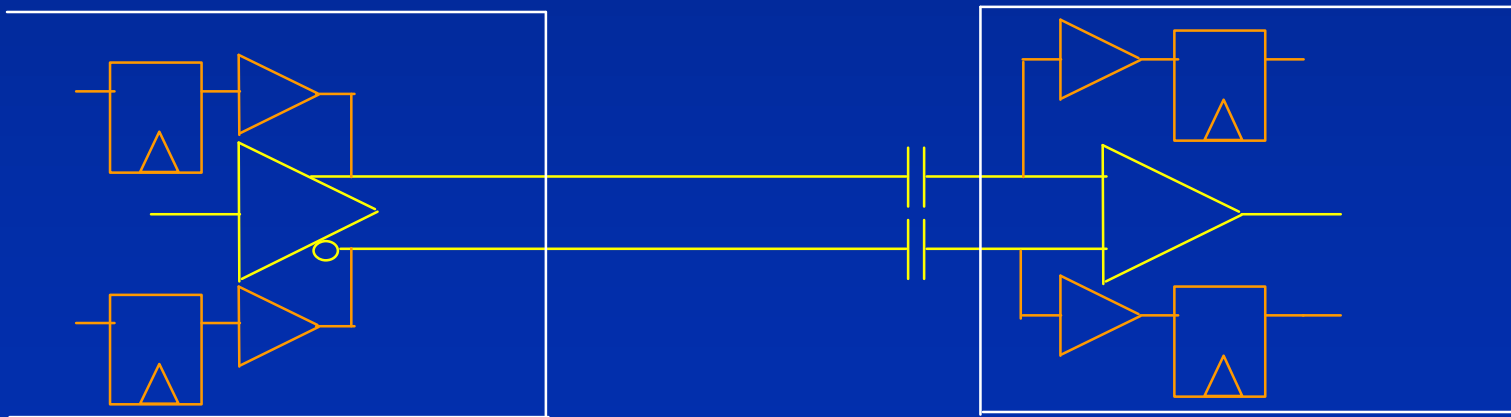
1149.1 Differential Drive / SE Receive

- 1149.1 compliant ?? (debatable)
- “+” and “-” lines always opposite
- Requires separate test receiver circuits
- Does not mask any faults, but diagnosis not full



1149.1 SE Drive / SE Receive

- 1149.1 compliant (no longer differential)
- “+” and “-” lines can be independent
- More noise and Ground/Bounce generation
- Requires separate test driver & receiver circuits
- Best possible testability and diagnosability
- Driver performance scalability is more difficult



Differential Technique Comparison

1149.1 Diff Technique

Full differential	<ul style="list-style-type: none">+ 1149.1 compliant+ mitigates ground bounce/noise- poor fault coverage and diagnosis
Diff drive / SE receive	<ul style="list-style-type: none">- 1149.1 compliance issues+ mitigates ground bounce/noise+ good fault coverage and diagnosis
Single-ended / single-ended	<ul style="list-style-type: none">+ 1149.1 compliant (- but noisy/GB)- impact on driver design: scalability+ best fault coverage and diagnosis

AC EXTEST Technology Comparison

AC EXTEST Technology

Timing-based	Freq-based	Edge-based

Timing-based Scheme in a Nutshell

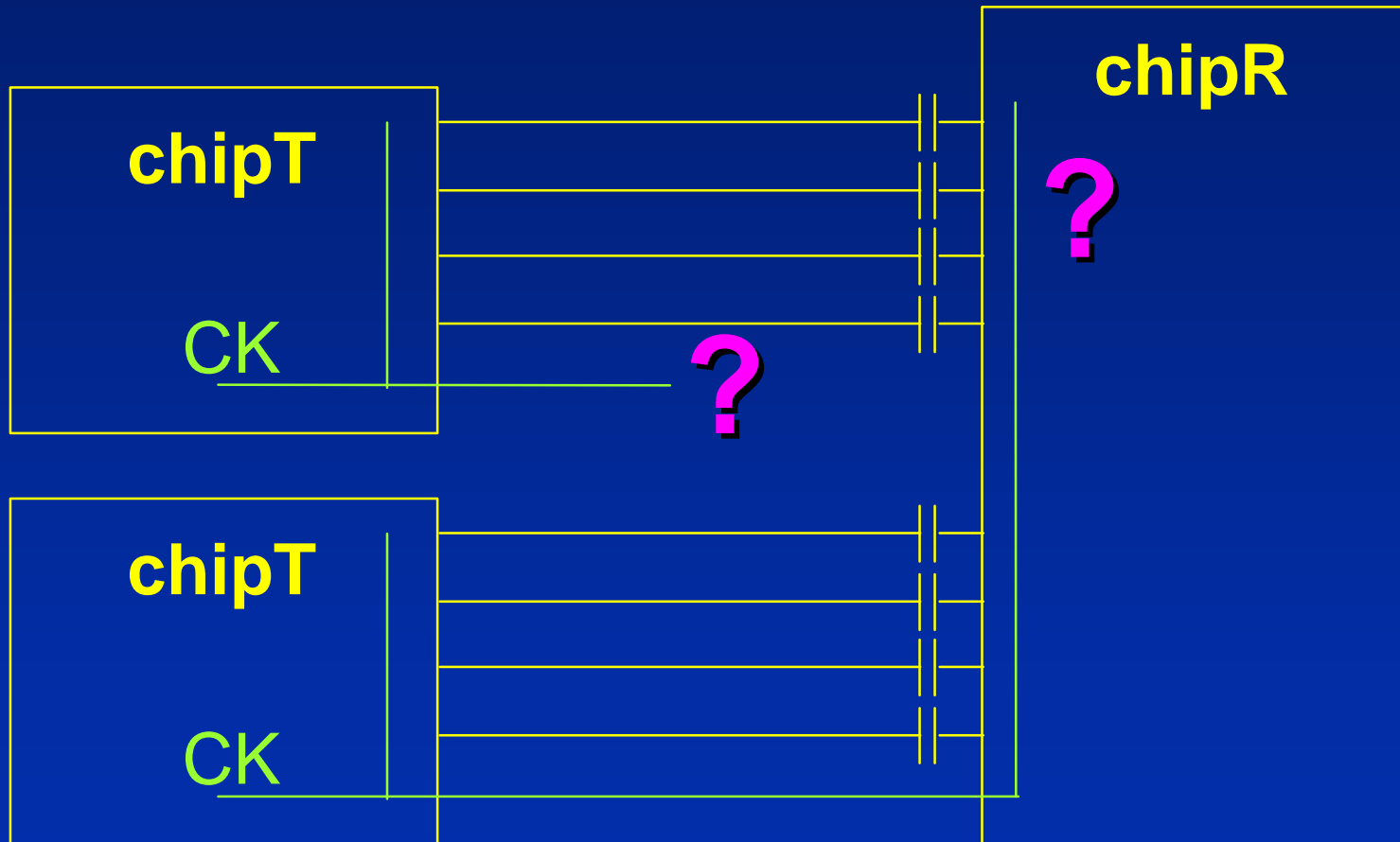
- Drive a known AC pattern from chip to chip
 - A '0' or a '1' pattern chosen by Boundary Reg bit
- Synchronize with clocked trigger across ICs
 - Trigger selects a data bit (0 or 1) from the pattern at receiver
 - Skew management important on clock and event initiation
- The coupling capacitor will pass the pattern
- Modify DC-EXTEST circuits on driving chip
- Use pattern matching circuit on receiving chip
- Modify DC-EXTEST software
- Must use either local or global reference clock

Timing-based Schematic : Local Clock

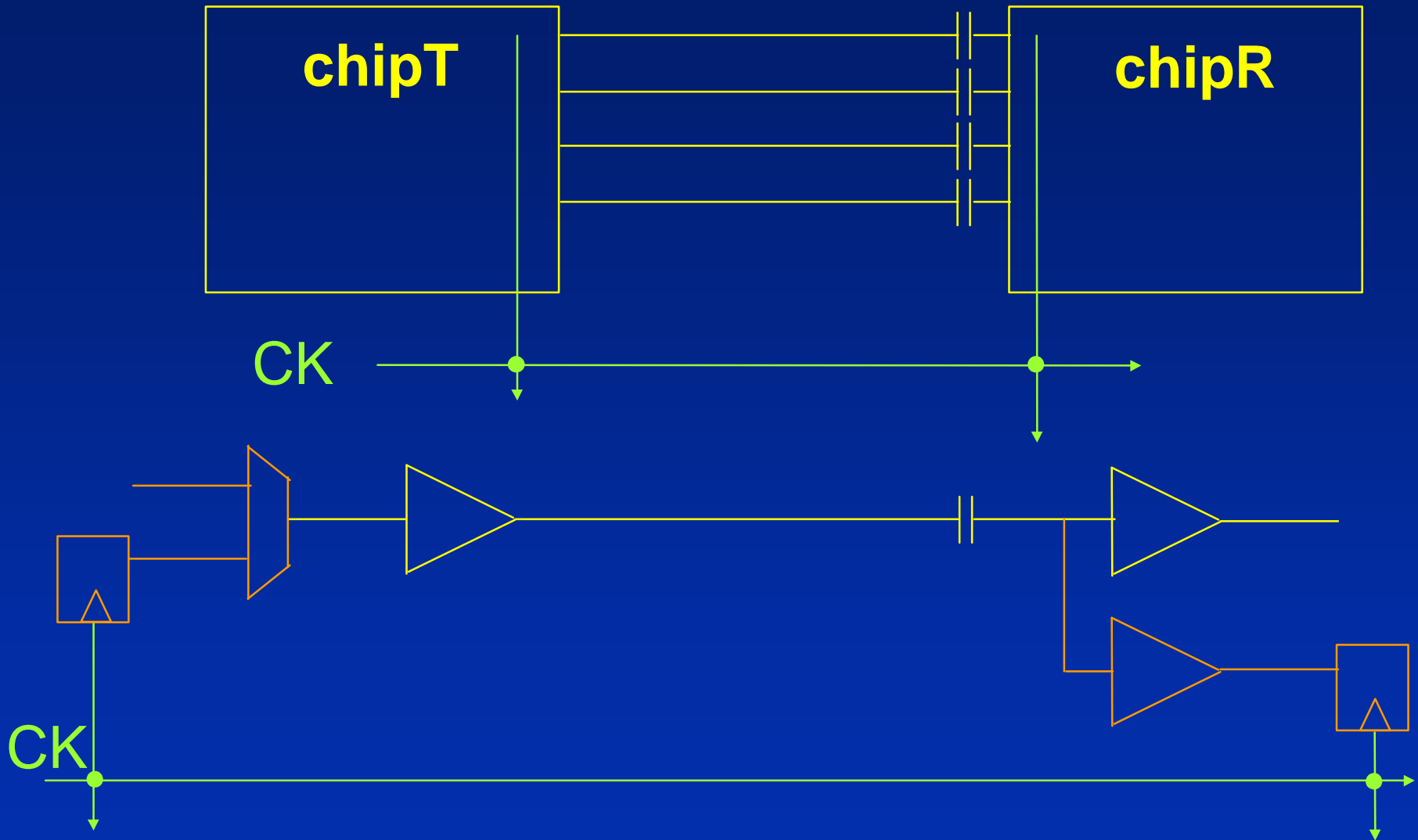
(chipT sends timed waveforms to chipR, skew spec is critical)



Topology Problem with Local References



Timing-based Schematic : Global Clock

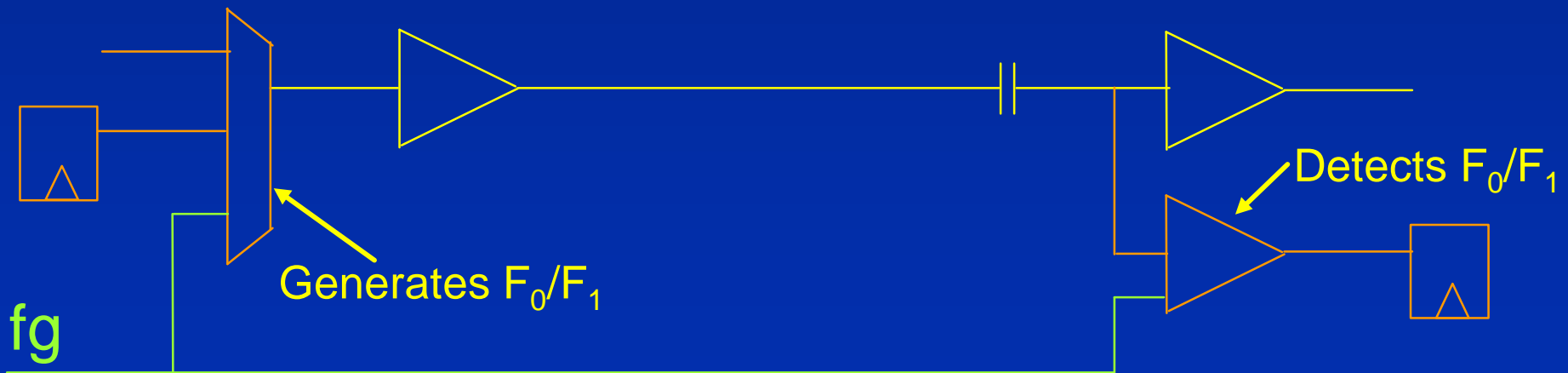


Frequency-based Scheme in a Nutshell

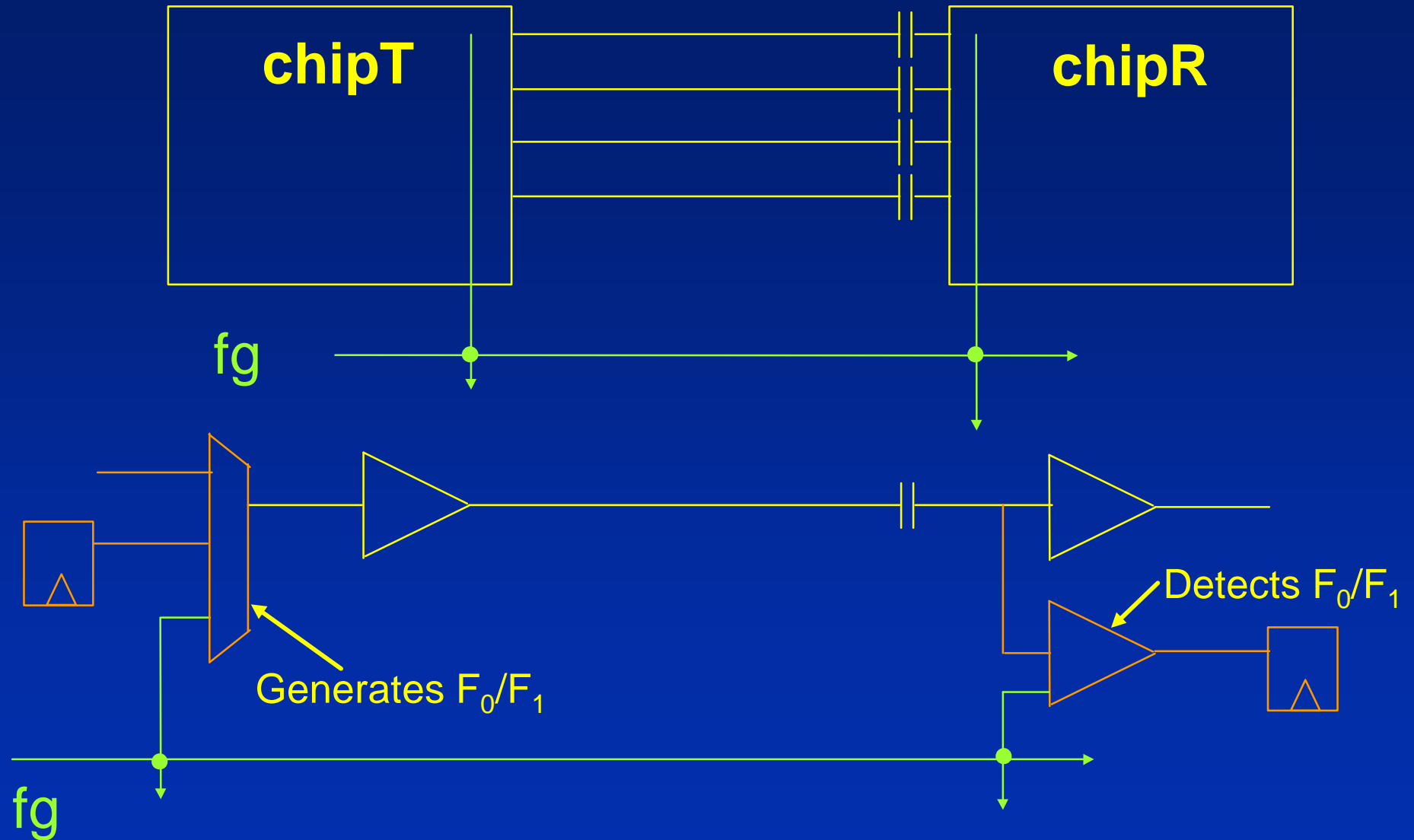
- Drive 1 of 2 frequencies from one chip to another
 - Derived from a reference frequency f_g
 - Frequency F_0 represents 0, F_1 represents 1
 - Driven frequency selected by bit in Boundary Register
 - No phase dependencies - 'phaseless' - only frequency matters
- The coupling capacitor will pass the waveforms
- Modify DC-EXTEST circuits on driving chip
- Use frequency detector circuit on receiving chip
 - Boundary-Scan data is encoded in many edges
 - Discrimination interval required, provides noise rejection
- Modify DC-EXTEST software
- Must use either local or global reference freq

Frequency-based Schematic : Local Clock

- Requires agreement on value of fg across system



Frequency-based Schematic : Global Clock



Edge-based Scheme in a Nutshell

- Drive a fast edge from one chip to another
- The coupling capacitor will pass the edge
 - Waveform is differentiated by high-pass filter
- Leverage DC-EXTEST circuits on driving chip
- Use +/- edge-detector circuit on receiving chip
 - Waveform is integrated back into original form before capture
- Leverage DC-EXTEST software completely
- No references needed
- Receiver must tolerate “low” frequency signal
- Receiver must reject noise.

Edge-based Schematic



Key is +/- edge-sensitive receiver with hysteresis

AC EXTEST Technology Comparison

AC EXTEST Technology

Timing-based	Freq-based	Edge-based
<ul style="list-style-type: none">- Extra pin- Skew critical+/- Digital ckts- Scalability- Noise	<ul style="list-style-type: none">? Extra pin+ Phaseless+/- Analog+ Scalability+ Noise rej.	<ul style="list-style-type: none">+ Small+ Simple+/- Analog? Scalability- Noise

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Where the proposals fall now

AC EXTEST Technology

1149.1 Diff Technique	Timing-based	Freq-based	Edge-based
Full differential	Cisco MSA		
Diff drive / SE receive	Cisco MSA with special receivers	Agilent 1st proposal	Philips proposal
Single-ended / single-ended			Agilent 2nd proposal

Comparison Criteria

- Variables to trade off:
 - Fault coverage and diagnosis quality
 - Circuit performance impact and Silicon area
 - Scalability (new processes, higher frequencies)
 - Robustness of test circuitry
 - Leverage of test software
- Fault detection can depend on implementation
 - Full differential vs. SE receivers
 - Trip voltages and sample times

Caveat!

The simulation results on the next slide are for a particular implementation of both driver and receiver. Different designs with different offsets and thresholds can behave differently. Simulation needed to assure.

Fault Detection Comparison

	Fault	Timing	Frequency	Edge
1	Missing Cap		✓	✓
2	Shorted Cap	✓	*	✓
3	dr open		✓	✓
4	rx open		✓	✓
5	dr s-a-0	✓ ?	✓	✓
6	dr s-a-1		✓	✓
7	rx s-a-0	✓	✓	✓
8	rx s-a-1	✓	✓	✓
9	dr+/- short	✓	✓	✓
10	rx+/- short	✓	✓	✓
11	dr+/rx- short	✓	✓	✓
12	dr-/rx+ short	✓	✓	✓
13	drA-/drB+ short		✓	✓
14	rxA-/rxB+ short		✓	✓
15	drA-/rxB+ short	✓	✓	✓
16	rxA-/drB+ short	✓	✓	✓

* Detectable with DC Extest

Fault Detection Conclusions

- Timing, full differential
 - All opens and missing caps not detected.
 - 25% shorts not detected.
- Frequency, differential drive/SE receive
 - Only the shorted capacitor is not detectable. Shorted cap CAN be detected with DC EXTEST, using standard interconnect test.
- Edge, full SE
 - Complete coverage, best diagnostics.

Recommendations

- Single-ended receivers give best detection and diagnosis
- Differential driver best
 - No loading of critical circuit
 - Much less noise/ground bounce
- Frequency and Edge-based methods best
 - Have best defect coverage
 - Frequency: easier to specify, lay out and route
 - Frequency: most tolerant of noise/ground-bounce
 - Edge: smaller and leverages the most software

Issues

- Diff-drive / SE-receive violates 1149.1 ??
- Fault diagnosis needs more investigation
- Realistic transmission line modeling needed
- Realistic package parasitic modeling needed
- Bidirectional data flow needed ??
- Fault detection can depend on implementation
 - Full differential vs. SE receivers
 - Trip voltages and sample times