

Section 6 review

- Most people did not fully review the material but felt comfortable enough with the material to concentrate specifically on Section 6.
- Sang brought up the point that some mention of testd should be made – even as a place holder. Ken will add an editors note.
- Sang ask about how simulation affected what was in the draft – Ken said yes it does and in fact he has made some changes based on that. Noted whether hysteresis would affect the results of the simulation. Carl noted that he built a “window comparator” and then referenced the data to the hysteretic buffer.
- Group was urged to look at simulations and summary sheets
- **AI – Carl and Sung still need to reconcile differences in simulation**
- Ken pointed out that transitions are relative to the performance of the mission receiver.
- Bob asked if 6.2.1 should specify “single-ended” test receiver
- Sung asked if you could share logic with input receiver – change wording to test receiver function
- Ken mentioned that he and Carl are considering changing range on 6.2.1b to 50% to 90%. **(Open issue) Carl mentioned that there may be a few changes to simulation that would result if these changes would be made (LVDS). Ken asked if window could be even narrower. Jeff said could possibly set that at delta V min. Designer will probably build in slop. Jeff will sit down with chip designers – maybe specification should say as close to 100% as possible. Sang asked if we are considering testd – we will need to reconsider these numbers. Carl said it would require a different rule.**
- Tapan asked if clever designer that designs outside of range will violate the standard.
- Carl mentioned that mission receiver designer will define the minimum delta V. Board designers need to adhere to that specification. At that point, test logic designer can determine his threshold point.
- Sung pointed out that 6.2.1b is most important for test coverage. Also, pointed out that this will be difficult to verify. Mentioned the need for compliance testing.
- Ken pointed out that later in the document compliance verification needs to be discussed. Could be more difficult when capacitor is inside chip.
- 6.2.1c – Ken mentioned that the current rule does not rule out 0 hysteresis delay (as specified in 6.2.3a). (Open issue) Ken will reword the rule to specify some delay should be added.
- Carl asked that last sentence in note 3 be deleted. Pandu asked what would happen if the buffer delay is large with respect to the hysteresis delay. Carl mentioned that as long as the sum of all propagation delays is less than the Ttest it should not affect the operation of the circuit. Jeff recommended that we add a statement that hysteresis delay should be small relative to Ttest. Sung mentioned that the sum of all delays should be less than Ttest.

- 6.2.1d – Jeff questioned “when the instruction is loaded”. Carl mentioned to change “when” to “while or whenever” Bill suggested to change “loaded” to “executed” – Adam suggested “operating”.
- Jeff mentioned that should add a note mentioning that this refers only to the operation of the receiver not protocol.
- 6.2.1e – Bill requested changing “are chosen” to “will be specified”.
- Sang and Sung asked if note 2 specifies translation between edge and technology. Suggested that Ken should add “logic level” and “Signal levels”.
- Jeff asked philosophically if a designer wants to meet our intent rather than use our suggestions, do we adequately show what our intent is.
- 6.2.1f – Carl mentioned that this applies to hysteretic comparator, if window comparator is used we will need to change the rule.
- Jeff and others mentioned change produce to maintain the logic level.
- Sung brought up the point that Vhyst should/may be different on positive and negative transition.
- Jeff asked whether we could just reuse the mission receiver as the test buffer. Carl pointed out that the mission receiver would not be hysteretic – would need to add a switchable mode. This is covered by rule b.
- 6.2.1h - Carl asked to specify the reason for the rule. Reason to assure that the decay will not happen so fast so as to be confused with a valid transition. Ken mentioned so far that the minimum requirement would be for 700pf. Ken to enhance example information into notes.
- Jeff questioned – how will we validate this? Don’t know what the capacitor will be. Carl questioned whether or not this information could get passed in BSDL. Jeff mentioned that chip designer should specify based on verified chip performance. Sung mentioned that some of this performance may be specified by mission performance. Big concern since this checking requires some sort of spice simulation and cannot be verified at the chip level – will need to specify this later. Sung questioned how you would even test this at a board level?
- The question came up as to whether or not we need to specify tester performance (to meet valid transition time requirements). It was pointed out there is no specification for valid transition time. Suggestion was made that tester performance should be specified in terms of Thyst.
- 6.2.1i – should we added a note equivalent to 6.2.1h note 1. Also, should assign a name to the multipliers (low pass and high pass filters). Ken recommended that there should be some specification with respect to the ration of the high pass and low pass filter. The ratio will affect the maximum voltage swing. Can specify that the ratio should be a minimum level (say 2:1).
- **Action – Carl and Ken to rework rules H, I and J.**
- 6.2.1j – Ken reviewed figure 29 to discuss how initialization logic allows us to measure the level at the pin during Capture DR point. Ken will add waveforms for Set and Reset inputs to flop. Should refer to data as Point A for consistency.
- Note 2 – Carl suggested a recommendation that states what note 2 says. **Action – Ken to make all references to Vbias and Vt consistent.**

- 6.2.11 – test receiver samples and holds at some time after falling edge of TCK (after Init is clocked in). Action – Ken to modify rules L and M.
- Should change when the command is loaded to when command is operating.
- 6.2.2 - Need to add permission to share circuitry with the mission receiver
- Figure 33 – Carl noted that raising the minimum swing trip to 90% will make Thyst harder to meet. Ken will relook at the implications of raising the trip to 90%. Is there a need to specify what the minimum pulse requirement is going into the flip flop and how do you meet it.
- Ken talked about Figure 26 on page 28 of draft 2.2. Mentioned that hysteresis delay could cause a negative voltage for some period of time. This would also reduce noise immunity as well. It can be controlled by the ratio of high pass to low pass filter. Could be an issue if the high pass filter is on the chip (may force on chip r's and c's to be too big). Will need to add explanation to the draft