Minutes for April 3rd Working Group meeting

Attendance is shown in the working group attendance spreadsheet.

Voting

Everyone ok with people who are not able to attend dialing in to vote or voting by email. Eligible voting members will be informed of logistics during teleconference.

Physical implementations

Jeff Rearick - .13 micron technology (CMOS SERDES). Phase and Activity based implementations were too difficult to implement. Edge and Frequency were easy to implement. Drive side push back was as expected. Possiblility of up to 6ns (+- 3) of skew added. Skew was on the launch/capture action only – not shifting. Problem was the test logic was required to be added to lower frequency (parallel) area. Phase and activity were affected most by clock skew.

- Carl could not understand the reason for skew on the receiver side. Also, with 6ns of skew – assuming ¼ cycle skew tolerance should be able to run around 40MHz TCK.
- External time constant was assumed to be around 50ns.
- John stated that the design goal for the chip was lower test time which got to 50Mhz requirement for minimum frequency on chip – that is why phase and activity were dropped since skew was too high to support that frequency.
- Jeff pointed out that requirement to keep PLL running may be a compliance issue with dot 1.
- Jeff also pointed out that in CMOS area it would be next to impossible to put the test logic in the high frequency part of the chip (driver side especially).

Sung – Some chips have been built with partners, plus Cisco has already done a test vehicle. Sang mentioned FPGA implementation of test vehicle. Assumed 100nf coupling capacitor. LVDS test receiver, mission mode (300 Mhz) – no null, short or AC detect. Test vehicle also provided fault insertion capability. Detected most of 16 faults. Shorted capacitor was not detected – can be detected by failure of DC EXTEST. Were able to identify all opens and most shorts. Couldn't detect shorts before the capacitor (shorts to Vdd were not detected). Would not work at frequencies below 800Khz. – primarily due to decay of signal. Results correlated pretty well with simulation, didn't try low frequency simulation though.

One partner has already implemented MSA proposal into quad serdes. They claim that the part is working ok. AMCC has tested physical implementation of activity proposal. So far they are seeing good results. Two other companies implementing MSA proposal – one company implementing higher threshold window comparator (may scale it down). Internal ASIC will be available in the June timeframe.

*** - Final analysis is that all proposals can be made to work in physical implementation.

Sung raised a concern about specifying bandwidth of driver and receiver. Also pointed out that lower bandwidth receivers may be a problem. Need to work on a more specific definition of input receiver parameters (Thyst specifically). Still a concern about noise vs. legitimate signal. What noise is really expected?

Break time…

Sung's presentation on input buffer and new MSA proposal (posted on the web)

Sung discussed issues with null detection – hysteretic buffer is not able to do this well. Carl pointed out that the use of VCOM/VREF on slide 11 could be a problem based on previous discussions of the working group.

Discussion on null detect (what is the advantage?). Sung mentioned simpler circuit and more compliance with dot 1. Carl mentioned that since we're talking about dot 6, compliance with dot 1 is less of a factor. Carl pointed out that the test buffer accomplishes the same thing that the null detect logic does – because the two cells will track each other. He mentioned that throat clearing is imperative though to make the test receiver work. Sung mentioned issue with putting capacitor in the test receiver (Charles mentioned this is only valid when you are not in a pure AC EXTEST mode). Jeff questioned whether the capacitor is easier or more diffcult to implement 6 resistors vs. capacitor. Capacitor size could be as much as 15% of the channel size. Could be less than that though. Either way the capacitor is seen to be a significant disadvantage. If we can deal with DC offsets and handle stuck at faults – it may be worth revisiting the window comparator. **Sung will report to the group about the size of the capacitor used in the application that he reported about. Also, would it be possible to use a lower value capacitor. Sung and Carl to discuss single ended vs. differential approach and the benefits/disadvantages of the test receiver (with capacitor) vs. MSA window comparator (no capacitor).** Ken pointed out that we still haven't looked at the case of single ended AC coupled net. Can MSA deal with this? Also, issue of diagnostic resolution with differential net came up.

Since MSA proposal will not use the low pass filter (capacitor) – some of the cells in the comparison will need to be changed. Charles pointed out that in Infiniband it is possible for VREF to be outside on voltage swing on the inputs. This could be a problem for window comparators – unless you generate VREF in a different way.

Final word – the choice comes down to capacitor size vs. diagnostic resolution (overriding boundary cell with error information), single ended net operation (no example shown yet) and VREF outside of voltage swing for DC circuits.

Activity detection is covered by the test receiver preloading (throat clearing).

Point was made that functional testing of the component is an issue. Simple window comparator would be easier to test.

Frans suggested adding another column for single ended nets. **AI – Sung to provide a single ended version on the window comparator.**

Sung believes that you will still need null detect and AC detect on top of the test receiver. This may or may not be the case – **Sung will investigate**.

Protocol open discussion

Is there better noise immunity by sampling on the 16th clock (phase) vs. 1st clock (edge)? There may be issues with the window comparator (possibly mission mode comparator), which would require continuous transitions on the net. Still debate as to whether having a 16 clock window provides lower probability of noise spike occurring at the sample time. Sung gave an example of circuit which requires a continuous data stream. Since all of the testing on MSA occurs in RTI with continuous data stream, it appears that MSA would not have this problem. Carl pointed out that it is possible to provide a continuous data stream while in RTI using throat clearing logic. **Question/AI: is pulse stream required for edge detect – Carl/Sung.** Issue that there may not be a continuous clock stream in RTI. You could make toggle during RTI a permission on the driver side. This would allow drivers to implement this feature if the driver requires it. Doesn't matter to the receiver.

Upper limit on TCK now imposed on test receiver if data is toggled in RTI. **Open issue: is current TCK frequency too low**. Group would prefer not to make toggle in RTI a permission vs. just not specify it. Sung believes that technology may be trending to require continuously toggling data. **Sung to try to arrange a meeting with the vendor that requires continuous toggle and the protocol team**.

Point was brought up that test receiver can detect same information in one transition that MSA can detect in two.

Verification and synthesis of window comparator vs. test receiver – window comparator might be a little easier but this is outside the protocol layer. Will consider this as a physical layer problem.

BSDL modifications – Original question was if you have to touch the BSDL anyways, is there a disadvantage of doing more modifications for any given proposal.

Answer from the group is that if modifications go beyond extensions then there could be a differentiator.

Ken presented a drawing that he sent out last night, showing an implementation of a boundary cell that also included hysteresis loading as well. Carl still has a few issues with the update latch (when is it clocked). Also, issue with PRELOAD affecting the contents of the update latch.

Analog setup at the pad – There may be some setup required at the pin which would be best handled by an initialization instruction which is executed prior to entering test mode. Programmable I/O might be a good example. This was discussed quite a bit inside the dot 1 working group but nothing came of it. Group believes that this has to be addressed in dot 6. **John will contact Adam Ley to find out if he can get any archived information from dot 1 (work with Tom Langford).** Sung also suggested getting input from Altera and Xilinx. This should be done in general with regards to the entire standard. **Bill will try to get feedback from FPGA vendors**.

Noise immunity vs. masking faults – the group decided that noise issues are not in the structural board test domain. Therefore masking of noise issues should not be a consideration. Group is concerned that typical board test environment is very noisy therefore noise immunity is very important. Group is fairly confident that we are not masking failures. Sung is not so sure. Group decided that noise immunity should be a parameter of input receiver design (setting of thresholds).

Group completed by discussing major plusses and minuses. It was suggested to remove test receiver discussions out of the picture for now and to assume the chapter 6 receiver on all protocols. The discussion came down to edge detect being most simple implementation and all proposals seem to be equal on most other counts. The question was raised – is there any advantage in other proposals that would offset the simplicity of the edge proposal. A proposal was made to use the edge detect with throat clearing and allow multiple transitions in RTI. This may satisfy Sung's requirements. In addition, if set and reset of the flip-flop are blocked upon leaving RTI, noise vulnerability is reduced significantly.

At this point the group did not want to risk any more long discussions and adjourned.