

Meeting Minutes – 7/13 ACEXTTEST Teleconference

Attendees:

Bill Eklow, Cisco
Ted Eaton, Cisco
Carl Barnhart, IBM
Ken Parker, Agilent
Sung Chung, Cisco
Sang Baeg, Cisco
Adam Ley, Asset-Intertech
Chenhuan Chiang, Lucent
Tapan Chakroborty, Lucent
Steven Terry, HP
Brad Ishihara, Altera
John Rohrbaugh, HP
Mike Richetti, Intellitech
Terry Borrow, Teradyne
Jeff Rearick, HP
Tom Langford, LSI
Bob Russell, EMC
Frans de Jong, Philips
Robert Shuelke, AMCC
Sabih Sabih, Xilinx
Harry Halvershorn, LogicVision
Steve Sunter, LogicVision
CJ Clark, Intellitech

The meeting was essentially divided into 3 parts, with each Tiger Team presenting its list of issues and proposals to resolve those issues.

Board Tiger Team

The Board/System Tiger team presentation is on the General Information page on the website (www.acextest.org). It is titled: Board/System Tiger Team Presentation for 7/13 Teleconference.

Adam Ley presented the Fault Model which was agreed to by the Board/System Tiger Team. Questions were asked about shorts to rails, clocks or midrange reference voltages. Rail was subsequently defined as a voltage that would be either much higher than the voltage threshold of the net in question, or much lower. This left shorts to clocks and midrange reference voltages still to be dealt with. Adam agreed to add midrange voltage references (rails) to the fault model. There was also considerable discussion about shorts between AC coupled nets and DC nets. This issue still needs to be dealt with.

Question was asked about resistive shorts and at speed problems – group reaffirmed that these would be nice to look at but the scope was still faults which would be covered by dot 1 in a single ended, DC domain. Further discussion concluded that very resistive shorts would occur in normal manufacturing process.

The Board/System tiger team then presented its board/system requirements. They are:

- No requirement for distinct/exclusive fg
- No globally distributed high speed test clocks
- No frequency shifting of TCK (this issue was deferred to the tools team)
- Vectors should be timing independent (no requirement for raising TCK frequency)
- Need to consider how to control AC and DC signals

Chip Tiger Team

The Chip Tiger team presentation is on the General Information page on the website (www.acetest.org). It is titled: AC EXTEST Chips Tiger Teams Recommendations.

Robert Shulke discussed the Chip Team's recommendations. The following questions/issues came out of the discussion:

- The chip team was asked to help finalize the fault model which was presented by the board/system team
- Still need to address Edge vs. Data approach
- Need to address maximum/minimum TCK frequencies (what should they be and how to you specify them)

Tools Tiger Team

The Tools Tiger team presentation is on the General Information page on the website (www.acetest.org). It is titled: Tools Tiger Team Evaluation.

Mike Richetti presented the tools issues to the group. The following questions/issues came out of the discussion:

- Is it possible to use dot 1 (DC EXTEST)
- It may not be possible to detect shorted caps by using DC EXTEST if technologies are different
- Clock frequency made need to run as low as 10KHz
- Modelling and compliance checking
- Can ICT handle clock frequencies and required drivers/detectors

There were 2 new proposals which were presented to the group.

1. Bob Russell would like the group to consider using a BIST type approach by building test generation/detection logic into the functional encoder/decoder. Bob will present a proposal to the group.
2. Ken Parker presented a new version of the edge detection scheme that is very similar to dot 1. In essence, the proposed scheme would generate a single edge as opposed to a series of edges or data. The proposal can be found on the General information link. The paper is titled: A 4th AC EXTEST Proposal. There is also a supplement document titled: Proposed Additions to the Integrating Receiver Proposal.

Open issues that need to be resolved:

1. Finalize fault model
2. How to deal with shorts between signal/clock, signal to in between V, AC to DC
3. Edge vs. data approach
4. Modelling and testing for compliance to the standard
5. ICT issues (can the ICT tester support the frequencies and drive/receive protocols required?)