

Clock sync protocols as submitted to the p1394.1 committee

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**This contribution is one of several, presented for independent review.
An overall contribution, which provides the context for multiple contributions,
is also provided in BR047R08.**

Bus bridges are minimally required to synchronize clock frequencies. This proposal also distributes a uniform time, as produced by the primary portal's cycle-master node.

High performance Serial Bus bridges

1. Introduction

1.10 Clock synchronization

1.10.1 Clock routing

To simplify interactions, all isochronous-capable nodes are expected to have synchronized timeOfDay clocks. The timeOfDay clock reference is generated by one node, the cycleMaster on the primary bus, and distributed to other nodes, as illustrated by the dotted lines in figure 1.

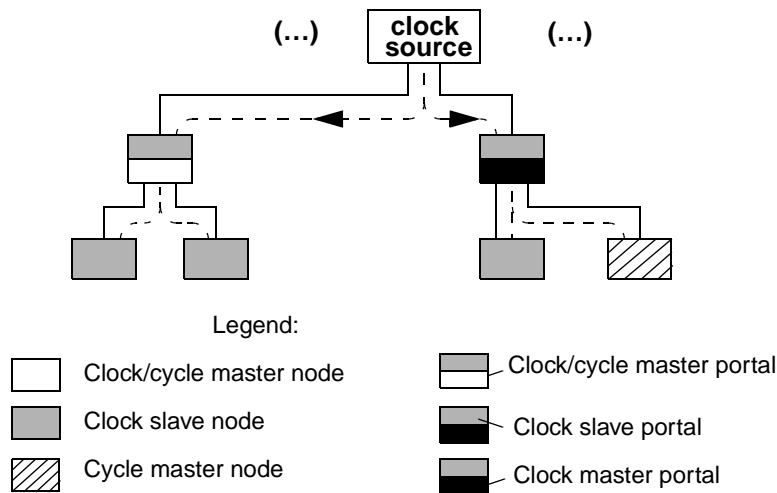


Figure 1—Clock synchronization

On secondary buses, the clock-reference node is the alpha portal and clock distribution is more efficient the alpha portal is also the cycle-master node. An alternate cycle-master node may be used, but only if the cycle-master node has the capability of phase-locking to the clock-referencing alpha portal.

1.10.2 Clock synchronization

Although simple in theory, cascading phase lock loops, as illustrated in figure 2, complicates the dynamics of the overall system. This design approach should not be used.

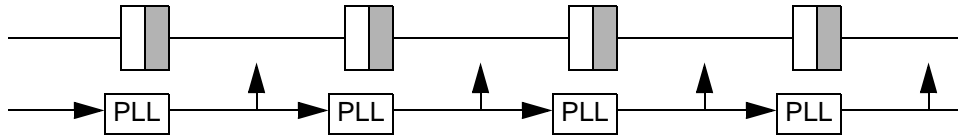


Figure 2—Overly simple clock delivery

Instead, the clock estimate is forwarded through bridges, and PLLs are used to remove jitter from the local timer on each bus, as illustrated in figure 3. This reduces the dependencies of each bus clock from PLL dynamics of the others..

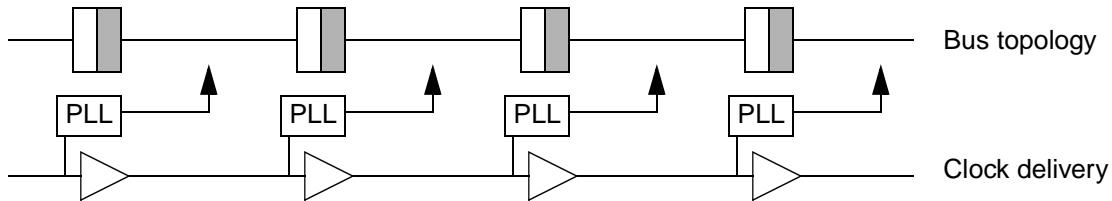


Figure 3—Desired clock delivery model

This design model mandates two time transmissions on the bus. A jitter-reduced signal marks the start of each isochronous cycle; in Serial Bus, the cycle-start packet transports this information. A second PLL source signal is repeated (with additional jitter errors) to the next bus with no PLL jitter filtering; the clockSync packet (see xx) serves this purpose.

1.10.3 Cycle-master synchronization

On remote buses, the clock-synchronization protocols proceed as follows. In every isochronous cycle a cycle-start packet is transmitted. During each cycle-start packet, all portals latch their current time value. During the following isochronous cycle, the clock-reference node transmits its previously latched value in a clockSync packet.

Other clock-slave nodes derive calculate an observed error as the difference between the clockSync packet and their latched value. That error is added to the free-running clock in the clock-slave nodes, to generate the clock-reference value that is distributed on the adjacent bus.

To minimize special routing requirements, the clockSync packets are “routed” by having alpha portals redistribute this information. The clockSync packet itself is not (strictly speaking) routed, but the observed bus-A time reference is either applied to bus-B or ignored, based on the portals’ source-routing tables.

1.10.4 Clock redistribution

To reduce the phase-lock whiplash effect, bridges are expected to redistribute a delayed clock reference and (when assuming the role of a cycleMaster) a phase-locked time in the cycle-start packet, as illustrated in figure 4. The intent is to redistribute an unfiltered (but delayed) clock reference, while phase-locking the cycle-start packet to reduce clock jitter effects.

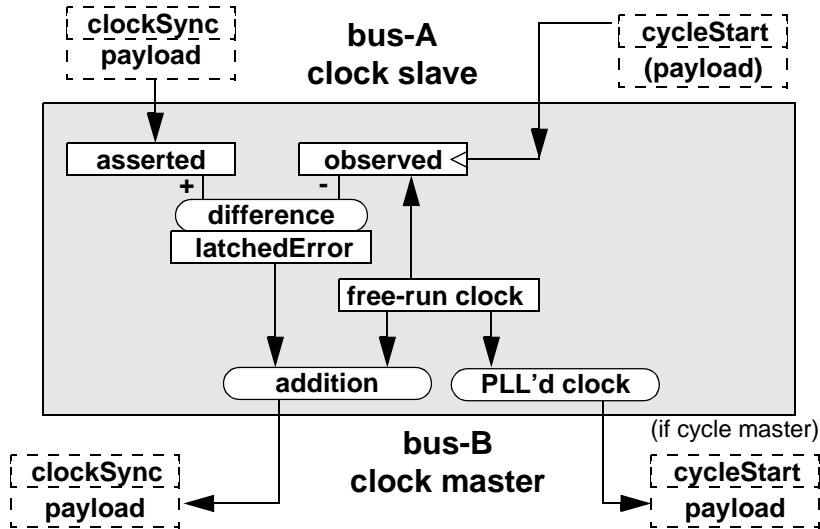


Figure 4—Clock redistribution model

For additional accuracy, the free-running clock value may be rate-adjusted, based on the long-term average of the *latchedError* value. Such rate adjustments shall not the free-run clock frequency to deviate beyond the specifications mandated by the attached bus standards.

7.5.2 clockSync packet format

The isochronous clock-sync packets are generated by the clock-master portal as a reference for the local cycle-master and clock-slave portals. Fields within the packet are used to distribute the current time value, as illustrated in figure 5.

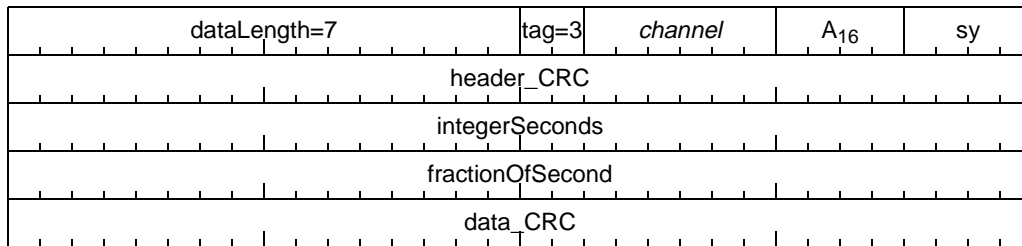


Figure 5—clockSync packet format

The 32-bit *integerSeconds* field specifies the desired clock-reference time, in seconds. The 32-bit *fractionOfSecond* field specifies the desired clock-reference time, in fractions of a second.

Annexes

Annex C

(informative)

Wireless HiperLan-2 layer

C.5.2 Isochronous delivery times

Data delivered in frames, where frames are sent periodically approximately once every 2ms. The 2ms clock is not necessarily synchronized to the net's 125ms isochronous cycle, as illustrated in figure C.1. This implies that each frame may contain 8 or 9 isochronous packets, depending on relative timings of HiperLan-2 frames and isochronous cycles on the interface.

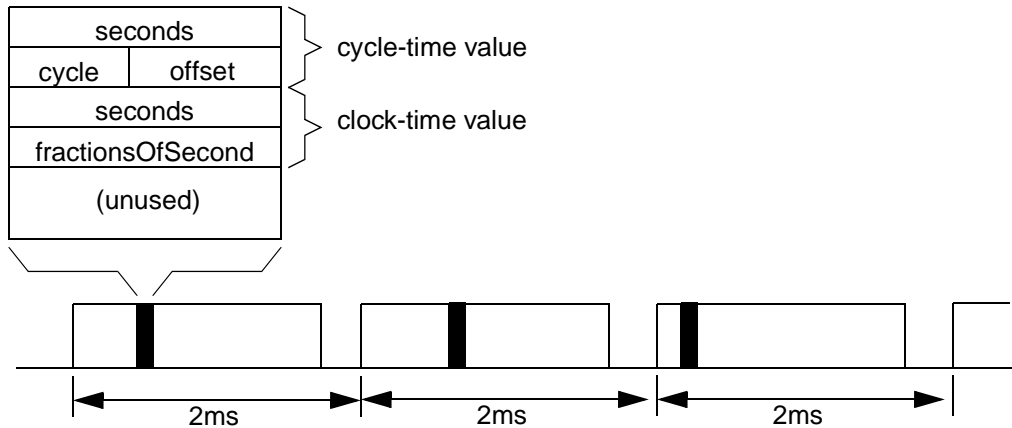


Figure C.1—Clock synchronization facilities

Hiperlan-2 clock distribution is done once within every 2ms frame. Time estimation involves latching the local-time value at the beginning of each frame, on all nodes. The clock-master copies its sampled time into a “packet” that is placed within the following frame (not illustrated). The clock-slave nodes compare their sampled time to the “packet” time, to estimate the error between clock-master and clock-slave clocks. The error value is latched (when stable) and used to compensate for the clock-slave’s node timer, as illustrated in figure C.2.

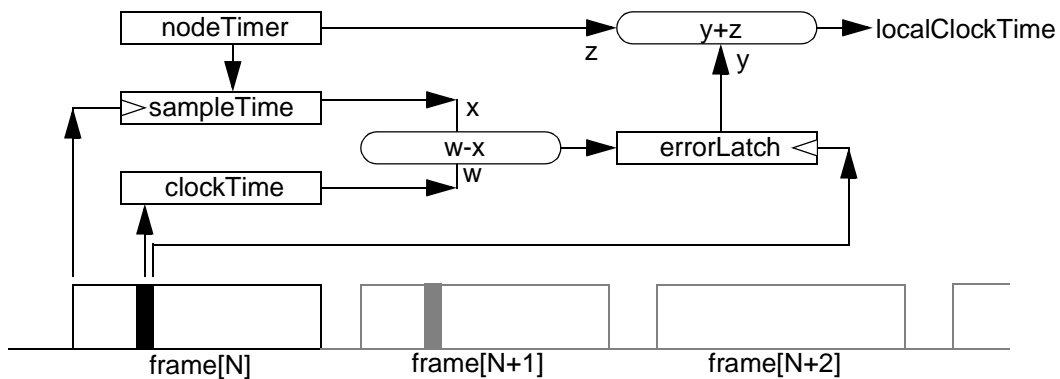


Figure C.2—Per-frame time adjustments