

# **P1394b PHY-Link Interface Strawman**

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## **1. Introduction**

This note proposes a direction for the development of a PHY-Link interface for discrete PHY and Link chips, capable of supporting speeds of S800-S3200. The emphasis of this proposal is to provide backwards compatibility in the short term with the current interface by scaling it up to S800, and to use faster clocking techniques for the higher speeds in the longer term for S1600 and S3200 interfaces. We bite the bullet of extra pins first, and the bullet of faster clocks later.

## **2. Rationale**

We need to identify the low risk way to handle S800. We are finding increasing pressure to preserve the option of isolation barriers between the PHY and the LINK. Until we can study the delay times better for the capacitor method we should do nothing that stresses the timing more. Beyond S800 the problems with isolation may be very difficult to handle cost effectively with the current interconnect scheme. Thus we propose that we need to quickly and cleanly solve the S800 problem but continue to work vigorously towards a solution to handle the higher speed PHYs in a better way. A road map towards the higher speed PHYs is therefore also proposed.

## **3. Requirements**

The following is in no particular order

1. Supports S800, or S800+S1600, or S800+S1600+S3200
2. Cost optimisation for S800 only (higher speeds may cost respectively more)
3. Capable of supporting P1394a Clause 5 at minimum extra complexity (pure backwards compatibility desirable)
  - 3.1. Existing S400 Links should be able to utilise new S800 PHYs - avoid the node being a speed trap
4. Minimises EMC and system design problems
  - 4.1. low signal frequencies
  - 4.2. low voltage
5. Support DC coupled and isolated (capacitive and inductive) interfaces
6. IP according to IEEE rules

## **4. Proposal**

The outline of this proposal is

### **4.1 S800**

The S800 interface builds on the existing scalability of the P1394a interface to utilise 16 data lines. The electrical specification is as per P1394a, and the timing is unchanged (PHY sources a 50 MHz SClk). An extra pin is introduced to indicate an even number of bytes in a transfer (so that when the pin is not present or not asserted, only a single byte is transferred - this is particularly important for ACK packets).

#### **4.1.1 Advantages**

- Backwards compatible with P1394a. Existing S400 PHYs can interoperate with new S800 Links, and existing S400 Links can utilise new S800 PHYs (avoid being speed trap)
- No new EMC problems
- No new clock or timing problems
- Easy to specify, low risk specification
- Leverage existing PHY/Link interface designs with minimal modification
- Supports DC coupled and isolated interfaces as per P1394a
- No IP issues
- Suitable for existing manufacturing technologies

#### **4.1.2 Disadvantages**

- 9 additional signal pins
- One byte extra latency (though latency in terms of SClk cycles is unchanged)
- Requires adaptation to internal datapaths which use 8 bits but faster clocks.

### **4.2 S1600**

The S1600 interface uses the same signals, but doubles the data rate. Precise techniques need to be investigated, but clocking on both edges (as previously proposed for S800) has the advantages of not increasing the maximum frequency of any of the signals, thus not compromising the existing electrical integrity and EMI properties. The doubled clock rate is used only when transferring data at S1600. Transferring data at S800 uses the rising edge only (100% compatible with the S800 specification).

It is proposed that the LReq signals and Status signals continue to operate by clocking on the rising edge only, thus maximising backwards compatibility.

The round trip time needs investigation in order to preserve the use of isolation barriers. Alternative AC timings may be needed depending on the setting of the Direct pin. Faster set-up and hold windows will be required.

#### **4.2.1 Advantages**

- Backwards compatible with P1394a. Existing S400 PHYs can interoperate with new S800/S1600 Links, and existing S400 Links can utilise new S800/S1600 PHYs (avoid being speed trap)
- Same clock rate as existing designs
- No new EMC problems
- Leverage existing PHY/Link interface designs
- Supports DC coupled and isolated interfaces as per P1394a
- No IP issues
- No extra pins (further to the S800 proposal)
- No extra latency

#### **4.2.2 Disadvantages**

- May need different AC timings for isolated interface operating at S1600
- Will need tighter set-up and hold times for operation at S1600
- Needs tight duty cycle specification

### **4.3 S3200**

The S3200 interface uses the same signals, but doubles the data rate again. This can be done by doubling the clock rate and continuing to use clocking on both edges. However, the round trip timing constraints are likely to make source clocking from Link to PHY desirable, in which case it may be preferable to use a 200 MHz clock. It is also likely that the electrical specification may have to change, both to track likely implementation technology (1.5V?) and to minimise EMC effects. Backwards compatibility may well have to be invoked via a configuration pin, with separate clocking circuits and buffers/drivers.

#### **4.3.1 Advantages**

- No extra signal pins
- No extra latency
- Can provide a backwards compatibility option (controlled by a configuration pin)

#### **4.3.2 Disadvantages**

- Technology is too early to nail this specification down (wait until it is really needed, and then see what we have available?)