

1394b PHY-Link Taskforce Progress Report 1



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1394b PHY-Link Taskforce

Status/Agenda

Since the last meeting:

1. Strawpoll approved going to S800 first, *providing* overall progress is maintained.
2. Details worked out for proposed S800 solution.

This meeting:

1. Will present details on proposed S800 solution and request a vote on approval.
2. Will present initial outline for S1600/S3200 solution.

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Details of S800 solution to be presented:

- Timing/Roundtrip delay

- Generation of 50/50 dutycycle 50Mhz clk

- I/O Pad types

- Cost considerations

- Use of predefined pad layout in PHY-link section.

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S800 - Generation of clock

Requirement: In order to maintain acceptable timing margins, a 50/50 duty cycle needs to be maintained.

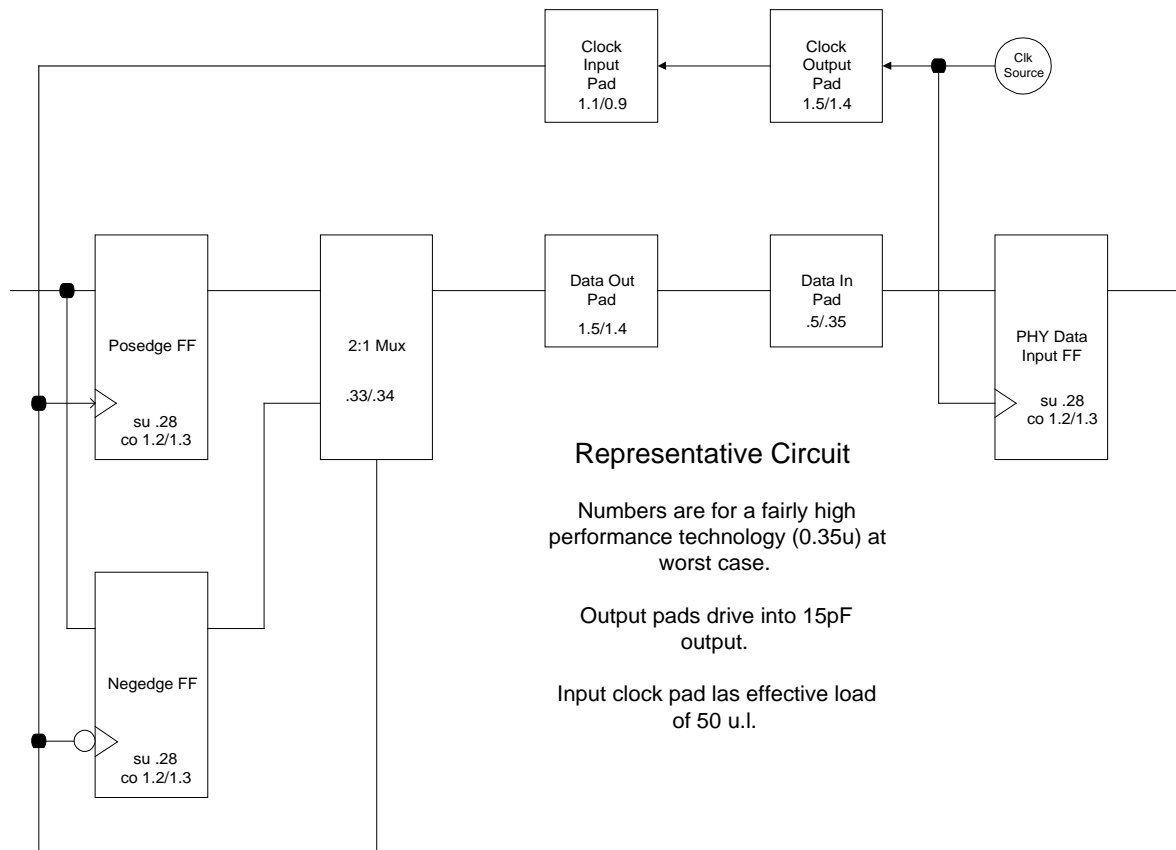
Requirement: In order to maintain compatibility with the current architecture, the clock must remain at 50MHz and be sourced from the PHY.

Solution: This can be accomplished by using a 100MHz source which is divided by 2, then fed into the PHY clock distribution network. Duty cycle then is only sensitive to instantaneous speed changes (should be very small).

Advantages: Maintains compatibility, easy and inexpensive to produce.

Disadvantages: More strain on timing margins, but avoids having to make technology changes which would throw compatibility out the window.

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| Cell | Cell Timing | Cumulative Timing | | | |
|---|-------------|-------------------|--|--|--|
| Clk Source | | | | | |
| Clk output pad | 1.5/1.4 | 1.5/1.4 | | | |
| Clock input pad | 1.1/0.9 | 2.6/2.3 | | | |
| FF clk to output | 1.2/1.3 | 3.8/3.6 | | | |
| 2:1 mux | .33/.34 | 4.13/3.94 | | | |
| Data output pad | 1.5/1.4 | 5.63/5.34 | | | |
| Data input pad | .50/.35 | 6.13/5.69 | | | |
| Data FF setup | 0.28 | 6.41/5.97 | | | |
| Total | | 6.41/5.97 | | | |
| <p>Conclusion: Using 0.6 micron technology (LSI 0.6u) these calculations produced a cumulative timing in excess of 10nS, or the entire clock period. Therefore, a lower performance technology (larger than 0.35u) probably cannot be used. However, requiring a more advanced technology for the S800 parts seems a reasonable tradeoff.</p> | | | | | |

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S800 PC brd signal distribution.

What about reflections?

A 2 cm trace length with no vias can be maintained if the pinout has the following order on both the PHY and the link:

ground - data - ground - clock - ground

A 2 cm trace wavelength corresponds roughly to a 15 GHz signal, or is an eighth wavelength antenna for a 2.5 GHz signal.

2.5 GHz is the 25th harmonic of the 100 MHz fundamental created by the changing data.

Given the fact that the waveforms at this speed are expected to be rounded off (I.e. approaching sinusoidal) there should be virtually no energy left by the 10th harmonic, let alone the 25th.

Therefore, emission *should* be able to be well controlled. (Although this needs to be verified in a lab environment by a volunteer).

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Other requirements:

In order to have a cost effective solution thru S800, ideally:

1. The databus width should remain at 8-bits, due to the PHY being pad-limited and costs rising significantly with gatecount.
2. The new protocol should retain compatibility with older PHYS/links:
 - 2b. No change from TTL pads should be made.
 - 2c. No clock frequency higher than 50MHz
3. Due to the need for low trace capacitance, length and clean EMI characteristics, a matching pad layout on both the PHY and link needs to be specified.

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Conclusions:

Assuming:

1. A suitably fast technology.
2. Fixed pinout on the PHY and link.
3. 2 cm PHY-link separation.

S800 can be achieved using the dual-edge clocking approach.

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S1600/S3200 Outline

Issues:

1. No technology appears adequate to allowing a PHY sourced clock faster than a dual-edge 50MHz.
2. The dual edge approach will not work if a PHY-link physical separation of $> 2-3$ cm is required, even at S800.
3. The current TTL drivers will be inadequate.

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Therefore:

If wider separations are to be supported, a more sinusoidal, and probably also differential electrical protocol will be required.

A specific recommendation will be presented at the next meeting.

In spite of PHY cost concerns due to pad limiting, a wider databus WILL be required.

In order to manage roundtrip delay, two 16-bit independent buses from both the PHY and link, with ea. sourcing its own clock will probably be necessary.

(Note: this is similar to the approach used by ATM. While too costly for S800, it may be required for S3200).