

1 Beta extension of the 1394a PHY – Link Interface Specification

1.1 Introduction

The beta PHY- Link interface provides the ability to extend the existing 1394a interface (as currently proposed) to support beta mode signaling and features:

1. Retention of the ability to provide isolation.
2. Largely retains the 1394a signaling protocol.
3. Retention of PHY sourced clocking (while routing the clock thru and back as described in section 1.1.2).
4. Retention of the simple speed selection mechanism of 1394-1995, while adding an enhancement which provides ease of board speed upgrades without the need to relay out the PCB.
5. Provides any PHY/link speed combination, including the use of older nonbeta PHYs and links, without the need for software intervention.
6. Increases the pincount by only 10 pins.
7. Uses frequencies which do not exceed 200 MHz (at 3200 baud).
8. Uses low voltage signaling.
9. Is relatively insensitive to latency.
10. Allows for support of relatively large distances between the PHY and Link chips for special applications.

1.2 Interface

The interface shown in Figure 2 shows the electrical interface between the PHY and link chips. The interface is similar to the 1394-1995 interface, except for the following changes:

1. The datapath width has been increased from 8 to 16 bits.
2. There is a return clock (SCLKRtn) from the Link to the PHY which follows data transmitted from the link to the PHY. (Note: as is discussed later in section 1.1.2, this clock is not sourced by the Link, but is, in fact, the PHY clock rebroadcast by the Link which aligns with data being sent from the Link to the PHY.
3. The signaling no longer supports 5-volts, but uses SSTL-3 (although LVTTL may be used in less demanding situations and with which SSTL-3 levels are compatible).

1.1.1 Theory of Ops

Extending the existing S100 – S400 ‘alpha’ interface, the beta interface continues the practice of increasing the width of the databus by a factor of 2 for every increment in speed one more step, to 16-bits at S800. At frequencies above S800, rather than increase the width of the data, the frequency of the clock sourced from the PHY increases by a factor of 2 for every speed increment, to 100 MHz at S1600 and 200 MHz at S3200. In this way, both manageable pincounts and frequencies can be achieved.

1.1.2 Clocking

Beta mode clocking is an extension of the existing PHY sourced clocking used in 1394-1995 and 1394a. There is no change to the clock distribution from the PHY to the link. However, with reference to figure 1, inside the link the following occurs:

1. The PHY clock is buffered and used as the internal clock source for the link.
2. At higher operating frequencies, if req'd, a delay element which tracks the link chips variations in voltage, temperature and process is inserted into the clock path before it is rebroadcast.
3. The clock is rebroadcast along with the data back to the PHY.

Note: If the clock output pad is not the same type as the data/control output pads, care must be exercised to ensure that the clock does not get ahead of the data. This can be accomplished by factoring the delay into the value selected for the delay element referred to above.

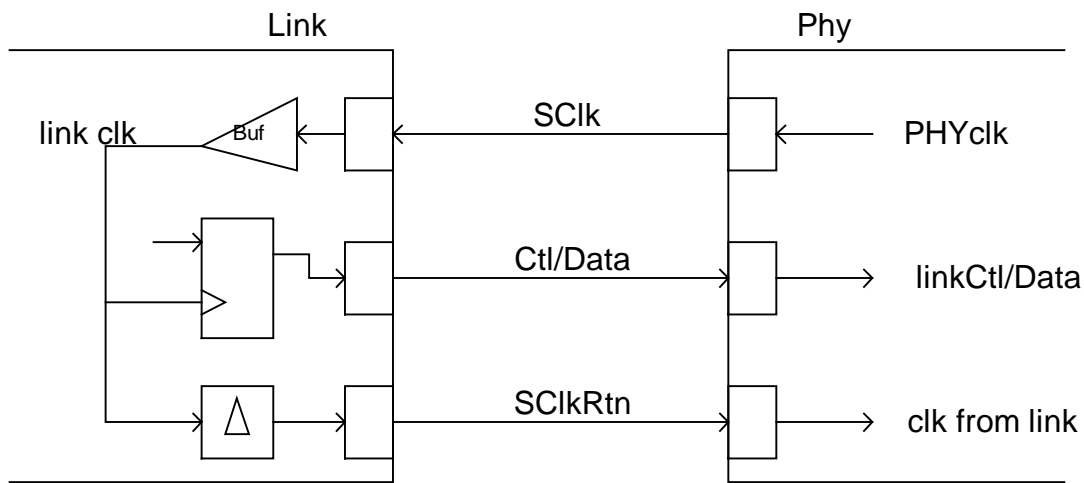


Figure 1

1.1.3 Interface Frequency Selection

The PHY clocks internally at (a minimum of) the highest interface frequency it is capable of supporting. As shown in Figure 2, the existing 'CLK25' 1394-1995 link signal has been replaced by 2 'infcClkSel' pins. In addition, these pins are present on both the PHY and the link, rather than just on the link as previously was the case.

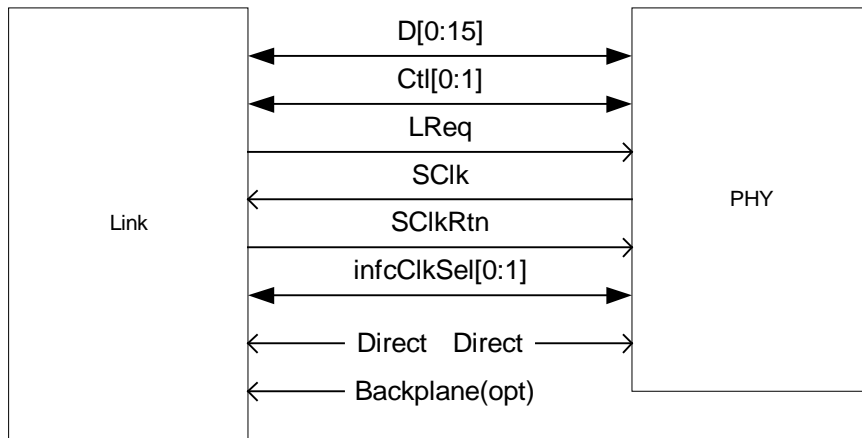


Figure 2

When bringing together a PHY and a Link of differing performance capabilities, the clock frequency is selected from the maximum speed of the slower of the two devices, based on the values shown in Table 1. Independent of its internal operating frequency, the PHY will transmit a clock and data rate corresponding to the current setting of `infcClkSel`. Similarly, the link will accept a clock of the frequency selected.

In the event that one chip is connected to another which is not beta capable, it is informed of this by `infcClkSel = 2'b00`.

<code>infcClkSel [1:0]</code>	Interface clock speed
2'b00	50 MHz, alpha interface
2'b01	50 MHz, beta interface
2'b10	100 MHz
2'b11	200 MHz

Table 1

Example 1: A link capable of operation at S1600 is attached to an early version S400 beta PHY in anticipation of higher frequency PHYs to come. `infcClkSel` is set to 2'b01. The S400 PHY simply operates at its design capabilities. The S1600 Link sets its interface to operate at a 50MHz clock rate, even though it may be capable of clocking at a higher rate internally.

Example 1a: A board manufacturer currently using chips with the same capability as in example, is now able to obtain S800 beta-PHYs and wishes to upgrade his production. No change in the clock frequency or of the PC board(`infcClkSel` setting) are necessary, and system software handles the increase in capability of the PHY to transmit S800 data.

Example 2: An S3200 PHY wishes to talk to an S1600 link. The common clock frequency is 100 MHz. `infcClkSel` is set to 100MHz(2'b10). The PHY adjusts its output clock and data rate to the link to 100 MHz. The link simply notes that it can run at its maximum capabilities.

(Admittedly extreme) Example 3: An older S400 *alpha* link is attached to an S3200 capable PHY. `infcClkSel` is set to 2'b00 on the PHY only. The S3200 PHY operates at 50MHz. The alpha link operates its interface at 50MHz, with its non-beta Clk25 pin pulled high. The 3200 PHY, knowing that it is communicating with an alpha link, may choose to bypass the asynchronous interface and operate synchronously as an alpha PHY would.

1.3 Isolation

The data and clock sent from the link to the PHY are, for all intents and purposes, asynchronous to the PHY clock, and need to be resynchronized to the PHY's clock domain. Therefore, as the interface is relatively latency insensitive by definition, isolation may be used providing that it is capable of passing the minimum pulse widths corresponding to the highest supported frequency of operation for a given link-PHY pair.

Recommendation: In order for total interface delays to remain within a manageable window, it is recommended that the maximum insertion delay of the isolation circuit not exceed 3 nS.

Requirement: The uniformity of the pin-pin delays of the isolation circuit must be such that under no circumstances the clock signal will propagate thru the isolation circuit such that it arrives after the data.

1.4 Roundtrip delay

The use of an asynchronous interface makes the interface relatively insensitive to roundtrip delay. However, as shown in Figure 3, an asynchronous FIFO should be used in the PHY in order to ensure that the individual data bits received arrive at the same time, and is therefore insensitive to the data alignment issues which would occur using FFs alone, due to metastability which could cause data to arrive on different clock edges. The use of an asynchronous FIFO will ensure that all data remains aligned with the same bit-cell.

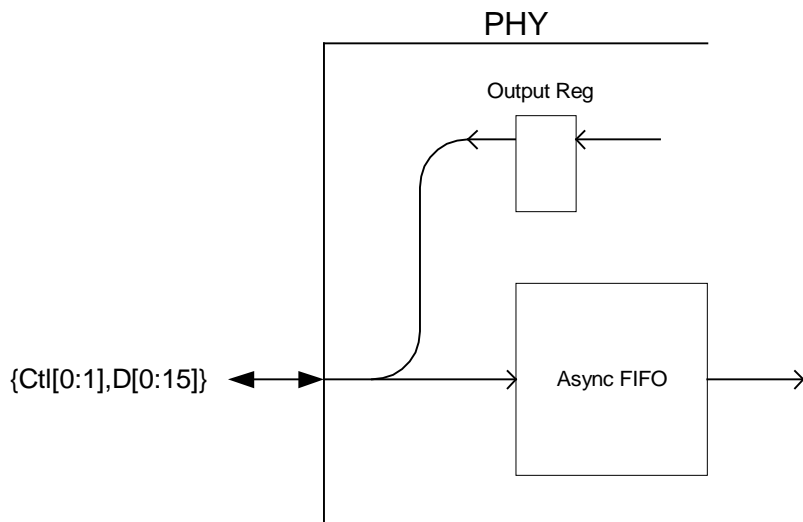


Figure 3

1.1.4 Recommendation Against Synchronous Operation of Beta Devices

It is strongly recommended against attempting to tune logic speed in order to obtain synchronous operation. While this is theoretically possible, it would require control over both the link and PHY designs, and presumably therefore imply the necessity of using parts in matched pairs only.

Note: Process variation alone between the two would likely make this feat impossible.

1.5 Pin Ordering

At 100 and 200 MHz, it is recommended that the clock and data pin ordering shown in Figure 4 be followed.

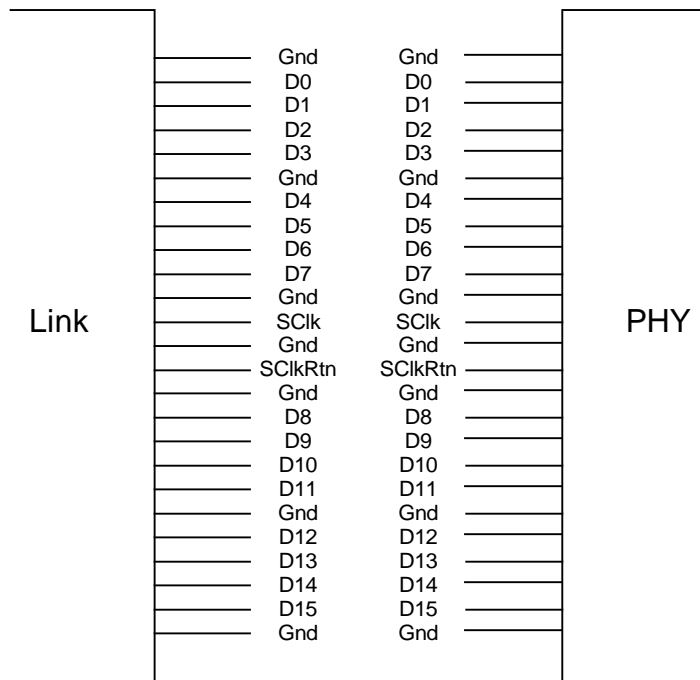


Figure 4

1.6 Electrical Interface

Requirement: Devices capable of operation at S1600 or above, shall implement the interface data, control and clock lines with signalling levels and properties in compliance with the SSTL-3 standard (EIA/JEDEC standard number 8-8).

Recommendation: Devices not capable of operation exceeding S800, shall have the option of implementing an interface either in compliance with SSTL-3, or using LVTTTL signalling levels.

1.7 Signaling Protocol

1.1.5 Receive

The 1394a protocol is used without modification.

1.1.6 Transmit

The 1394a protocol is used without modification.

Note: The asynchronous nature of the interface plus the possible addition of a FIFO in the PHY to receive data from the link presents a delay between the PHY turning over the bus to the link which is, in effect, a random number of added bit cells inserted between the initiation of link control of the bus, and the start of data. Therefore, beta PHYs are required to assume that during this interval, the link is, in effect, sending a link control code of 2'b01 (hold), and act accordingly.