

12 PHY – Link Interface

Introduction

The beta PHY- Link interface provides the ability to support beta mode signaling and features:

1. The ability to provide isolation.
2. Largely retains the 1394 signaling protocol.
3. Retains PHY sourced clocking (while routing the clock thru and back as described in section xxx.)
4. Retains the simple speed selection mechanism of 1394-1995, while adding an enhancement to S1600 and S3200 parts which provides ease of board speed upgrades without the need to relay out the PCB.
5. Increases the pincount by a max. of only 10 pins.
6. Uses frequencies which do not exceed 200 MHz (at 3200 baud).
7. Uses LVTTTL compatible low voltage signaling.
8. Is relatively insensitive to latency.
9. Allows for support of relatively large distances between the PHY and link chips for special applications.

Interface

The interface shown in Figure 1 shows the electrical interface between the PHY and link chips. The interface is similar to the 1394-1995 interface, except for the following changes:

1. The datapath width increases from 8 to 16 bits at S800 and above.
2. There is a return clock (SClkRtn) from the Link to the PHY, implemented on S1600 and S3200 devices, which follows the data transmitted from the Link to the PHY. (Note: as is discussed later in section tbd, this clock is not sourced by the Link, but is, in fact, the PHY clock rebroadcast by the Link which aligns with data being sent from the Link to the PHY).
3. The signaling no longer supports 5-volts, but uses SSTL-3 (although LVTTTL may be used in less demanding situations and with which SSTL-3 levels are compatible).

12.1.1 Theory of Ops

Extending the existing S100 – S400 ‘alpha’ interface, the beta interface continues the practice of increasing the width of the databus by a factor of 2 for every increment in speed, up to 16-bits at S800. At frequencies above S800, rather than increase the width of the data, the frequency of the clock sourced from the PHY increases by a factor of 2 for every speed increment, to 100 MHz at S1600 and 200 MHz at S3200. In this way, both manageable pincounts and frequencies can be achieved.

Interface Frequency Selection

The PHY clocks internally at (a minimum of) the highest interface frequency it is capable of supporting. As shown in figure Figure 1, the existing ‘CLK25’ 1394-1995 link signal has been replaced by 2 ‘infcClkSel’ pins for devices capable of S1600

or S3200 operation only. Similarly, the SClkRtn signal is only present on devices capable of S1600 or S3200 operational speeds.

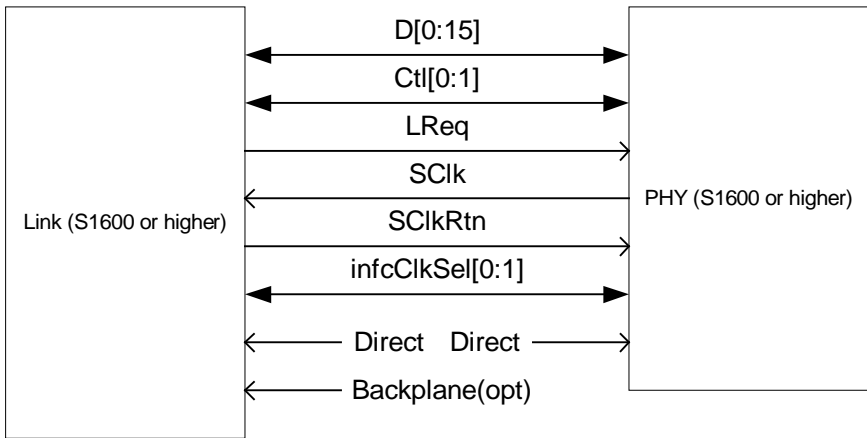


Figure 1

When bringing together a PHY and a Link of differing performance capabilities, the maximum speed of the slower of the two devices is selected for the clock frequency, based on the values shown in Table 1. Independent from its internal operating frequency, the PHY will transmit a clock and data rate corresponding to the current setting of infcClkSel. Similarly, the link will accept a clock of the frequency selected.

In the event that one chip is connected to another which is not beta capable, it is informed of this by infcClkSel = 2'b00. This does not apply when one or more devices are used which are limited to S800 operation.

A PHY which is connected to either an alpha link, or one capable of no greater than S800, will not use the SClkRtn signal, and will bypass the asynchronous interface.

A S1600 or S3200 capable PHY or link which is connected to either an alpha device, or one not capable of greater than S800 operation, will have its infcClkSel lines tied to 2'b00. The previous reference to a code 2'b01 has been deleted.

InfcClkSel [1:0]	Interface clock speed
2'b00	50 MHz, alpha interface
2'b01	reserved
2'b10	100 MHz
2'b11	200 MHz

Table 1

Example 1: A link capable of operation at S1600 is attached to an early version S400 beta-PHY in anticipation of higher frequency PHYs to come. InfcClkSel is set to 2'b00. The S400 PHY simply operates at its design capabilities. The S1600 Link sets its interface to operate at a 50MHz clock rate, even though it may clock at a higher rate internally. SClkRtn is not used, but should be present on the PC board to allow for future upgrades.

Example 1a: A board manufacturer is now able to obtain S800 beta-PHYs and wishes to upgrade his production. No change in the clock frequency or of the PC board are necessary, and software handles the increase in capability of the PHY to transmit 16-bit data.

Example 2: An S3200 PHY wishes to talk to an S1600 link. The common clock frequency is 100 MHz. InfcClkSel is set to 2'b10. The PHY adjusts its output clock and data rate to the link to 100 MHz. The link simply notes that it can run at its maximum capabilities.

(Admittedly extreme) Example 3: An older S400 *alpha* link is attached to an S3200 capable PHY. InfcClkSel is set to 2'b00 on the PHY only. The S3200 PHY operates at 50MHz. The alpha link operates its interface at 50MHz, with the non-beta Clk25 pin pulled high. The 3200 PHY, knowing that it is communicating with an alpha link, may choose to bypass the asynchronous interface and operate synchronously as an alpha PHY would.

12.1.2 Isolation

12.1.3 The data and clock sent from a link to a PHY are, for all intents and purposes, asynchronous to the PHY clock, and need to be resynchronized to the PHYs clock domain. Therefore, as the interface is relatively latency insensitive by definition, isolation may be used providing that it is capable of passing the minimum pulse widths which are present at the highest supported frequencies of operation of a given link-PHY pair.

12.1.4

12.1.5 Recommendation: In order for total interface delays to remain within a manageable window, it is recommended that the maximum insertion delay of the isolation circuit not exceed 3 nS.

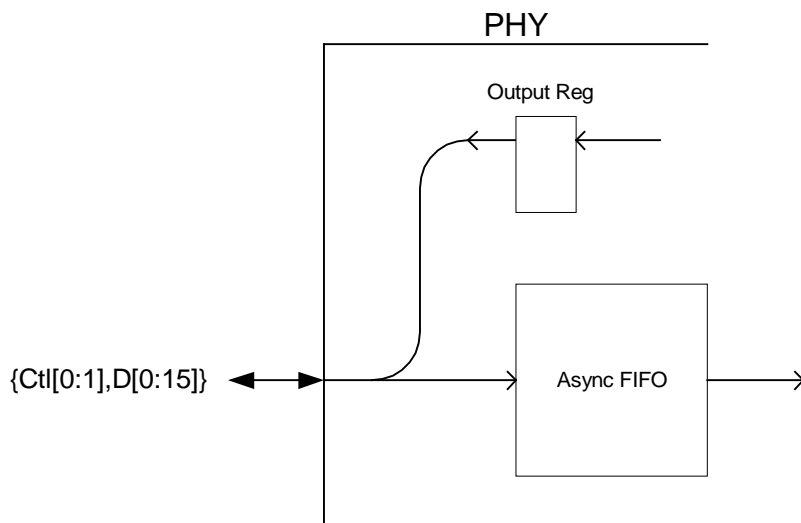
12.1.6

12.1.7 Requirement: The uniformity of the pin-pin delays of the isolation circuit must be such that under no circumstances the clock signal will propagate thru the isolation circuit such that it arrives after the data.

12.1.8 Roundtrip delay

12.1.9 The use of an asynchronous interface makes the interface relatively insensitive to roundtrip delay. However, as shown in Figure 2, an asynchronous FIFO should be used in the PHY in order to ensure that the data received arrives at the same time, and is insensitive to the data alignment issues which would occur using FFs alone, and the metastability which could cause data to arrive on subsequent clock edges. This will ensure that the all data remains aligned with the same bit-cell.

12.1.10



12.1.11

Figure 2

12.1.12 Recommendation Against Synchronous Operation of Beta Devices

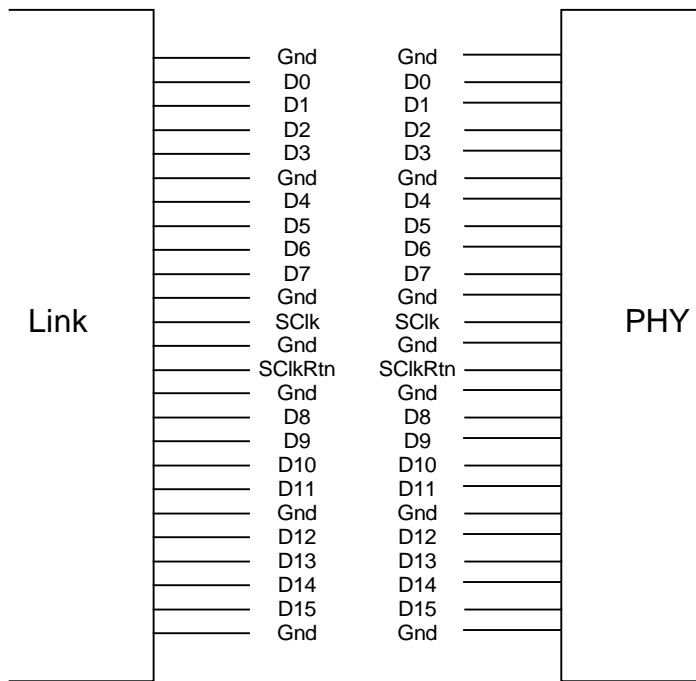
12.1.13 It is strongly recommended against attempting to tune logic speed in order to obtain synchronous operation. While this is theoretically possible, it would require control over both the link and PHY designs, and presumably therefore imply the necessity of using parts in a matched pair only.

12.1.14

12.1.15 Pin Ordering

12.1.16 At 100 and 200 MHz, it is recommended that the clock and data pin ordering shown in Figure 3 be followed. Note: as previously stated, if it is important to allow for upgrades, relative pin positions should be maintained, even if not used in lower capability devices.

12.1.17



12.1.18

Figure 3

12.1.19 Electrical Interface

Requirement: Devices capable of operation at S1600 or above, shall implement the interface in compliance with the SSTL-3 standard (EIA/JEDEC standard number 8-8).

Recommendation: Devices incapable of operation not exceeding S800, shall have the option of implementing an interface either in compliance with SSTL-3, or using LVTTL signalling levels.

12.1.20 Signaling Protocol

Receive

The 1394a protocol is used without modification.

Transmit

The 1394a protocol is used without modification.

Note: The asynchronous nature of the interface plus the possible addition of a fifo in the PHY to receive data from the link presents a delay between the PHY turning over the bus to the link which is, in effect, a random number of added bit cells inserted between the initiation of link control of the bus, and the start of data. Therefore, beta PHYs are required to assume that during this interval, that the link is, in effect, sending a link control code of 2'b01 (hold), and act accordingly.

12.1.21 PHY-link Bit Width Table

12.1.22

12.1.23 The following table shows the number of bits of the PHY-link databus which are used for operation at different speeds and clock rates. One should make special note of the combination of an S3200 interface speed with an S100 bus speed.

12.1.24

Interface Top Speed	Bus Speed	Bit Width
S400 (50 MHz)	S100	2
	S200	4
	S400	8
S800 (50 MHz)	S100	2
	S200	4
	S400	8
	S800	16
S1600 (100 MHz)	S100	1
	S200	2
	S400	4
	S800	8
	S1600	16
S3200 (200 MHz)	S100	1 (held for 2 clocks)
	S200	1
	S400	2
	S800	4
	S1600	8
	S3200	16