

PHY-link Taskforce

Santa Cruz

February 10, 1998

PHY-link Taskforce

■ Recap

- Initial draft of PHY-link spec presented in FL and added to Draft 0.071 of the 'b' spec.
- Presentation/questions from FL meeting and new/other issues were discussed for 8 weeks following FL meeting.
- New draft posted to ftp site 1/30

PHY-link Taskforce

I Brief review of the Initial Draft:

The initial phy-link interface draft:

- I Retained capability for isolation
- I Largely retained 1394a signal protocol
- I Retained PHY sourced clocking
- I Retained existing speed selection mechanism
- I Increased pincount by no more than 10 pins (8/10 for data)

PHY-link Taskforce

- Initial draft (continued)
 - Maintained or increased existing timing margins.
 - Increase width to 16-bits at S800, then increase clock at S1600 and S3200
 - Used low-voltage signaling.
 - Allowed PHY-link physical separation sufficient to support DeviceBay
 - Relatively latency insensitive.

PHY-link Taskforce

New Draft

- The new draft is a refinement of the original reflecting an incremental examination of issues raised since the original draft was published.

PHY-link Taskforce

Issues resolved since the original draft:

- 1. Do we need SClkRtn at S800?
- No. New draft changed to presence of SClkRtn to S1600 and S3200 operation only.
- The effect of adding greater PHY-link separations on the margin was examined and found not to violate design margins.
- Presence/absence of SClkRtn is supported by the clk select pin mechanism previously proposed.

PHY-link Taskforce

Elimination of SClkRtn at S800 essentially creates 16-bit alpha interface at S800, beta at 1600+.

PHY-link Taskforce

- 2. Is Lreq fast enough at 50 MHz?
- Resolved: No . Lreq needs to clock at the same rate as SCLKRtn (or just SCLK at S800).

PHY-link Taskforce

- 3. Does the new interface have any effect on the use of repeaters?
- No.

PHY-link Taskforce

- 4. Should Clk recovery be used instead of SClkRtn:
 - No.
 - Note: Significant resistance to use of PLLs.
 - No compelling need identified.

PHY-link Taskforce

5. At the ad hoc meeting held in FL, a request for reconsideration was made to revisit the groups standing recommendation for a 16-bit/50 MHz interface in favor of an 8-bit 100 MHz one. In FL the limited number of members of the group present were roughly evenly split regarding reopening the issue.

Policy: to reopen an issue, a majority of the taskforce reflector members must vote in favor of reconsideration.

Upon presentation to the taskforce reflector, literally no support for 8-bit/100 MHz was presented or voted in favor of, so the matter was closed.

PHY-link Taskforce

- 6. Is a change to an LVTTTL interface really necessary?
 - Yes. Timing analysis contributed on the reflector showed that:
 - | A. Adequate timing margins require the use of LV technology.
 - | B. PCI bus (the current driver of the requirement for 5V compatibility) cannot support beta data rates in any event.

PHY-link Taskforce

As of today:

The initial draft has been posted for 8 wks and ample opportunity for discussion has been given.

The revised draft addresses all subsequent issues to date.

The current workload no longer warrants the existence of a formal taskforce.

PHY-link Taskforce

**We think we are done and
any remaining issues are
easily handled within the
committee proper.**