P1394b PHY-Link Interface Requirements

(A document describing proposals for discussion
at the Portland, Oregon meeting of the P1394b Committee,
August 18 & 19, 1998)

Seán Killeen, SSL - Co-Chair & Editor of the P1394b PHY-Link Task Group

1.0 Introduction & Scope

The purpose of this document is to present a set of requirements for the P1394b PHY-Link interface. This set of requirements is put forward as a proposal and is open for discussion at all levels. Active discussion and debate is requested in order to agree on the final set of interface requirements. This will then facilitate the creation of an interface specification that will meet the technical and industry requirements.

2.0 Interface Description

The P1394b PHY-Link interface provides a mechanism for data and control information to be exchanged between 1394 PHY & Link devices that adhere to the specifications. It is a point-to-point interface between two devices only. The interface provides a reliable mechanism of transfer of 1394 packet information between the two devices. It also provides mechanisms for other information, not related to 1394 packets, to be exchanged by the devices.

3.0 Interface Requirements

The following are a set of requirements that may be desirable for a P1394b PHY-Link interface specification. A brief description of each point is presented. These are not presented in any particular order or priority.

3.1 Data Transfer Rate

The P1394b PHY-Link interface specification must provide for a mechanism to transfer data between the PHY & Link devices at the S100, S200, S400, S800, S1600 & S3200 speeds. This data transfer is bi-directional in nature.

It is desirable that a consistency of approach be adopted in the specification across this speed range in order to promote the principle of design re-use.

It is desirable that a natural progression be available to extend this specification to higher speeds in the future.

3.2 Logical Pinout

It is desirable that the pinout requirements of the PHY-Link interface be minimised, without affecting the overall system reliability, in order to minimise overall device costs.

The interface pinout should be capable of supporting the necessary data and control transfer bandwidth as well as providing sufficient flow control mechanisms to enable the interface to operate effectively in the application.

The interface pinout should provide a measure of signalling bandwidth overhead, which will be unassigned (but reserved) by the specification, in order to allow extensions to cater for future and as yet unforeseen requirements.

3.3 Signalling Method

The signalling method should be compatible with the design goals of

- Realisable in low-cost silicon fabrication processes which are commercially available
- Provides sufficient reliability of operation to maintain an interface BER of <tbd>
- Provides for design migration from one generation to the next of device supply voltage

3.4 Clocking Scheme

The clocking scheme should provide for the safe and reliable transfer of information from one device to the other. Sufficient clock information should be provided to allow the transmitted data signals from one device to be received accurately.

A source synchronous clocking scheme, where each source/transmitting device provides a clock signal to accompany its synchronously transmitted data, provides a good mechanism to provide for safe & reliable transfer of data and control information.

Other schemes are possible and can be considered.

3.5 Transfer Types

The transfer types supported by the P1394b PHY-Link interface should be modelled on the transfer types supported by the P1394a PHY-Link interface.

The P1394a information transfer types are:

- Link Request - Link makes a request of a service from the PHY device
- Link Transmit - Link sends 1394 packet information to the PHY device for transmission
- Link Receive - Link receives 1394 packet information from the PHY device (from the 1394 bus)
- PHY Status - PHY issues status information (not packet data)

Similar transfer mechanisms should be provided by the P1394b PHY-Link interface, including any necessary extensions to allow for new Link Request types etc.

There may be other transfer mechanisms required of the P1394b PHY-Link interface. In particular, it may be desirable to include the following transfer types:

- Link Information Transmit - Link transmits broad bandwidth non-packet information to the PHY
- Link Information Receive - Link receives broad bandwidth non-packet information from the PHY

These transfer types should be defined in such a manner as to provide simple extension for future use.

There are currently no defined applications for transfer types of these types, although it is possible that future applications may require these types of information transfer.

A flexible and extendible information transfer mechanism between the two devices may avoid the necessity for future revision of the PHY-Link interface to add relatively simple features.

Other transfer types may be desirable and can be considered.

3.6 Control Information Transfer Rate

Currently the P1394a PHY-Link interface defines a 200 Mbit/sec control channel between the PHY and link devices.

It may be desirable to increase the bandwidth of this control channel as the data rate increases beyond the S400 data rate.

(This could be done by increasing the pin count allocated to the control interface, by increasing the logical information content of the signals carried over the current pin count (by using prior context) or by increasing the raw transfer rate of information transfer over the available pins)

It may be desirable to maintain a constant control channel transfer rate for the PHY-Link interface regardless of the actual (current) data transfer rate.

A constant control channel transfer rate may simplify the design of the control logic required to maintain coherency on both sides of the interface.

3.7 Flow Control Mechanisms

Flow control mechanisms handle the efficient transfer of ownership from one device to the other in a manner that is suitable for the application usage of the interface. Considerations for the choice of flow control mechanism for the P1394b PHY-Link interface should include:

- Frequency of transfer of ownership
- Optimization for ‘most common’ owner
- Latency of transfer of ownership (buffering concerns etc.)
- Interruptability & resumability of flow control mechanisms

Other considerations may be desirable and can be considered.

3.8 Compatibility Models

A new definition of the PHY-Link interface should draw the best elements from the work that has gone before.

It may be desirable not to constrain the P1394b PHY-Link interface to be directly backwards compatible with the P1394a PHY-Link interface. Such backwards compatibility may not provide any lasting benefits to products designed to use either interface, and will certainly hamper the free selection of the best engineering solution to the requirements of the P1394b PHY-Link interface.

The compatibility models to be considered are:

- P1394b Link connected to P1394b PHY - required mode of operation
- P1394a Link connected to P1394b PHY - desirable mode of operation?
- P1394b Link connected to P1394a PHY - desirable mode of operation?

The principle of additional cost for additional usable features should apply to consideration of the required/ mandated/specified modes of operation. The utility of directly connecting P1394a PHY/Link devices to P1394b PHY/Link devices needs to be well justified to warrant additional specification work which will necessitate additional design work and silicon cost.

3.9 Discovery

It may be desirable for the P1394b PHY-Link interface to specify a means for the Link device to discover attributes of the PHY device to which it is connected. The only attribute currently defined is the 1394 Node ID which is issued by the PHY at bus initialisation.

There may be other attributes that would warrant definition in a PHY-Link interface specification.

It may be desirable to define a generic ‘discovery’ mechanism to allow future attributes to be discovered, either in an active or passive manner.

3.10 Extendability & Flexibility

It may be desirable to include provisions in the P1394b PHY-Link interface to allow the utility of the interface to be easily extended in the future. Such extensions may include:

- Additional data transfer rates
- Additional control transfer rates
- Additional transfer types
- Additional flow control mechanisms
- etc.

It should be recognised that the addition of extra flexibility to the specification will generally increase the cost of any implementation by some amount. This additional cost may be justified if the interface definition can be easily adapted to support new functionality or features without a major re-structuring in the future.

3.11 Power Consumption & Noise

It may be desirable to analyse the power profile of the P1394b PHY-Link interface during common usage in order to minimise signal transitions to reduce power consumption.

It may be desirable to analyse the characteristics of the signalling scheme in order to minimise the potential for noise/cross-coupling/ISI/ground-bounce and any other negative attribute.

3.12 Isolation Mechanisms

It may be desirable to define a closely specified isolation mechanism to allow the PHY and Link devices to operate from completely separate or partially separate power supplies.

The PHY-Link interface should specify the required characteristics of such an isolation scheme.

3.13 PHY Buffering & Bus Ownership

<TBD>

3.14 Interface Timing

<TBD>

3.15 Error Handling

<TBD>

3.16 Initialization & Reset

<TBD>

3.17 PHY Register Map

<TBD>

4.0 Other Protocol Issues

<TBD>

5.0 Other Signalling Issues

<TBD>

6.0 Miscellaneous Issues

<TBD>

7.0 Call to Action/Schedule for Completion

The success of the P1394 PHY-Link interface definition process depends heavily on the practical support of a number of people, willing to take sections of the interface and work the associated issues.

I will take responsibility for separating out individual sections that can be worked on in relative isolation and for collating the resulting conclusions and recommendations.

This process of dividing and actually doing the detailed specification work can only practically commence once the large scale decisions are made on the infrastructure that the P1394b PHY-Link interface will provide.

It would be appreciated if the people who can actively contribute to this interface definition process would make themselves known to me in order that I can determine the best fit of people to requirements.

I anticipate that a first draft of a new P1394 PHY-Link interface section should be ready for the September meeting in the Chicago area. This will be a very preliminary draft, outlining the main direction of the interface definition. To enable this goal to be met, definite decisions need to be made regarding the interface fundamentals. This decision making process will be discussed at the August meeting in Portland and a mechanism agreed upon to allow strong progress to be made.

Any comments, queries or suggestions should be addressed to:

Seán Killeen,
SSL Dublin,
32-34 Harcourt Street,
Dublin 2,
IRELAND

Tel.: +353-1-402-5700
Fax: +353-1-402-5711
Email: sean.killeen@ssl.ie