

Proposal for a P1394b PHY-Link Interface

The purpose of this document is to provide a proposal for a P1394b PHY-Link interface. This interface is to serve as a single point-to-point contact between a PHY device/chip and a Link device/chip. The features of this interface are as follows:

- provides for bi-directional data transfer at 800 & 1600 Mbps
- 'owned' by the PHY device, but provides defined handover mechanisms
- defines a continuous bi-directional control path for low latency responses & actions
- includes some extendability to allow as-yet-unforeseen functionality to be added in a backwards-compatible fashion
- provides mechanism(s) to allow extension to higher data transfer speeds
- uses simple source synchronous clocking - no advanced data capture mechanisms
- implementable in cost-effective, commercially available CMOS silicon technology
- interface clock rate at binary multiples of 100 MHz
- choice of faster/wider for speeds in excess of S800 - see tables later
- supports an optional isolation barrier between the PHY & Link devices
- Control lines run at the same rate as their respective source clock (simple scheme)
- PHY & Link source clocks run at the same frequency - 100 or 200 MHz

General Interface Description

This description of a PHY-Link interface operates as follows.....

The interface operates as a symmetrical version of the P1394a interface, with some signals being redefined to make their usage more generic and extendible. This interface provides mechanisms for the PHY and Link devices to operate more as peers than as master-slave, although at any one time, a master-slave relationship is in place. Both devices have the facility to request services of the other as well as interrupt the other during the execution of those services. The details of the interaction protocols outline which types of requests and interrupts are valid and the times at which they are valid.

The interface supports a variety of data transfer rates. A mandatory set of signals supports S100-S800 using data clocked only with respect to the rising edge of the source clock, running at 100 MHz. This mode of operation is defined as 'base-mode' and must be supported by all devices using this interface.

In order to support higher data rates, the following techniques are used:

- Datapath widening - valid datapath widths of 16 & 32 bits are defined
- Double-edge clocking - clocking of data with respect to the falling edge of the source clock is defined

- Fast Interface Clocking - clocking the interface at 200 MHz is defined

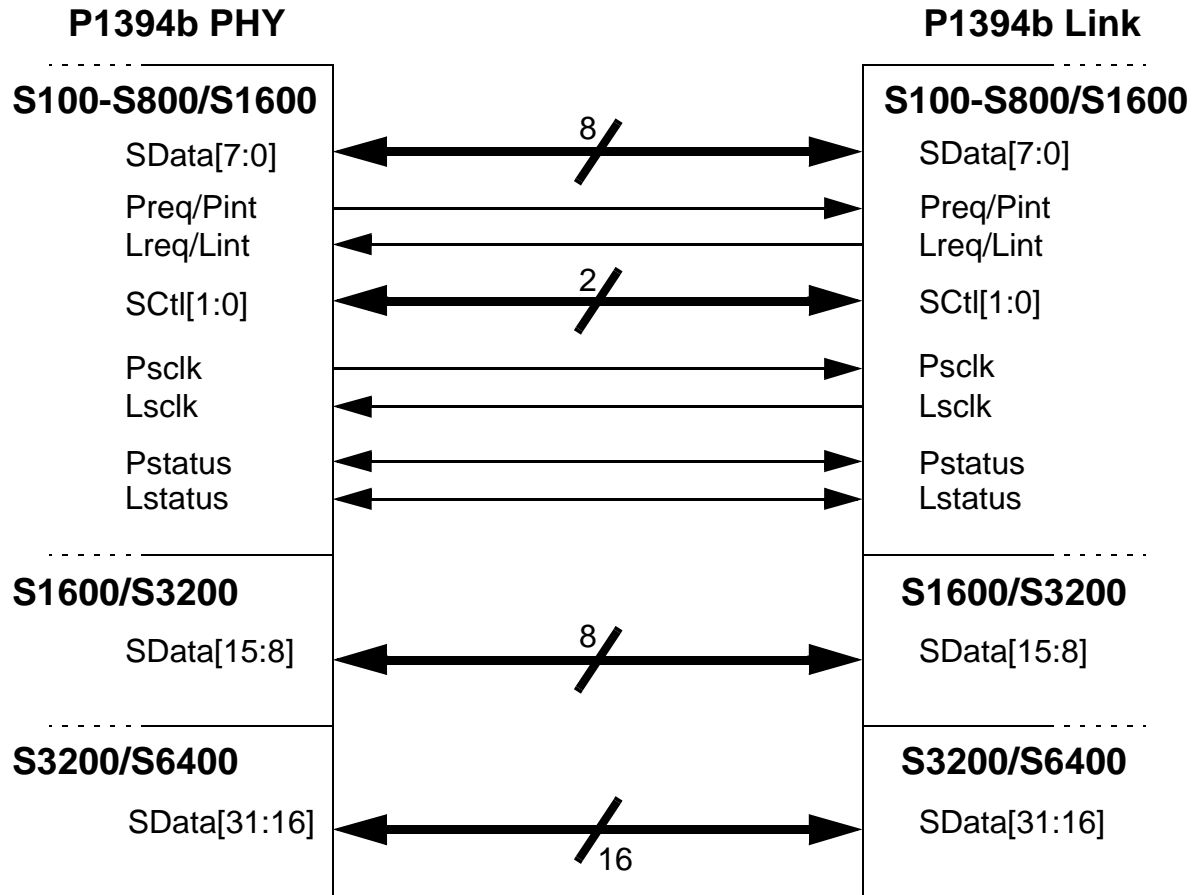
Mechanisms & protocols to make use of these extension schemes are defined in later sections. Note that it is not anticipated that devices which support a certain data transfer rate will support all of the alternative mechanisms to realise that data transfer rate. These modes are defined in order that full flexibility of interface width vs interface speed be accommodated both for discrete and integrated applications without the necessity for advanced data/clock recovery hardware with the additional cost which would ensue. This specification also provides a discovery mechanism to allow Link & PHY devices to be aware of which modes of transfer and transfer rates are supported by both devices.

Datapath Width (bits)	Interface Clock Speed (MHz)	Single/Double Edge Clocking	Data Transfer Rate (Mbps)	Data Transfer Name (Speed - Bits:1/200:Single/Double)
8	100	Single	800	S800 (8-1-S) - Base Mode
8	100	Double	1600	S1600 (8-1-D)
8	200	Single	1600	S1600 (8-2-S)
8	200	Double	3200	S3200 (8-2-D)
16	100	Single	1600	S1600 (16-1-S)
16	100	Double	3200	S3200 (16-1-D)
16	200	Single	3200	S3200 (16-2-S)
16	200	Double	6400	S6400 (16-2-D)
32	100	Single	3200	S3200 (32-1-S)
32	100	Double	6400	S6400 (32-1-D)
32	200	Single	6400	S6400 (32-2-S)
32	200	Double	12800	S12800 (32-2-D)

Table 1: PHY-Link Data Transfer rates

The similarity of this definition of the PHY-Link interface and the existing P1394a interface should allow P1394a Link devices to intercommunicate with P1394b PHYs. The restrictions on the P1394b functions that result from this type of connection are not fully understood at this time. It may not be necessary for all P1394b PHY devices to support this type of connection.

Proposed Interface Pinout



Signal Description

Signal Name	Driver	Signal Description
Basic Signalling for S100-S800 (S1600, S3200 also possible) - Base Mode		
Sdata[7:0]	Bi-direct	Required 8-bit databus for all P1394b compatible PHY & Link devices for S100-S800 single-edge (S1600 & S3200 rates also possible)
Preqint	PHY	PHY->Link request/interrupt
Lreqint	LINK	Link->PHY request/interrupt
Sctl[1:0]	Bi-direct	Required 2-bit control bus for all P1394b compatible PHY & Link devices
Psclk	PHY	PHY->Link interface serial clock source (this clock runs at 100 MHz after device reset)
Lsclk	LINK	Link->PHY interface serial clock source (this clock runs at 100 MHz after device reset)
Pstatus	Bidirect	PHY status indication signal (other uses anticipated)
Lstatus	Bidirect	LINK status indication signal (other uses anticipated)
Extended Signalling for S100-S1600 (S3200, S6400 also possible) - Extended Mode		
Sdata[15:8]	Bi-direct	Optional 8-bit databus for P1394b compatible PHY & Link devices requiring single-edge S1600 (S3200 & S6400 rates also possible)
Extended Signalling for S100-S3200 (S6400, S12800 also possible) - Super Extended Mode		
Sdata[31:16]	Bi-direct	Optional 8-bit databus for P1394b compatible PHY & Link devices requiring single-edge S3200 (S6400 & S12800 rates also possible)

Table 2: Proposed PHY-Link signal descriptions

Mode	Pins
Base Mode	16
Extended Mode	24

Mode	Pins
Super Extended Mode	40

Table 3: Logical Interface Pin Requirements

Details of Signal Usage

Sdata[7:0]	<p>Serial Data. This 8 bit datapath is used during all data transfer operations, regardless of transfer rate. Base Mode uses all 8 data bits for S100, S200, S400 or S800 data. Padding is achieved by duplicating the data over a number of clock cycles. S1600 & S3200 data transfers are possible in Base Mode using faster clocking or double edges.</p> <p>The PHY device drives Sdata[7:0] after interface reset. During data transfer from PHY to Link, the PHY drives Sdata[7:0]. During data transfer from Link to PHY, the Link drives Sdata[7:0]</p>
Preqint	<p>PHY request / PHY interrupt. The serial data stream on this signal is used by the PHY to directly communicate with the Link device, to request a service of the Link or to interrupt a current interface operation being carried out by the Link</p>
Lreqint	<p>LINK request / LINK interrupt. The serial data stream on this signal is used by the Link to directly communicate with the PHY device, to request a service of the PHY or to interrupt a current interface operation being carried out by the PHY.</p>
Sctl[1:0]	<p>Serial Control. This 2 bit bus, in conjunction with other bus interface signals, indicates the current information transfer phase of the interface, including the direction of transfer</p>
Psclk	<p>PHY serial clock. All information transfer from the PHY to the Link takes place with respect to the rising and falling edges of this clock signal</p>
Lsclk	<p>LINK serial clock. All information transfer from the Link to the PHY takes place with respect to the rising and falling edges of this clock signal</p>
Pstatus	<p>PHY Status. The serial data stream on this signal provides an indication of some status from the PHY. The operation of this signal is not yet defined. This signal is bidirectional and can provide additional context-sensitive bus information on a cycle-by-cycle basis.</p>
Lstatus	<p>LINK Status. The serial data stream on this signal provides an indication of some status from the Link. The operation of this signal is not yet defined. This signal is bidirectional and can provide</p>

additional context-sensitive bus information on a cycle-by-cycle basis.

Sdata[15:8] Serial Data. This optional 8 bit datapath is used for Extended Mode data transfer operations. Extended Mode uses 16 data bits for S100, S200, S400, S800 or S1600 data. S3200 & S6400 data transfers are possible in Extended Mode using faster clocking or double edges.

Sdata[31:16] Serial Data. This additional optional 16 bit datapath is used for Super Extended Mode data transfer operations. Super Extended Mode uses 32 data bits for S100, S200, S400, S800, S1600 or S3200 data. S6400 & S12800 data transfers are possible in Super Extended Mode using faster clocking or double edges.

Sdata[31:16] cannot be added to the PHY-Link interface unless Sdata[15:8] are also implemented.