

12. P1394b PHY – Link interface specification

NOTE : This section is to be viewed as a discussion & proposal document. The contents of this section are under considerable review and comments/criticisms/suggestions are actively sought.

This section specifies the signalling, protocol & electrical characteristics of the PHY-Link interface. The interface is described in isolation from other operational characteristics of either PHY or Link devices. The PHY-Link interface specifies a point-to-point communications mechanism between a single P1394b Link and PHY device for the purpose of transfer of 1394 packet and status information between these two devices.

This interface describes mechanisms to support communication between PHY & Link devices at speeds of S100, S200, S400, S800, S1600 & S3200. For all of these cases, the interface pinout is identical. Variations in data clocking method and clock rate are used to accommodate the higher speeds. Lower speeds are accommodated by data padding.

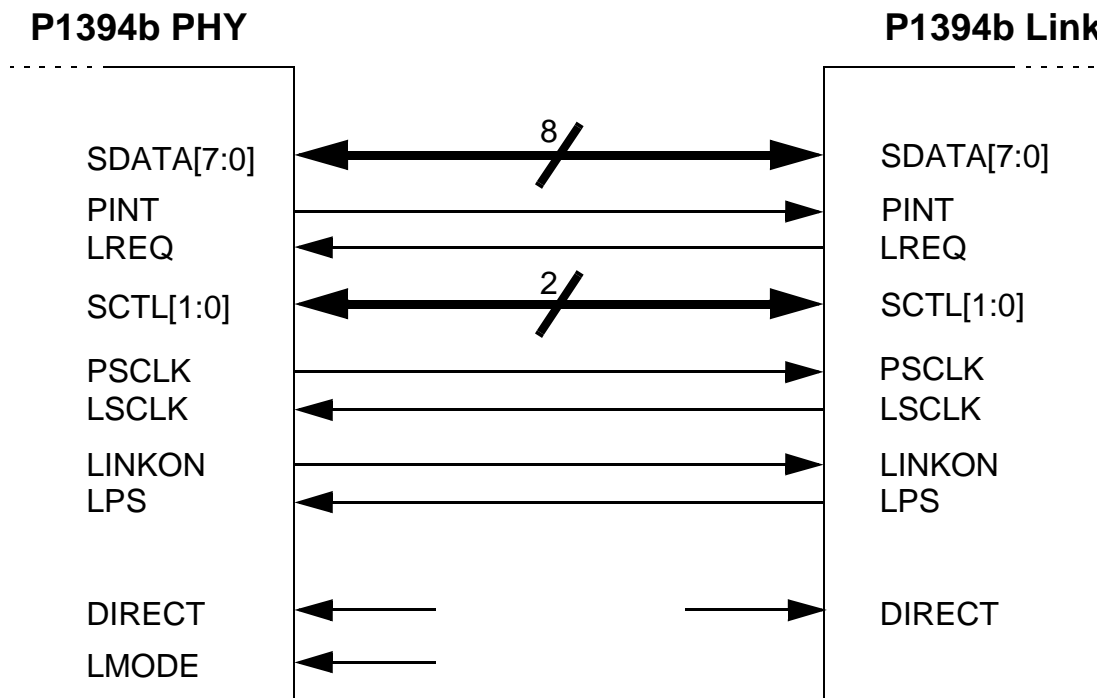
The P1394b PHY-Link interface is an evolution of the interface specified in the IEEE 1394-1995 & associated P1394a standards. The P1394b interface is a superset of the signals defined in those standards, and supports the operation of P1394a-compliant links. In this mode of operation, the complete set of functionality provided by the P1394b PHY will not be available. The purpose of this backwards-compatibility is to provide a migration path for existing P1394a Link applications.

12.1 P1394b PHY-Link Interface Requirements

The following are the requirements which are satisfied by the P1394b PHY-Link interface

- provides for bi-directional 1394 packet data transfer at 100, 200, 400, 800, 1600 & 3200 Mbps
- provides a mechanism for status information transfer from the PHY to the Link
- provides a mechanism for the Link to access a register space within the PHY
- provides a means for the Link to request services from the PHY
- provides a means for the PHY to interrupt the Link during an operation
- supports an optional isolation interface to allow separate PHY & Link device power supply domains

12.2 P1394b PHY to P1394b Link Interface Pinout



12.2.1 Interface Signal Descriptions

The signals of the P1394b PHY-Link interface are divided into mandatory and optional signals.

The mandatory signals are SDATA[7:0], PINT, LREQ, SCTL[1:0], PSCLK & LSCLK. These signals shall be implemented by all PHY & Link devices adhering to this specification.

The optional signals are LINKON, LPS, DIRECT & LMODE. These signals may be implemented by PHY or Link implementations. If they are implemented, their operation shall be as described in this specification.

No other signals are specified to exist between a P1394b PHY & Link device. All other signals as may be implemented fall outside the scope of this standard.

The following table describes the PHY-Link interface signals in brief.

Table 12-1— PHY-Link Interface Signal Descriptions

Signal Name	Direction	Description
SDATA[7:0]	Bidirectional	Serial Data. Mandatory 8-bit databus for all P1394b compatible PHY & Link devices
PINT	PHY Drives	PHY Interrupt. Mandatory PHY to Link interrupt indication
LREQ	Link Drives	Link Request. Mandatory Link to PHY request indication
SCTL[1:0]	Bidirectional	Serial Control. Mandatory 2-bit control bus for all P1394b compatible PHY & Link devices

Table 12-1— PHY-Link Interface Signal Descriptions

Signal Name	Direction	Description
PSCLK	PHY Drives	PHY Serial Clock. Mandatory PHY to Link interface serial clock source
LSCLK	Link Drives	Link Serial Clock. Mandatory Link to PHY interface serial clock source
LINKON	PHY Drives	Link On. Optional PHY indication of a link-on event
LPS	Link Drives	Link Power Status. Optional Link indication of link power status
DIRECT	System Drives	Direct. Optional system indication of the connection type between PHY & Link
LMODE	System Drives	Link Mode. Optional system indication of the PHY-Link interface mode

12.2.1.1 Detailed Signal Descriptions

- SDATA[7:0] - Serial Data. This databus is used to carry 1394 packet data, packet speed & grant type between the PHY and the Link. This is a bidirectional databus. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, data on this bus can be considered to be synchronous to the PSCLK source clock. When driven by the Link device, data on this bus can be considered to be synchronous to the LSCLK source clock.
- PINT - PHY Interrupt. This signal is always driven by the PHY and is valid after *<tb>* serial clock cycles following an interface reset. The serial information on this signal is used by the PHY to transfer status, register, interrupt and other information to the Link. The data on this signal can be considered to be synchronous to the PSCLK source clock.
- LREQ - Link Request. This signal is always driven by the Link and is valid after *<tb>* serial clock cycles following an interface reset. The serial information on this signal is used by the Link to request packet transmission and register/other status information from the PHY, as well as indicating the occurrence of certain Link events that are relevant to the PHY. The data on this signal can be considered to be synchronous to the PSCLK source clock.
- SCTL[1:0] - Serial Control. This is a bidirectional control bus between the PHY and the Link. It is used to indicate the phase of operation of the interface. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, information on this bus can be considered to be synchronous to the PSCLK source clock. When driven by the Link device, information on this bus can be considered to be synchronous to the LSCLK source clock.
- PSCLK - PHY Serial Clock. This signal is always driven by the PHY device. Following an interface reset, the clock on this signal shall be a 100 MHz clock. Depending on the negotiated maximum data transfer rate between the PHY and the Link device, this clock signal may run at either 100 or 200 MHz. It is a nominally 50% duty cycle clock. The PHY device shall be an original provider of the interface source clock i.e. the PHY shall not derive its PSCLK signal from the incoming LSCLK signal.
- LSCLK - Link Serial Clock. This signal is always driven by the Link device. Following an interface reset, the clock on this signal shall be a 100 MHz clock. Depending on the negotiated maximum data transfer rate between the PHY and the Link device, this clock signal may run at either 100 or 200 MHz. It is a nominally 50% duty cycle clock. The Link device may derive its LSCLK output signal from the incoming PSCLK signal.

Note that the nominal frequency of the PSCLK & LSCLK signals shall be the same at all times. The frequency of the LSCLK & PSCLK signals may only change from 100 to 200 MHz or back upon the occurrence of a PHY-Link interface reset.

- 1 • LINKON - Optional Link On Event Notification. If provided, this signal is always driven by the PHY
2 device. This signal is used to provide notification to a Link device of a received Link-On PHY
3 packet by the PHY. The waveform transmitted by the PHY shall be capable of crossing an
4 isolation barrier.
- 5 • LPS - Optional Link Power Status Notification. If provided, this signal is always driven by the Link
6 device. This signal is used to provide notification to a PHY device of the powered status of the
7 Link. If this signal indicates that the Link device is powered, the Link shall be capable of
8 maintaining communications over the PHY-Link interface as specified in this standard.
- 9 • DIRECT - Optional Direct Connection Notification. This signal is an input to both PHY & Link devices.
10 If it is provided, this signal is used to indicate that the PHY and Link devices are directly
11 connected to each other i.e. a DC connection exists between both devices.
- 12 • LMODE - Optional Link Mode Indication. If provided, this is an input signal to the PHY device to
13 indicate that the PHY-Link interface is being used in a P1394a-compliant manner. The default
14 operation (including the case where this signal is not provided) is to support P1394b operation
15 only.

12.3 General Interface Characteristics

24 The operation of the PHY-Link interface is an evolution of the IEEE 1394-1995 & P1394a interface specifications. This
25 is to maximise the development effort that has been invested in 1394 Link & PHY designs to date, and recognises that the
26 existing interface provides a sound basis for the requirements of P1394b for higher speed 1394 connections.

29 New mechanisms are put in place to provide necessary features which are specific to P1394b. The interface is also
30 specified as being more symmetrical, in order to avoid any dead-lock or long latency situations where either the Link or
31 PHY device cannot establish communications with the other while a lengthy operation is taking place.

33 In general, the PHY device is the owner of the PHY-Link interface. All 1394 bus packets are transferred to the Link
34 device as they are received. The Link requests the use of the 1394 bus through the PHY. The PHY interprets and queues
35 the Link transmit requests as appropriate. When the PHY is granted the bus by the current BOSS, the PHY passes that
36 grant to the Link which then transmits data as required.

39 From a functional point of view, the PHY-Link interface can be viewed as a master-slave interface. At any point in time,
40 either the PHY or the Link is the current owner of the interface, and a handover mechanism to pass ownership from one
41 to the other is defined. Since the interface is source-clocked by both devices, there is a period during the handover where
42 the data and control buses are being transferred from one device to the other. It is essential that this handover be at the
43 same physical logic levels to avoid any bus contention which can lead to device reliability issues.

12.4 Initialization & Reset Behavior

52 <To be Defined>

12.5 PHY-Link Interface Phases

58 The PHY-Link interface defines a number of phases of operation in order to complete data transfers from the PHY to the
59 Link and vice versa. It is a goal of the interface specification that these phases all be uniquely identifiable in real time,
60 while retaining the use of a minimum of control pins. This goal can be achieved by using some context information on the
61 control lines, which allows the current state of the interface to be determined by looking at the current values on the
62 control lines in conjunction with previous values on these lines. This approach has some power dissipation penalties.

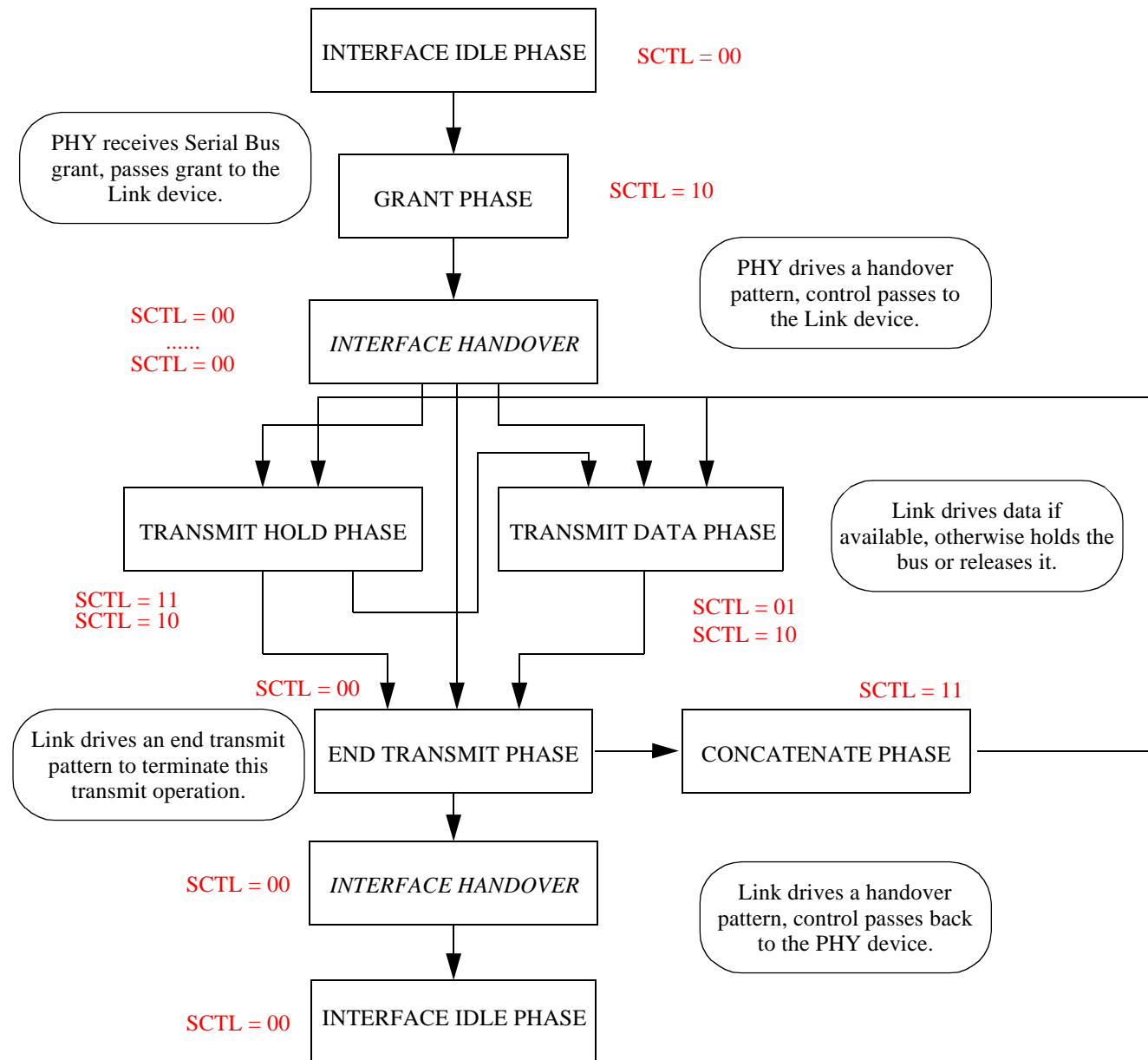
The typical operations which are carried out over the PHY-Link interface are

- 1394 Packet Transmit (data transferred from Link to PHY device)
- 1394 Packet Receive (data transferred from PHY to Link device)

Note that the transfer of status information from PHY to Link is accomplished over the PINT signal line.

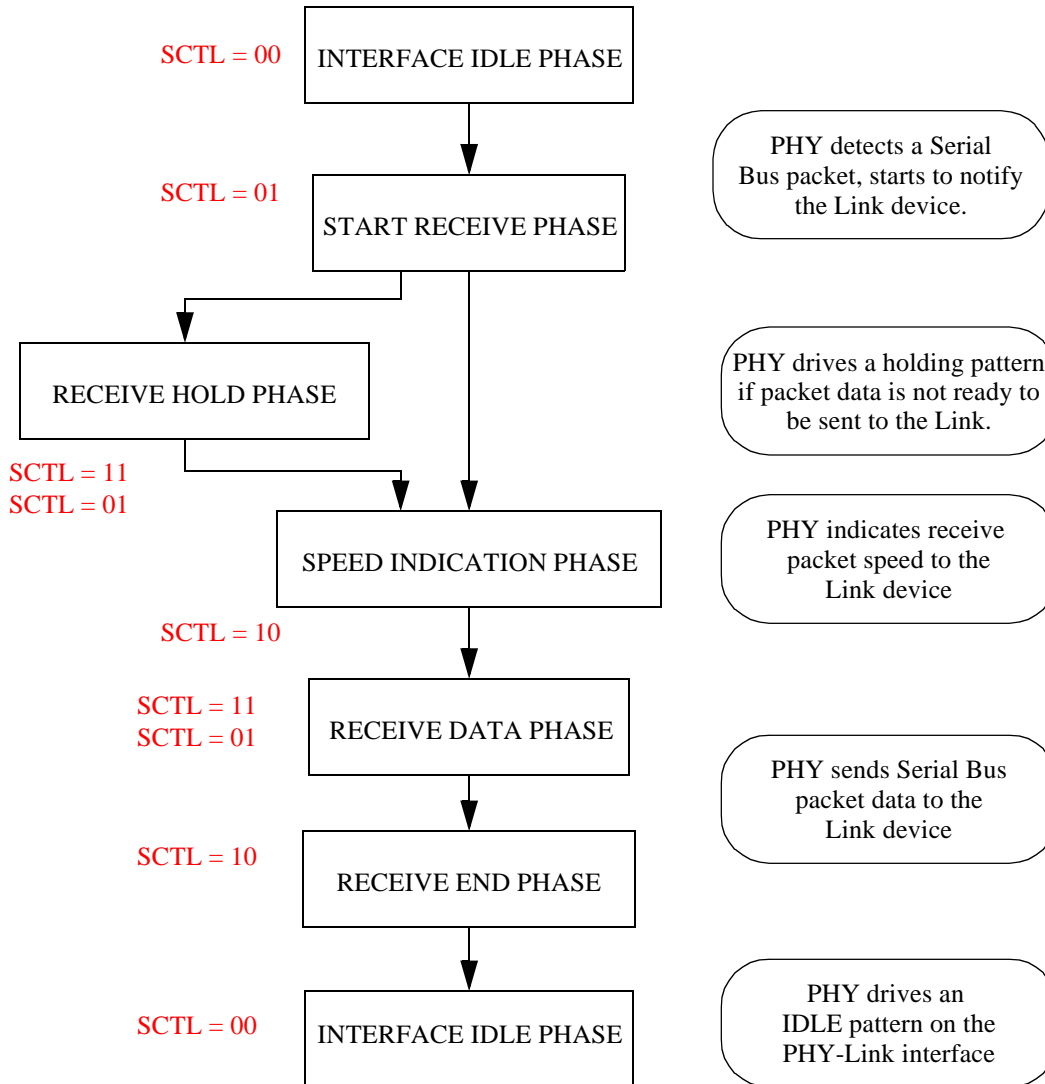
12.5.1 1394 Packet Transmit Operation

When the Link device has requested access to the Serial Bus via the LREQ signal, the PHY device performs an arbitration. When access to the Serial Bus has been granted to the PHY, the PHY propagates this grant to the Link device. The Link device then assumes ownership of the interface data and control buses. The Link device transmits 1394 packet data or bus holding symbols until such time as it has completed its packet transmit operation. Once the Link device has commenced transmitting 1394 packet information, it must continue to do so in consecutive PHY-Link interface bus cycles until transmission is complete. The operation of a packet transmission takes the following course:



12.5.2 1394 Packet Receive Operation

When the PHY device detects a 1394 packet being received over the Serial Bus, it initiates a packet receive operation to the Link device. The PHY device does not perform any packet filtering on the received information. Any PHY packets originated by the PHY device as part of bus initialisation are sent to its local link device in the same manner as packets received from other nodes. The Link device must be ready to receive a Serial Bus packet at any time over the PHY-Link interface. When the PHY has started to send a packet to the Link, it may send a holding pattern until such time as it has actual packet data to send. Once the PHY has started to send actual packet data, it shall send packet data information in consecutive PHY-Link interface bus cycles until transmission is complete. The operation of a packet receive takes the following course:



12.5.3 Definition of PHY-Link Interface Phases

The PHY-Link interface phases described in the previous transmit & receive operations are implemented by logic patterns on the SCTL lines. These patterns are outlined in the following tables:

Table 12-2—Transmit Phase Patterns

Transmit Phase	SCTL[1:0] Pattern(s)	Description
IDLE	00	PHY driving IDLE pattern as a default
GRANT	10	PHY issuing a bus GRANT to the Link device (one cycle)
<i>HANDOVER</i>	00	PHY drives SCTL=00 for <tb> interface cycles, followed by Link device driving SCTL=00 for <tb> interface cycles
TRANSMIT HOLD	11, 10	Link drives a holding pattern while data is prepared
TRANSMIT DATA	01, 10	Link drives a data transmission pattern while data is sent
END TRANSMIT	00	Link indicates that all valid transmit data has been sent
CONCATENATE	11	Link indicates that it has concatenated packets to send (<i>this phase may not be necessary</i>)
HANDOVER	00	Link drives SCTL=00 for <tb> interface cycles, followed by PHY device driving SCTL=00 for <tb> interface cycles
IDLE	00	PHY driving IDLE pattern (<i>minimum of <tb> cycles before any new operation can commence</i>)

During the Transmit Operation, the current status of the PHY-Link interface will generally be one of

- TRANSMIT_HOLD : SCTL[1:0] lines transitioning from [11] to [10] alternately **OR**
- TRANSMIT_DATA : SCTL[1:0] lines transitioning from [01] to [10] alternately

These patterns can be used during device validation as a simple means of determining that a Serial Bus packet transmit operation is in progress.

Table 12-3—Receive Phase Patterns

Receive Phase	SCTL[1:0] Pattern(s)	Description
IDLE	00	PHY driving IDLE pattern as a default
START RECEIVE	01	PHY indicates the start of a Serial Bus packet
RECEIVE HOLD	11, 01	PHY drives a holding pattern to indicate that Serial Bus packet data is not ready for transmission to the Link device.
SPEED INDICATION	10	PHY indicates the speed of the incoming packet to the Link
RECEIVE DATA	11, 01	PHY transfers Serial Bus packet data to the Link
RECEIVE END	10	PHY indicates that all packet data has been transferred
IDLE	00	PHY drives IDLE pattern

During the Receive Operation, the current status of the PHY-Link interface will generally be one of

- RECEIVE_HOLD : SCTL[1:0] lines transitioning from [11] to [01] alternately **OR**
- RECEIVE_DATA : SCTL[1:0] lines transitioning from [11] to [01] alternately

These patterns can be used during device validation as a simple means of determining that a Serial Bus packet receive operation is in progress.

<Is there any requirement for a RECEIVE_PAUSE state to aid in PHY receive buffer management - allow the PHY to pause sending data to the Link for a single interface cycle or more - no Link flow control anticipated ?>

<Do we need to send more information to the Link at the start of a packet receive - packet format (P1394a/P1394b), any 'source' information, any 'routing' information - these could be supported by allowing multiple SPEED_INDICATION phases>

< Specific requirement for a concatenated receive format ?>

12.6 Link Requests

There are two defined formats for Link requests, a short form and a more general extended form. The short form is used for time-critical request functions and common request operations to avoid creating a bottleneck for Link requests.

12.6.1 Short Form Link Requests

The short form Link request is used for the following Link requests/information

- Acknowledge Request
- Cycle Start Notification
- Rate Change Accept
- Rate Change Deny
- Interface Reset Request

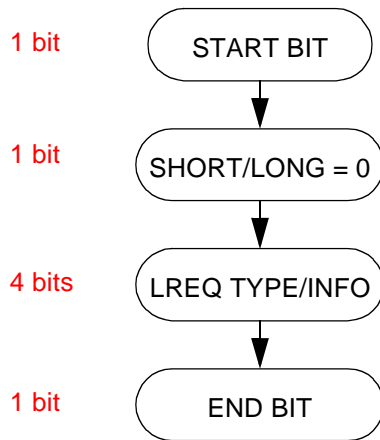


Figure 12-1—Short LREQ Form

12.6.2 Extended Form Link Requests

The extended form Link request is used for the following Link requests/information

- Packet Transmit Requests
- PHY Register read/write operations

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- Special request types

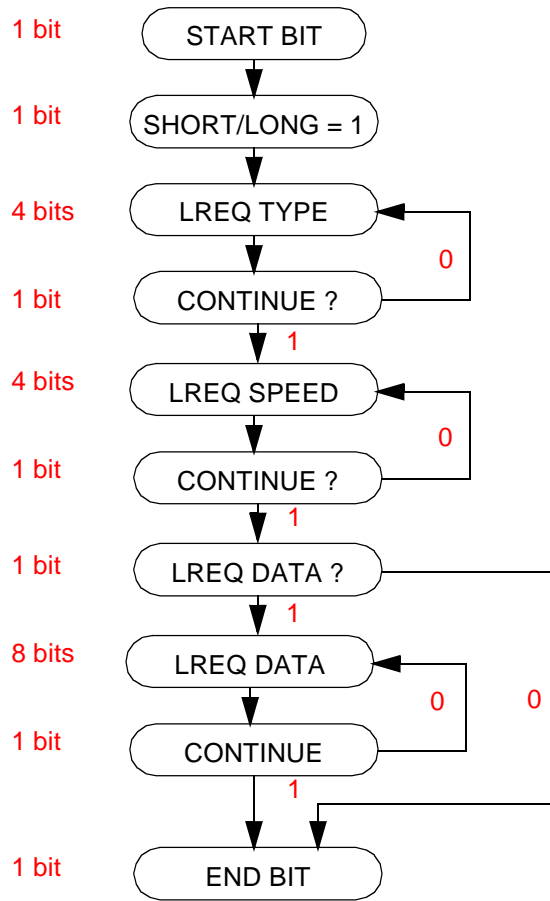


Figure 12-2—Extended LREQ Form

12.7 PHY Grants

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12.8 Status Transfers

All PHY status transfers as to take place over the PINT signal line. No status information is transferred over SDATA[7:0]. This allows packet transfers and status transfers to be completely independent, and avoids interrupted status issues etc.

Status Transfer format <td>

12.9 Isolation Interface

12.10 PHY/Link Interface Handover

The PHY-Link interface is designed to allow signal registering to be used on both sides. This facilitates scaling the interface clocking rate without creating onerous setup/hold requirements with respect to received clocks. Because of the source synchronous nature of the P1394b PHY-Link interface, this signal registering causes a latency in interface handover.

When the PHY issues a grant to the Link device, the following sequence of events takes place:

- PHY issues grant to the Link device
- PHY issues synchronized signal to internal logic to start process of 'listening' to the incoming Link-synchronous SCTL lines
- PHY drives HANDBOVER signal to <td> interface clock cycles - (initial analysis suggests 5)
- Link detects PHY grant.
- Link issues synchronized signal to internal output logic to indicate that control is to be taken of the PHY-Link interface.
- Link output logic drives HANDBOVER phase for <td> interface clock cycles - (initial analysis suggests 2).
- PHY starts to monitor incoming SCTL phase lines.
- Link drives TRANSMIT_HOLD or TRANSMIT_DATA phase.
- Interface handover is complete.

A similar process is used to return ownership of the interface to the PHY.

If the Link device fails to respond by driving TRANSMIT_HOLD or TRANSMIT_DATA after <td> cycles of monitoring by the PHY, the PHY shall take ownership of the interface again.

12.11 Interface Clocking Rate

This section describes a mechanism to transition from one interface clocking rate to another. This supports the defined 100 & 200 MHz interface clocking rates, and allows further interface clocking rates & schemes to be defined in a regular fashion.

The P1394b PHY-Link interface base clock rate is 100 MHz. When PHY and Link devices are reset (power-on reset), both devices shall communicate using a base rate of 100 MHz. The PHY shall source an interface clock of 100 MHz to Link. The Link shall source a 100 MHz clock to the PHY.

To change the PHY-Link interface clocking rate, the following handshake scheme is used. This scheme can be initiated by either the PHY or the Link device. The PHY-Link interface may only change clocking rate on an interface reset.

12.11.1 PHY-Initiated Interface Rate Change

- PHY sends Interface Rate Change status information to the Link, a request for the desired interface rate
- Link responds by sending a Rate Change Accept/Deny LREQ stream
- PHY initiates a PHY-Link interface reset
- PHY-Link interface re-starts as described in Reset/Initialization section at the new interface rate

If the Link does not respond with an Accept LREQ stream, the PHY shall not initiate the PHY-Link interface reset. The interface clocking rate shall remain at the current rate.

1 **12.11.2 Link-Initiated Interface Rate Change**

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- 3 • Link sends Interface Rate Change LREQ to the PHY, a request for the desired interface rate
- 4 • PHY responds by sending a Rate Change Accept/Deny status
- 5 • PHY initiates a PHY-Link interface reset
- 6 • PHY-Link interface re-starts as described in Reset/Initialization section at the new interface rate
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10 If the PHY does not respond with a Rate Change Accept status, the PHY shall not initiate the PHY-Link interface reset.
11 The interface clocking rate shall remain at the current rate.
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19 **12.12 Speed Format of received & transmitted packet data**

20 **12.12.1 100 MHz Interface Clocking Rate**

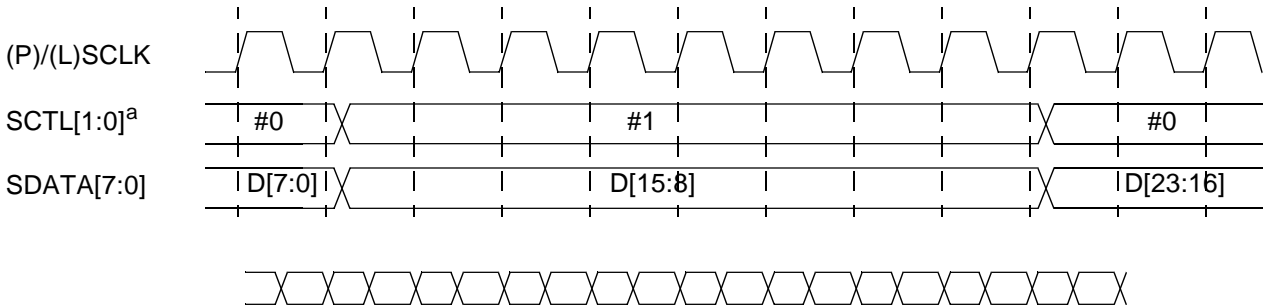
21 **12.12.1.1 S100 Data**

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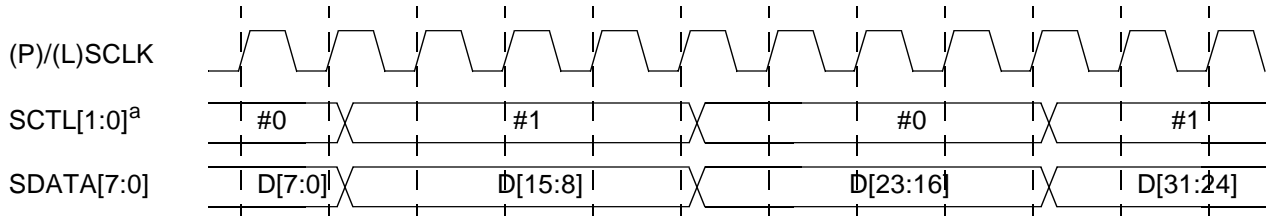
25 For packet data transmitted or received at S100, the following data delivery format is used to transfer the S100 data
26 to/from the PHY/Link device.
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42 ^a For a Transmit Operation, #0 = TRANSMIT_DATA_#0, #1 = TRANSMIT_DATA_#1,
43 For a Receive Operation, #0 = RECEIVE_DATA_#0, #1 = RECEIVE_DATA_#1
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12.12.1.2 S200 Data

For packet data transmitted or received at S200, the following data delivery format is used to transfer the S200 data to/from the PHY/Link device.



^a For a Transmit Operation, #0 = TRANSMIT_DATA_#0, #1 = TRANSMIT_DATA_#1,
For a Receive Operation, #0 = RECEIVE_DATA_#0, #1 = RECEIVE_DATA_#1

12.12.1.3 S400 Data

For S400, use same scheme as S100 & S200, change SCTL[1:0] every 2 cycles, SDATA[7:0] every 2 cycles

12.12.1.4 S800 Data

For S800, use same scheme as S100 & S200, change SCTL[1:0] every cycle, SDATA[7:0] every cycle

12.12.2 200 MHz Interface Clocking Rate

12.12.2.1 S100 Data

For S100, change SCTL[1:0] every 16 cycles, SDATA[7:0] every 16 cycles

12.12.2.2 S200 Data

For S200, change SCTL[1:0] every 8 cycles, SDATA[7:0] every 8 cycles

12.12.2.3 S400 Data

For S400, change SCTL[1:0] every 4 cycles, SDATA[7:0] every 4 cycles

12.12.2.4 S800 Data

For S800, change SCTL[1:0] every 2 cycles, SDATA[7:0] every 2 cycles

12.12.2.5 S1600 Data

For S1600, change SCTL[1:0] every cycle, SDATA[7:0] every cycle

12.12.2.6 S3200 Data

For S3200, change SCTL[1:0] every half cycle, SDATA[7:0] every half cycle

1 **12.12.2.7 S100 Data**
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3 For S100, change SCTL[1:0] every 16 cycles, SDATA[7:0] every 16 cycles
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