

12. P1394b PHY – Link interface specification

NOTE : This section is to be viewed as a discussion & proposal document. The contents of this section are under considerable review and comments/criticisms/suggestions are actively sought.

This section specifies the signalling, protocol & electrical characteristics of the PHY-Link interface. The interface is described in isolation from other operational characteristics of either PHY or Link devices. The PHY-Link interface specifies a point-to-point communications mechanism between a single P1394b Link and PHY device for the purpose of transfer of 1394 packet and status information between these two devices.

This interface describes mechanisms to support communication between PHY & Link devices at speeds of S100, S200, S400, S800, S1600 & S3200. For all of these cases, the interface pinout is identical. Variations in data clocking method and clock rate are used to accommodate the higher speeds. Lower speeds are accommodated by data padding.

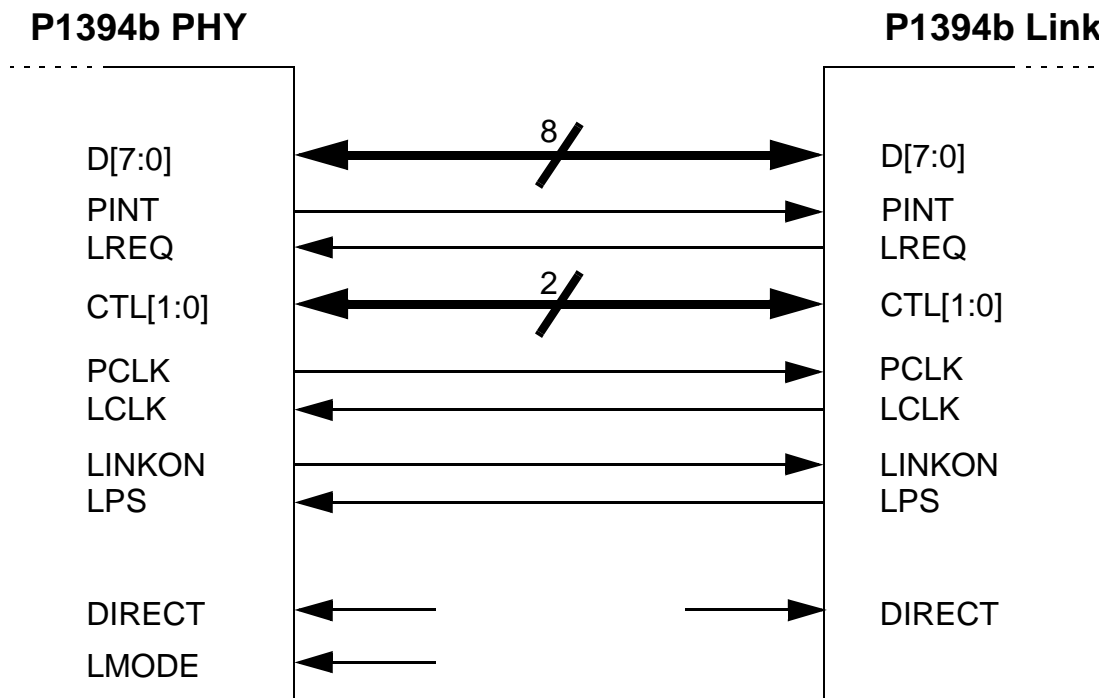
The P1394b PHY-Link interface is an evolution of the interface specified in the IEEE 1394-1995 & associated P1394a standards. The P1394b interface is a superset of the signals defined in those standards, and supports the operation of P1394a-compliant links. In this mode of operation, the complete set of functionality provided by the P1394b PHY will not be available. The purpose of this backwards-compatibility is to provide a migration path for existing P1394a Link applications.

12.1 P1394b PHY-Link Interface Requirements

The following are the requirements which are satisfied by the P1394b PHY-Link interface

- provides for bi-directional 1394 packet data transfer at S100, S200, S400, S800, S1600 & S3200
- provides a mechanism for status information transfer from the PHY to the Link
- provides a mechanism for the Link to access a register space within the PHY
- provides a means for the Link to request services from the PHY
- provides a means for the PHY to interrupt the Link during an operation
- supports an optional isolation interface to allow separate PHY & Link device power supply domains
- support operation by a P1394a-compliant link device
- provide a means for the current 'phase' of the PHY-Link interface to be more readily visible

12.2 P1394b PHY to P1394b Link Interface Pinout



12.2.1 Interface Signal Descriptions

The signals of the P1394b PHY-Link interface are divided into mandatory and optional signals.

The mandatory signals are D[7:0], PINT, LREQ, CTL[1:0], PCLK & LCLK. These signals shall be implemented by all PHY & Link devices adhering to this specification.

The optional signals are LINKON, LPS, DIRECT & LMODE. These signals may be implemented by PHY or Link implementations. If they are implemented, their operation shall be as described in this specification.

No other signals are specified to exist between a P1394b PHY & Link device. Any other signals that may be implemented fall outside the scope of this standard.

The following table describes the PHY-Link interface signals in brief.

Table 12-1— PHY-Link Interface Signal Descriptions

Signal Name	Direction	Description
D[7:0]	Bidirectional	PHY-Link interface Data bus. Mandatory 8-bit databus for all P1394b compatible PHY & Link devices
PINT	PHY Drives	PHY Interrupt. Mandatory PHY to Link interrupt indication
LREQ	Link Drives	Link Request. Mandatory Link to PHY request indication
CTL[1:0]	Bidirectional	PHY-Link Control bus. Mandatory 2-bit control bus for all P1394b compatible PHY & Link devices

Table 12-1— PHY-Link Interface Signal Descriptions

Signal Name	Direction	Description
PCLK	PHY Drives	PHY Source Clock. Mandatory PHY to Link interface serial clock source
LCLK	Link Drives	Link Source Clock. Mandatory Link to PHY interface serial clock source
LINKON	PHY Drives	Link On. Mandatory for the PHY, optional for the Link device.
LPS	Link Drives	Link Power Status. Mandatory for the PHY, optional for the Link device.
DIRECT	System Drives	Direct. Optional system indication of the connection type between PHY & Link
LMODE	System Drives	Link Mode. Optional system indication of the PHY-Link interface mode

12.2.1.1 Detailed Signal Descriptions

- D[7:0] - Serial Data. This databus is used to carry 1394 packet data, packet speed & grant type between the PHY and the Link. This is a bidirectional databus. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, data on this bus is to be considered to be synchronous to the PCLK source clock. When driven by the Link device, data on this bus is to be considered to be synchronous to the LCLK source clock.
- PINT - PHY Interrupt. This signal is always driven by the PHY and is valid after *<tb>* serial clock cycles following an interface reset. The serial information on this signal is used by the PHY to transfer status, register, interrupt and other information to the Link. The data on this signal is to be considered to be synchronous to the PCLK source clock.
- LREQ - Link Request. This signal is always driven by the Link and is valid after *<tb>* serial clock cycles following an interface reset. The serial information on this signal is used by the Link to request packet transmission and register/other status information from the PHY, as well as indicating the occurrence of certain Link events that are relevant to the PHY. The data on this signal is to be considered to be synchronous to the LCLK source clock.
- CTL[1:0] - Serial Control. This is a bidirectional control bus between the PHY and the Link. It is used to indicate the phase of operation of the interface. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, information on this bus is to be considered to be synchronous to the PCLK source clock. When driven by the Link device, information on this bus is to be considered to be synchronous to the LCLK source clock.
- PCLK - PHY Serial Clock. This signal is always driven by the PHY device. Following an interface reset, the clock on this signal shall be either a 100 or 200 MHz clock. It is a nominally 50% duty cycle clock. The PHY device shall be an original provider of the interface source clock i.e. the PHY shall not derive its PCLK signal from the incoming LCLK signal.
- LCLK - Link Serial Clock. This signal is always driven by the Link device. The Link device shall derive its LCLK output signal from the incoming PCLK signal. Depending on the PCLK signal, LCLK will either be a 100 or 200 MHz clock. LCLK is a nominally 50% duty cycle clock.
- LINKON - Optional Link On Event Notification. If provided, this signal is always driven by the PHY device. This signal is used to provide notification to a Link device of a received Link-On PHY packet by the PHY.
- LPS - Optional Link Power Status Notification. If provided, this signal is always driven by the Link device. This signal is used to provide notification to a PHY device of the powered status of the Link. If this signal indicates that the Link device is powered, the Link shall be capable of maintaining communications over the PHY-Link interface as specified in this standard.

- 1 • DIRECT - Optional Direct Connection Notification. This signal is an input to both PHY & Link devices. If it is provided, this signal is used to indicate that the PHY and Link devices are directly connected to each other i.e. a DC connection exists between both devices.
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- 4 • LMODE - Optional Link Mode Indication. If provided, this is an input signal to the PHY device to indicate that the PHY-Link interface is being used in a P1394a-compliant manner. The default operation (including the case where this signal is not provided) is to support P1394b operation only.
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12.3 General Interface Characteristics

The operation of the PHY-Link interface is an evolution of the IEEE 1394-1995 & P1394a interface specifications. This is to maximise the development effort that has been invested in 1394 Link & PHY designs to date, and recognises that the existing interface provides a sound basis for the requirements of P1394b for higher speed 1394 connections.

New mechanisms are put in place to provide necessary features which are specific to P1394b. The interface is also specified as being more symmetrical, in order to avoid any dead-lock or long latency situations where either the Link or PHY device cannot establish communications with the other while a lengthy operation is taking place.

In general, the PHY device is the owner of the PHY-Link interface. All 1394 bus packets are transferred to the Link device as they are received. The Link requests the use of the 1394 bus through the PHY. The PHY interprets and queues the Link transmit requests as appropriate. When the PHY is granted the bus by the current BOSS, the PHY passes that grant to the Link which then transmits data as required.

From a functional point of view, the PHY-Link interface can be viewed as a master-slave interface. At any point in time, either the PHY or the Link is the current owner of the interface, and a handover mechanism to pass ownership from one to the other is defined. Since the interface is source-clocked by both devices, there is a period during the handover where the data and control buses are being transferred from one device to the other. It is essential that this handover be at the same physical logic levels to avoid any bus contention which can lead to device reliability issues.

12.4 Initialization & Reset Behavior

The LPS input requests the PHY to disable or enable the PHY-Link interface. The output characteristics of LPS, if provided by the Link, depend upon the interface mode, differentiated or undifferentiated. When the interface mode is differentiated, LPS shall be a pulsed output while logically asserted. When logically deasserted, LPS shall be driven low in either interface mode. The characteristics of LPS are specified by figure and table .

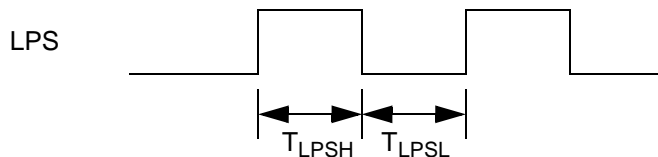


Figure 12-1—LPS waveform when differentiated

Table 12-2—LPS Timing parameters

Parameter	Description	Unit	Minimum	Maximum
T_{LPSL}	LPS low time (when pulsed)	μs	0.09	1.00
T_{LPSH}	LPS high time (when pulsed)	μs	0.09	1.00
T_{LPS_RESET}	Time for PHY to recognize LPS logically deasserted and reset the interface	μs	1.2	2.75
$T_{LPS_DISABLE}$	Time for PHY to recognize LPS logically deasserted and disable the interface	μs	25	30
$T_{RESTORE}$	Time to permit the optional differentiator and isolation circuits to restore during an interface reset	μs	15	20 ^a

^a. This maximum does not apply when the PHY-Link interface is disabled (see), in which case an indefinite time may elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface it is necessary that the Link ensure that LPS is logically deasserted for less than $T_{LPS_DISABLE}$.

The Link requests the PHY to reset the interface by deasserting LPS. Within 1.2 μs after it deasserts LPS, the Link shall place CTL[1:0] and D[7:0] in a high-impedance state and condition LREQ according to the interface mode: if undifferentiated, LREQ shall be driven zero otherwise it shall be placed in a high-impedance state.

If the PHY observes LPS logically deasserted for T_{LPS_RESET} , it shall reset the interface. The voltage levels shown in figure for CTL{1:0}, D[7:0] and LREQ while LPS is logically deasserted are accurate only for an undifferentiated interface, but the timing relationships remain accurate for both modes. When the interface is undifferentiated, the PHY drives CTL[1:0] and D[7:0] to zero. Otherwise, the PHY places the CTL[1:0] and D[7:0] signals in a high-impedance state.

If the Link continuously deasserts LPS for a longer period, it requests the PHY not only to reset but also to disable the interface. The Link shall condition its outputs as already described for reset.

If the PHY observes LPS logically deasserted for $T_{LPS_DISABLE}$, it shall disable the interface. The PHY has already reset the interface as described above; it now disables the interface by stopping PCLK. The voltage levels shown in figure for CTL[1:0], D[7:0], LREQ and PCLK while LPS is logically deasserted are accurate only for an undifferentiated interface, but the timing relationships remain accurate for both modes. When the interface is undifferentiated, the PHY disables the interface by driving PCLK to zero while continuing to drive CTL[1:0] and D[7:0] to zero. Otherwise, the PHY disables the interface by placing PCLK in a high-impedance state while continuing to maintain the CTL[1:0] and D[7:0] signals in a high-impedance state.

NOTE—When the PHY-Link interface is disabled and none of the PHY's ports are active or in a transitional state, the PHY may place most of its circuitry in a low power state.

When the PHY-Link interface is reset, the PHY shall cancel any outstanding bus request or register read request. Although the cancellation of bus requests may affect PHY arbitration stats in ways not described in section X, the PHY's behaviors (as observable from Serial Bus) shall be consistent with that section. For example, the PHY may have initiated arbitration in response to a bus request but reset of the PHY-Link interface might cancel the request before it is granted. Appropriate PHY behavior would be either the transmission of a null packet or the removal of the arbitration request before it is granted.

12.5 PHY-Link Interface Phases

The PHY-Link interface defines a number of phases of operation in order to complete data transfers from the PHY to the Link and vice versa. It is a goal of the interface specification that these phases all be uniquely identifiable in real time, while retaining the use of a minimum of control pins. This goal can be achieved by using some context information on the control lines, which allows the current state of the interface to be determined by looking at the current values on the control lines in conjunction with previous values on these lines. This approach has some power dissipation penalties.

The operations which are carried out over the PHY-Link interface are

- 1394 Packet Transmit (data transferred from Link to PHY device)
- 1394 Packet Receive (data transferred from PHY to Link device)

Note that the transfer of status information from PHY to Link is accomplished over the PINT signal line.

12.5.1 1394 Packet Transmit Operation

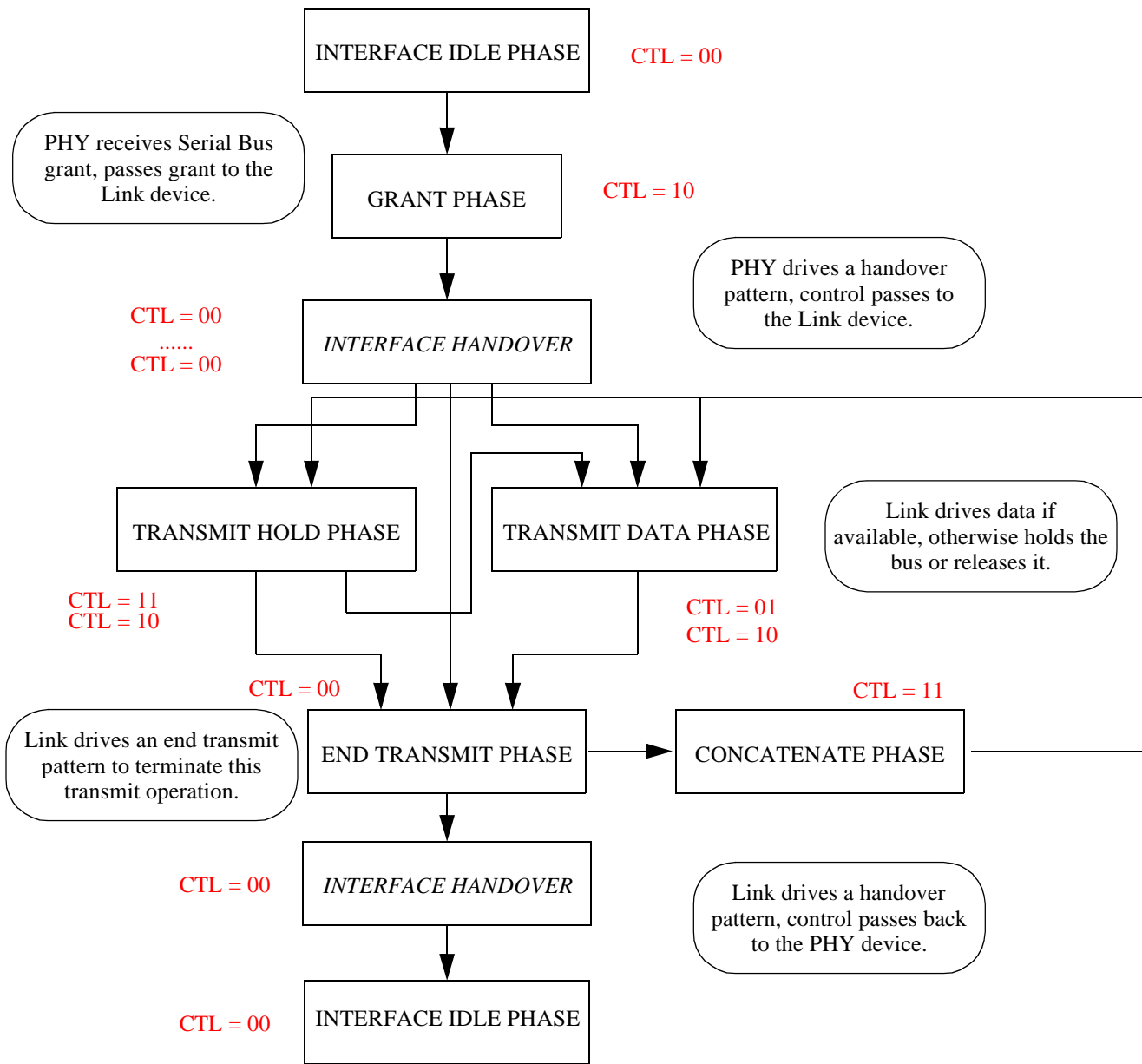
When the Link device has requested access to the Serial Bus via the LREQ signal, the PHY device performs an arbitration. When access to the Serial Bus has been granted to the PHY, the PHY propagates this grant to the Link device. The Link device then assumes ownership of the interface data and control buses. The Link device transmits 1394 packet data or bus holding symbols until such time as it has completed its packet transmit operation. Once the Link device has commenced transmitting 1394 packet information, it must continue to do so in consecutive PHY-Link interface bus cycles until transmission is complete.

The PHY device indicates to the Link the type of grant that is being given for this bus access, in order to distinguish asynchronous and isochronous bus grants. The PHY drives one of the following values on D[7:0] in the same cycle as driving GRANT on CTL[1:0]

Table 12-3—Grant Indications

D[7:0] Value during GRANT cycle	Description
00000000 ₂	Reserved
00000001 ₂	Asynchronous Transmit Grant
00000010 ₂	Isochronous Transmit Grant
00000100 ₂	Acknowledge Transmit Grant
00001000 ₂	Cycle Start Transmit Grant

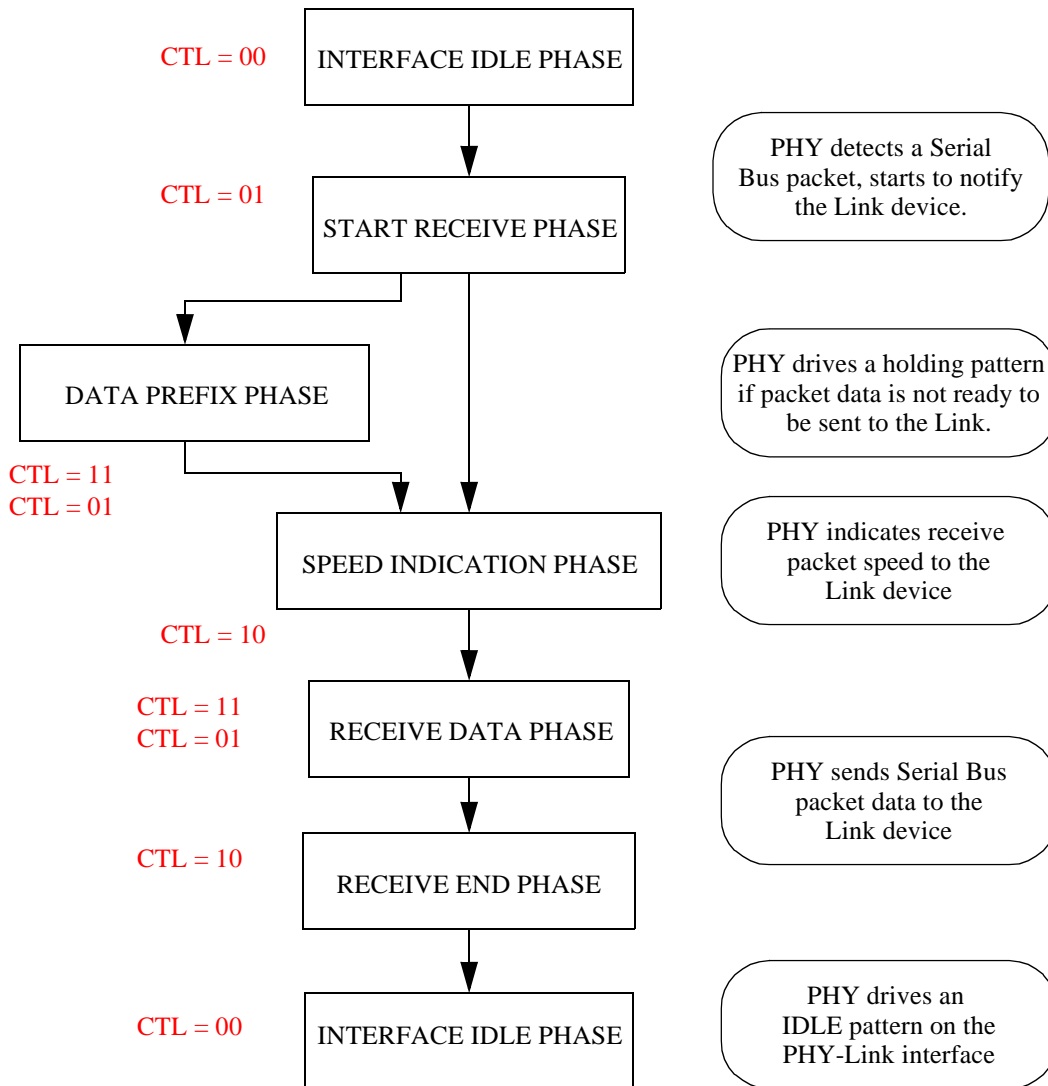
1 The operation of a packet transmission takes the following course:
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51 **12.5.2 1394 Packet Receive Operation**
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53 When the PHY device detects a 1394 packet being received over the Serial Bus, it initiates a packet receive operation to
54 the Link device. The PHY device does not perform any packet filtering on the received information. Any PHY packets
55 originated by the PHY device as part of bus initialisation are sent to its local link device in the same manner as packets
56 received from other nodes. The Link device must be ready to receive a Serial Bus packet at any time over the PHY-Link
57 interface. When the PHY has started to send a packet to the Link, it may send a holding pattern until such time as it has
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1 actual packet data to send. Once the PHY has started to send actual packet data, it shall send packet data information in
 2 consecutive PHY-Link interface bus cycles until transmission is complete. The operation of a packet receive takes the
 3 following course:
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12.5.3 Definition of PHY-Link Interface Phases

The PHY-Link interface phases described in the previous transmit & receive operations are implemented by logic patterns on the CTL lines. These patterns are outlined in the following tables:

Table 12-4—Transmit Phase Patterns

Transmit Phase	CTL[1:0] Pattern(s)	Description
IDLE	00	PHY driving IDLE pattern as a default
GRANT	10	PHY issuing a bus GRANT to the Link device (one cycle)
IDLE	00	PHY drives CTL=00 for <td> interface cycles, followed by Link device driving CTL=00 for <td> interface cycles
TRANSMIT HOLD	11, 10	Link drives a holding pattern while data is prepared
TRANSMIT DATA	01, 10	Link drives a data transmission pattern while data is sent
END TRANSMIT	00	Link indicates that all valid transmit data has been sent
CONCATENATE	11	Link indicates that it has a concatenated packet to send <i>(this phase may not be necessary)</i>
HANDOVER	00	Link drives CTL=00 for <td> interface cycles, followed by PHY device driving CTL=00 for <td> interface cycles
IDLE	00	PHY driving IDLE pattern <i>(minimum of <td> cycles before any new operation can commence)</i>

During the Transmit Operation, the current status of the PHY-Link interface will generally be one of

- TRANSMIT_HOLD : CTL[1:0] lines transitioning from [11] to [10] alternately **OR**
- TRANSMIT_DATA : CTL[1:0] lines transitioning from [01] to [10] alternately

These patterns can be used during device validation as a simple means of determining that a Serial Bus packet transmit operation is in progress.

Table 12-5—Receive Phase Patterns

Receive Phase	CTL[1:0] Pattern(s)	Description
IDLE	00	PHY driving IDLE pattern as a default
START RECEIVE	01	PHY indicates the start of a Serial Bus packet
DATA PREFIX	11, 01	PHY drives a data prefix pattern to indicate that Serial Bus packet data is not ready for transmission to the Link device.
SPEED INDICATION	10	PHY indicates the speed of the incoming packet to the Link
RECEIVE DATA	11, 01	PHY transfers Serial Bus packet data to the Link
RECEIVE END	10	PHY indicates that all packet data has been transferred
IDLE	00	PHY drives IDLE pattern

During the Receive Operation, the current status of the PHY-Link interface will generally be one of

- DATA_PREFIX : CTL[1:0] lines transitioning from [11] to [01] alternately **OR**
- RECEIVE_DATA : CTL[1:0] lines transitioning from [11] to [01] alternately

These patterns can be used during device validation as a simple means of determining that a Serial Bus packet receive operation is in progress.

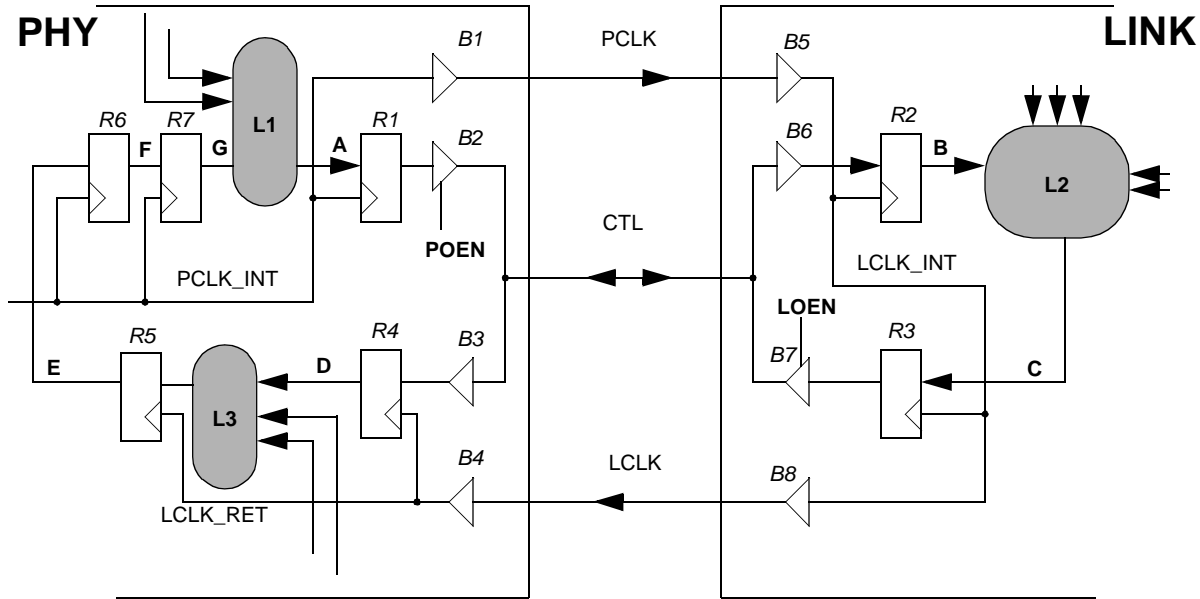
During the SPEED INDICATION phase, the PHY drives a value on D[7:0] to indicate the speed of the incoming Serial Bus packet in accordance with the following table

Table 12-6—SPEED_INDICATION values

D[7:0]	Packet Speed
00000000	Reserved
00000001	S100
00000010	S200
00000011	S400
00000100	S800
00000101	S1600
00000110	S3200
00000111-11111111	Reserved

12.6 PHY-Link Interface Handover

The handover of the interface from PHY to Link or vice versa is described in this section. This handover is complicated to some extent by the differing clock domains present in the PHY & Link devices. The expected clock domains are outlined in the following diagram:



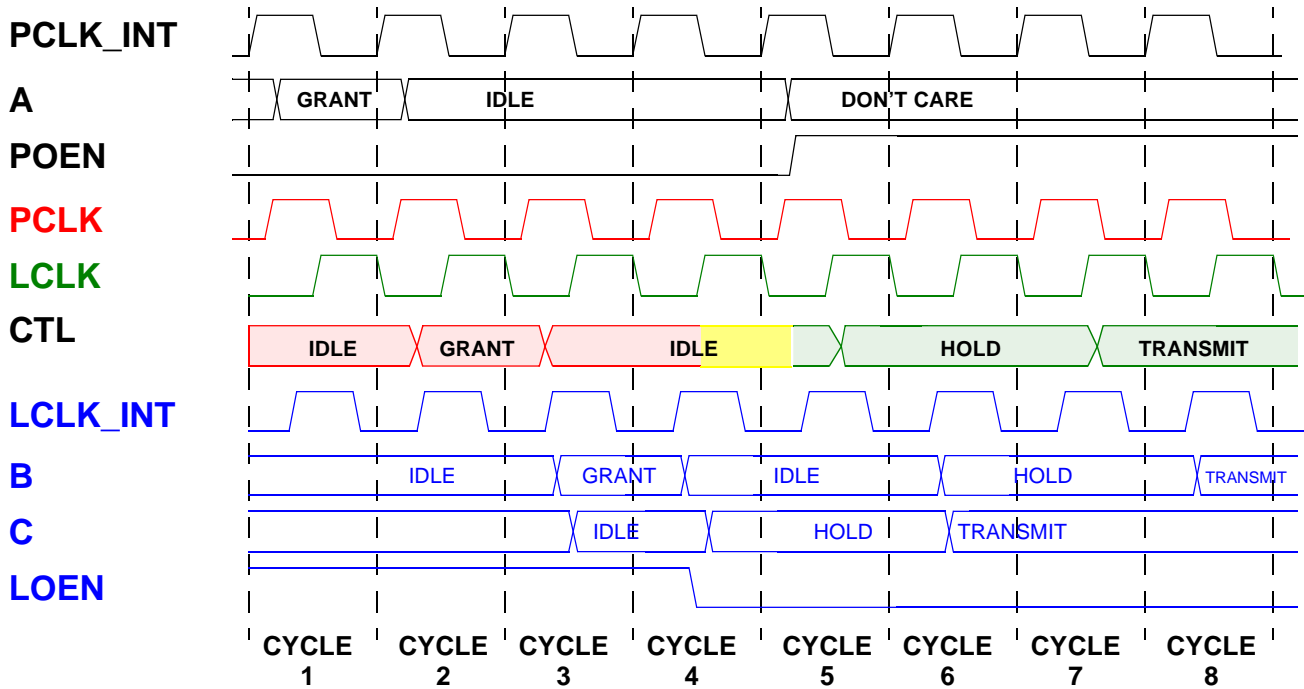
The following table explains the function of each of the elements above:

Element	Description	Element	Description
B1	Output I/O Buffer for PCLK	B2	Output Tristate I/O Buffer for CTL
B3	Input I/O Buffer for CTL	B4	Input I/O Buffer + Clock Tree for LCLK
B5	Input I/O Buffer + Clock Tree for PCLK	B6	Input I/O Buffer for received CTL
B7	Output Tristate I/O Buffer for CTL	B8	Output I/O Buffer for LCLK
R1	Required PHY D/CTL output register (clocked by PCLK_INT)	R2	Required Link D/CTL input register (clocked by LCLK_INT)
R3	Required Link D/CTL output register (clocked by LCLK_INT)	R4	Required PHY D/CTL input register (clocked by LCLK_RET)
R5	Register to generate clean 'handback event' pulse in the LCLK_RET domain	R6/R7	Stage 1/2 synchronisation register - synchronising handback signal back to PCLK_INT domain
L1	Logic to determine next PHY D/CTL logical signal level	L2	Logic to determine next Link D/CTL logical signal level
L3	Logic to gather post-registered input D/CTL signals to generate a combinational 'handback event' signal		
A	Pre-registered PHY output D/CTL	B	Post-registered Link input D/CTL
C	Pre-registered Link output D/CTL	D	Post-registered PHY input D/CTL
E	Registered 'Interface Handback Event' signal	F/G	Stage 1/2 synchronisation register output
POEN	PHY CTL Tristate Output Enable	LOEN	Link CTL Tristate Output Enable

Description of the Interface Handover (PHY to Link) (Cycle numbers refer to following diagram):

- a) PHY has control of the PHY-Link interface and is driving CTL Lines. PHY desires to hand over the interface to the Link and generates a GRANT value for one cycle (CYCLE 1), followed by a IDLE value for 3 cycles (CYCLES 2,3 & 4) on the A signals (pre-output register) in Logic L1.
- b) In the next interface cycle, this GRANT value is visible on the PHY-Link CTL signals (CYCLE 2). In the next interface cycle, this GRANT value is visible to the Link (CYCLE 3) on its internal B signals (post-input register).
- c) After driving the IDLE pattern for 3 cycle(s), the PHY tristates its CTL/D outputs.
- d) The Link combines B signals from all CTL signals in Logic L2 to determine that the PHY is handing over the interface. Within the same bus interface cycle (CYCLE 3), the Link generates signals C to drive the IDLE value back to the PHY to avoid bus contention issues.
- e) The Link drives the IDLE pattern for 1 cycle to avoid contention issues - during CYCLE 4, both PHY & Link are driving IDLE. In the following cycles, the Link then drives the required bus phase value (HOLD or TRANSMIT) and begins data transfer to the PHY.

The following timing diagram describes the PHY to Link interface handover process. From the timing diagram, the requirement for the PHY to drive three (3) cycles of IDLE and the Link to drive one (1) cycle of IDLE is visible:

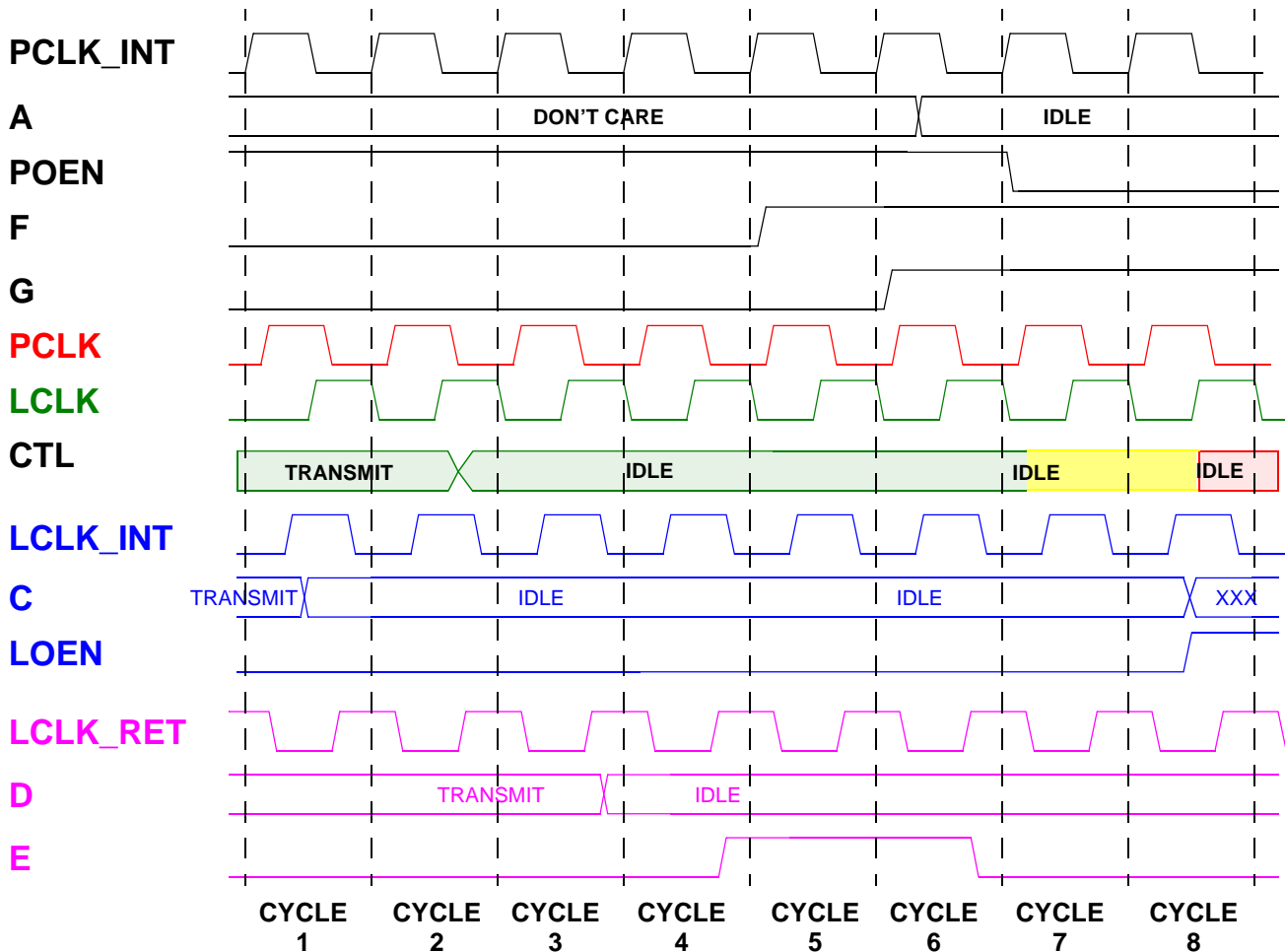


Note : in the above diagram, colour is used to indicate signals within a particular clock domain.

Description of the Interface Handover (Link to PHY) (Cycle numbers refer to following diagram):

- a) When the Link has completed its data transfer operation, it generates a IDLE pattern for 7 cycles (Cycles 2 to 8) on its C signals (pre-output register).
- b) In the next interface cycle (Cycle 3), this IDLE value is visible on the PHY-Link CTL signals. In the next interface cycle (Cycle 4), this IDLE value is visible to the PHY on its internal D signals (post-input register).
- c) After driving the IDLE pattern for 7 cycles, the Link tristates its CTL/D outputs.
- d) The PHY combines D signals from all CTL signals to determine that the Link is handing the interface back to the PHY - ie. an IDLE state has been detected. The PHY generates a combinational handback signal within Logic L3 within Cycle 4. This combinational signal must be registered in the LCLK_RET domain to be transferred reliably back to the PCLK_INT domain.
- e) The registered handback signal is resynchronised to the PCLK_INT domain by a metastability-safe two stage synchroniser (Cycles 5 & 6).
- f) The PHY drives the IDLE pattern to re-establish ownership of the PHY-Link interface (Cycle 7).
- g) Note that due to uncertainties in the PCLK_INT capture of the handback event (signal E), the Link is obliged to drive the IDLE state for one more cycle (Cycle 7) to ensure that the CTL lines are not allowed to go tri-state.

The following timing diagram describes the Link to PHY interface handover process. From the timing diagram, the requirement for the Link to drive seven (7) cycles of IDLE is evident:



Note : in the above diagram, colour is used to indicate signals within a particular clock domain.

NOTE—the Link device must accept ownership of the PHY-Link if a grant is issued by the PHY. If the Link does not have a request outstanding, the Link shall immediately hand the interface back to the PHY by driving IDLE appropriately.

12.7 Link Requests

The Link makes requests of the PHY to request packet transmit services or to notify the PHY of Link events that are relevant to the PHY's operation. The Link may issue transmit requests for the current or the next fairness interval. The Link may have up to five transmit requests outstanding at any time

- Asynchronous transmit request for the current fairness interval
- Asynchronous transmit request for the next fairness interval
- Isochronous transmit request for the current fairness interval
- Isochronous transmit request for the next fairness interval
- Cycle Start transmit request

Once a Link request has been accepted by the PHY, the Link request is valid until it is serviced, or until the Link issues a cancel request which is accepted by the PHY.

The format for Link requests is described in the following section. A short form is used for time critical or common operations, and an extended form is used for longer requests.

Link requests are generated in two flavors, a short form and an extended form. The short form is used to allow the Link to notify the PHY of the occurrence of specific events, or to request non-packet transmission related services. The following requests/notifications use the short LREQ form:

- Acknowledge Request
- Arbitration Acceleration Enable
- Arbitration Acceleration Disable
- Cycle Start Notification
- Subaction End Notification
- Interface Reset Request
- Cancel Asynchronous Transmit Request
- Cancel Isochronous Transmit Request

The extended LREQ format is used to make packet transmission requests and access PHY registers. The extended LREQ format contains speed information related to the bus request being issued or register address/data information:

- Asynchronous Transmission Request for this fairness interval
- Asynchronous Transmission Request for the next fairness interval
- Isochronous Transmission Request for this fairness interval
- Isochronous Transmission Request for the next fairness interval
- PHY register read request

- PHY register write request

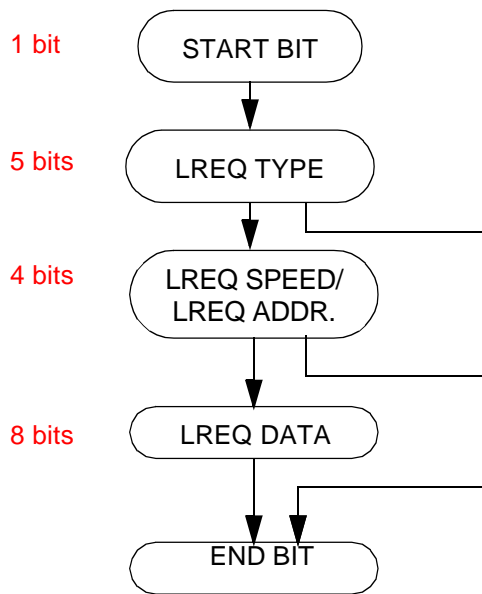


Figure 12-2— LREQ Format

Table 12-7—LREQ Type Definitions

LREQ Type	Description
00000	Acknowledgement Request
00001	Interface Reset Request
00010	Cycle start received notification
00011	Subaction End notification
00100	Cancel current asynchronous request
00101	Cancel current isochronous request
00110	Cancel next asynchronous request
00111	Cancel next isochronous request
01000	Arbitration Acceleration Enable
01001	Arbitration Acceleration Disable
01110	PHY Register Read request

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Table 12-7—LREQ Type Definitions

LREQ Type	Description
01111	PHY Register Write request
01010	Asynchronous request for this fairness interval
01011	Asynchronous request for next fairness interval
01100	Isochronous request for this fairness interval
01101	Isochronous request for next fairness interval
10000	Cycle Start request
10001	Beta-only asynchronous request for this fairness interval
10010	Beta-only asynchronous request for next fairness interval
10011	Beta-only isochronous request for this fairness interval
10100	Beta-only isochronous request for next fairness interval

NOTE—LREQ types of 10001_2 - 10100_2 indicate that the Link is aware that the Serial Bus path to the destination node is via all Beta-capable nodes. This will allow some packet format optimisations within the PHY for Beta-only networks or delivery paths.

For multi-bit fields such as LREQ Type, Address & Data, the most significant bit of the field is transferred first on PINT ie. LREQ Type[3] followed by Type[2], Type[1] & Type[0].

LREQ Type values of 01010_2 - 01111_2 indicate that there is additional information as part of the Link request. Other LREQ Type values do not require further information.

For LREQ Type values of 01110_2 & 01111_2 , the following four bits transferred represent the address of a register within the PHY device’s addressable space.

For an LREQ Type value of 1111_2 , there is an additional 8 bit field containing the data to be written to the specified PHY register.

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For LREQ Type values of 1010₂ - 1101₂, the four bits following the LREQ Type represent the requested transmit speed in accordance with the following table

Table 12-8—LREQ Speed Definitions

LREQ Speed	Description
0000	S100
0001	S1600
0010	S200
0011	S3200
0100	S400
0101	Not defined
0110	S800
0111-1111	Reserved

12.8 Status Transfers

All PHY status transfers take place over the PINT signal line. This is a full-time means of information transfer from the PHY to the Link. Status transfers are used to signal

- Serial Bus events necessary for the Link to perform its functions
 - Serial Bus Reset
 - Arbitration Reset Gap token
 - Subaction Gap token
 - PHY Interrupt
- Acknowledgement of a Link asynchronous/isochronous request
- Acknowledgement of a cancelled request
- Acknowledgement of a bus reset

Status transfers are also used to transfer PHY register information from the PHY to the Link in response to a PHY register read request. PHY status transfers can occur at the same time as LREQ requests are issued.

LREQ requests and status transfers are used to implement an unambiguous request generation/cancellation mechanism between the PHY and the Link. When the Link makes a bus request, the PHY acknowledges the request via a status transfer. This allows the Link to maintain a coherent picture of currently outstanding requests. The Link does not deem an issued request to be valid until such time as the PHY issues an acknowledgement status transfer.

Using an acknowledged mechanism for request generation avoids any problems with bus events overlapping with Link requests. For example, the Link issues a request to transmit an asynchronous packet in the next fairness interval at the same time as the current fairness interval is expiring according to the PHY. The PHY is in a position to know whether the Link request should be serviced in the new fairness interval or in the following one. In order for the Link to also know unambiguously, the PHY generates the appropriate sequence of status transfers. If the PHY issues a status transfer to indicate that the fairness interval has ended (arbitration reset gap indication) followed by a LREQ acknowledgement status transfer, the Link now unambiguously knows that its request will be serviced following another arbitration reset gap indication. If the PHY issues a status transfer for the LREQ acknowledgement followed by the status transfer indicating the arbitration reset gap, the Link unambiguously knows that its request will be serviced in the current fairness interval.

1 A similar mechanism applies to request cancellations. If the Link has made a transmit request which it now desires to
 2 cancel, there is a chance that the grant for that request will be received during the request for cancellation. If the PHY
 3 issues a Cancellation Acknowledgement status transfer, the Link unambiguously knows that its request has been
 4 cancelled. If the Link does not receive the Cancellation Acknowledgement, it must assume that its request has not been
 5 cancelled.
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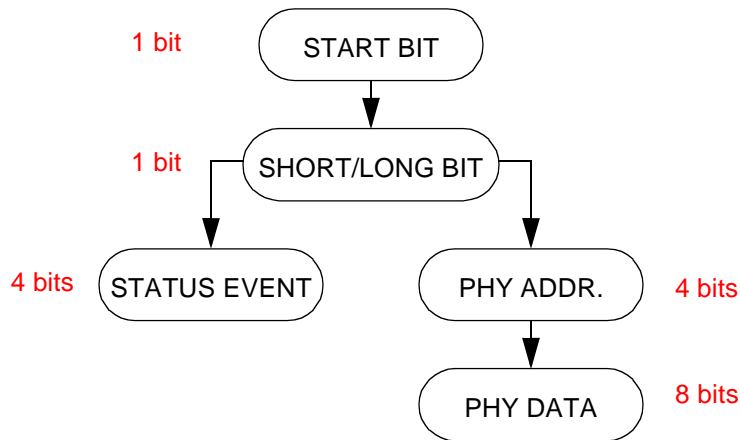


Figure 12-3— Status Transfer Format

29 The Start Bit of a status transfer is always a '1'.

31 The Short/Long bit indicates whether the remainder of the status transfer indicates a status event or a register transfer operation. A Short/Long bit value of '0' indicates a short transfer.

35 The Status Event field indicates the occurrence of a single PHY event. The occurrence of multiple PHY events is signalled by multiple status transfers. The order of status transfers is determined by the PHY.

Table 12-9—Status Event field definition

Status Event	Definition
0000	Reserved
0001	Serial Bus Reset
0010	Arbitration Reset Gap
0011	Subaction Gap
0100	PHY Interrupt
0101	Acknowledge Link Asynchronous Request for this fairness interval

Table 12-9—Status Event field definition

Status Event	Definition
0110	Acknowledge Link Isochronous Request for this fairness interval
0111	Acknowledge Link Asynchronous Request for the next fairness interval
1000	Acknowledge Link Isochronous Request for the next fairness interval
1001	Acknowledge Interface Reset Request
1010	Acknowledge Cancelled Asynchronous Request for this fairness interval
1011	Acknowledge Cancelled Isochronous Request for this fairness interval
1100	Acknowledge Cancelled Asynchronous Request for the next fairness interval
1101	Acknowledge Cancelled Isochronous Request for the next fairness interval
1110	Acknowledge Cycle Start request
1111	Reserved

12.9 Interface Clocking Rate

This specification describes three clocking rates for the PHY-Link interface - single-edge clocking running at 100 MHz (S800 capable), single-edge clocking running at 200 MHz (S1600 capable), double-edge clocking running at 200 MHz (S3200 capable).

A Beta-PHY whose maximum speed is S800 shall always use the single-edge clocking scheme at 100 MHz.

A Beta-PHY whose maximum speed is S1600 shall always use the single-edge clocking scheme at 200 MHz.

A Beta-PHY whose maximum speed is S3200 shall always use the double-edge clocking scheme at 200 MHz.

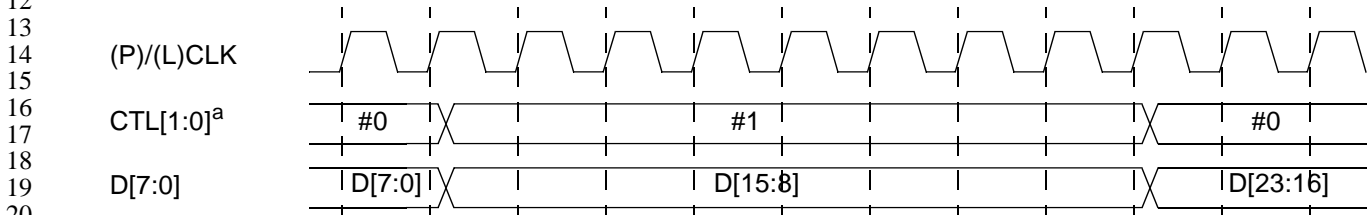
A Beta-Link may support any or all of the above clocking schemes. It is the responsibility of the system designer to ensure that the Beta Link and PHY use a compatible clocking scheme.

1 **12.10 Speed Format of received & transmitted packet data**

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3 **12.10.1 100 MHz Interface Clocking Rate**

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6 **12.10.1.1 S100 Data**

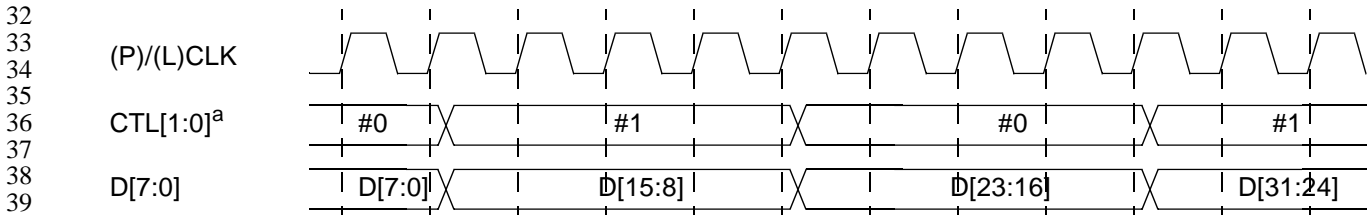
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8 For packet data transmitted or received at S100, the following data delivery format is used to transfer the S100 data
9 to/from the PHY/Link device.



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22 ^a For a Transmit Operation, #0 = TRANSMIT_DATA_#0, #1 = TRANSMIT_DATA_#1,
23 For a Receive Operation, #0 = RECEIVE_DATA_#0, #1 = RECEIVE_DATA_#1

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26 **12.10.1.2 S200 Data**

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28 For packet data transmitted or received at S200, the following data delivery format is used to transfer the S200 data
29 to/from the PHY/Link device.



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42 ^a For a Transmit Operation, #0 = TRANSMIT_DATA_#0, #1 = TRANSMIT_DATA_#1,
43 For a Receive Operation, #0 = RECEIVE_DATA_#0, #1 = RECEIVE_DATA_#1

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46 **12.10.1.3 S400 Data**

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48 For S400, use same scheme as S100 & S200, change CTL[1:0] every 2 cycles, D[7:0] every 2 cycles

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51 **12.10.1.4 S800 Data**

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53 For S800, use same scheme as S100 & S200, change CTL[1:0] every cycle, D[7:0] every cycle

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56 **12.10.2 200 MHz Interface Clocking Rate**

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59 **12.10.2.1 S100 Data**

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61 For S100, change CTL[1:0] every 16 cycles, D[7:0] every 16 cycles

1 **12.10.2.2 S200 Data**

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3 For S200, change CTL[1:0] every 8 cycles, D[7:0] every 8 cycles

5 **12.10.2.3 S400 Data**

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8 For S400, change CTL[1:0] every 4 cycles, D[7:0] every 4 cycles

10 **12.10.2.4 S800 Data**

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13 For S800, change CTL[1:0] every 2 cycles, D[7:0] every 2 cycles

15 **12.10.2.5 S1600 Data**

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18 For S1600, change CTL[1:0] every cycle, D[7:0] every cycle

20 **12.10.2.6 S3200 Data**

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23 For S3200, change CTL[1:0] every half cycle, D[7:0] every half cycle

25 **12.11 P1394a Link support**

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28 The P1394b PHY-Link interface is a superset of the P1394a signals. This allows a P1394b PHY to optionally support the
29 existing P1394a PHY-Link interface.

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32 If the optional LMODE input to the PHY is connected to logical '1', the Beta-PHY shall operate its PHY-Link interface
33 in accordance with the PHY-Link interface specification detailed in the P1394a specification. In this case, the P1394b
34 PHY-Link interface pins are used as follows:

35
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37 **Table 12-10—Mapping of P1394b PHY-Link signals to P1394a**

P1394b PHY-Link Interface pin	P1394a PHY-Link interface pin
SCTL[1:0]	SCTL[1:0]
D[7:0]	D[7:0]
PCLK	SCLK
LREQ	LREQ
LINKON	LINKON
LPS	LPS
LCLK	Not Used
PINT	Not Used
LMODE	Not Used

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62 In this mode of operation, packet and status transfers take place in the manner defined by P1394a. No P1394b specific
63 features, such as request for next cycle, request cancellation etc. are available. The P1394a LREQ cancellation rules also
64 take effect.
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