

## 12. P1394b PHY – Link interface specification

*NOTE: This section is to be viewed as a discussion & proposal document. The contents of this section are under considerable review and comments/criticisms/suggestions are actively sought.*

This section specifies the signalling, protocol & electrical characteristics of the PHY-Link interface. The interface is described in isolation from other operational characteristics of either PHY or Link devices. The PHY-Link interface specifies a point-to-point communications mechanism between a single P1394b Link and PHY device for the purpose of transfer of 1394 packet and status information between these two devices.

This interface describes mechanisms to support communication between PHY & Link devices at speeds of S100, S200, S400, S800, S1600 & S3200. For all of these cases, the interface pinout is identical. Variations in data clocking method and clock rate are used to accommodate the higher speeds. Lower speeds are accommodated by data padding.

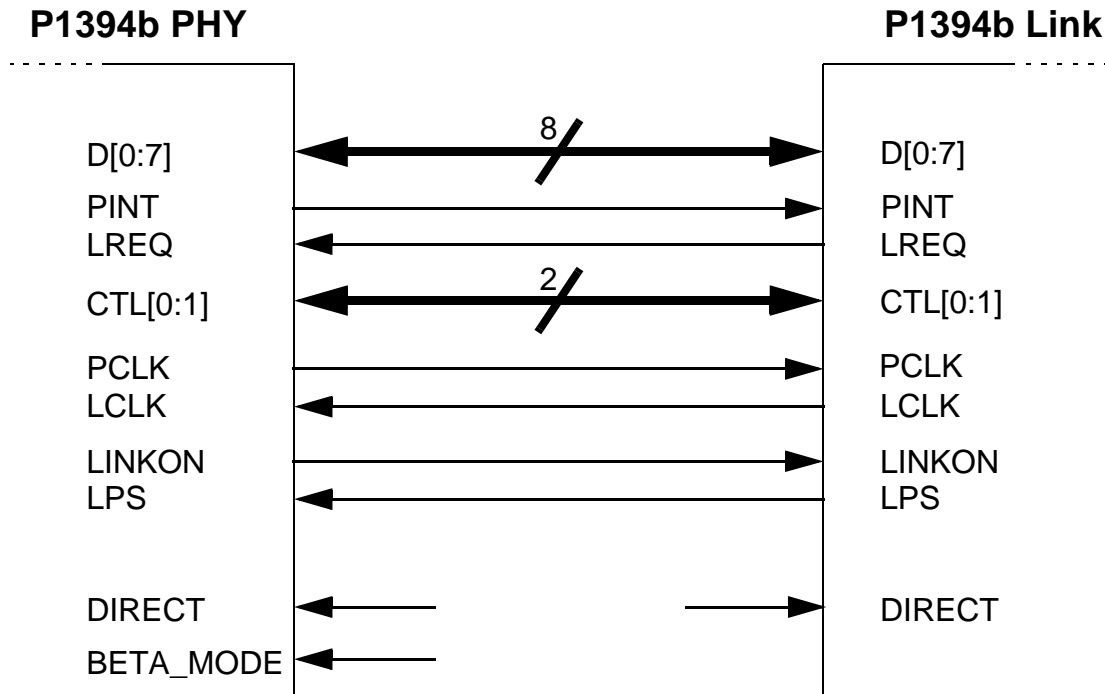
The P1394b PHY-Link interface is an evolution of the interface specified in the IEEE 1394-1995 & associated P1394a standards. The P1394b interface is a superset of the signals defined in those standards, and supports the operation of P1394a-compliant links. In this mode of operation, the complete set of functionality provided by the P1394b PHY will not be available. The purpose of this backwards-compatibility is to provide a migration path for existing P1394a Link applications.

### 12.1 P1394b PHY-Link Interface Requirements

The following are the requirements which are satisfied by the P1394b PHY-Link interface

- provides for bi-directional 1394 packet data transfer at S100, S200, S400, S800, S1600 & S3200
- provides a mechanism for status information transfer from the PHY to the Link
- provides a mechanism for the Link to access a register space within the PHY
- provides a means for the Link to request services from the PHY
- provides a means for the PHY to interrupt the Link during an operation
- supports an optional isolation interface to allow separate PHY & Link device power supply domains
- supports operation by a P1394a-compliant link device
- provide a means for the current operation on the PHY-Link interface to be more readily determined for debug
- supports operation between PHY & Link devices of 'adjacent' supply-voltages i.e.. 3.3V interoperates with 2.5V, 2.5V interoperates with 3.3V & 1.8V, 1.8V interoperates with 2.5V & 1.5V
- supports a minimum distance of 9 inches between PHY & Link discrete devices

**12.2 P1394b PHY to P1394b Link Interface Pinout**



**Figure 12-1—PHY-Link Interface Logical Signalling**

NOTE—this diagram indicates the logical signalling required between the PHY & Link devices and does not imply a DC connection between the two devices.

**12.2.1 Interface Signal Descriptions**

The signals of the P1394b PHY-Link interface are divided into mandatory and optional signals for the PHY & Link devices.

**12.2.1.1 PHY Device Signals**

The mandatory signals for the PHY device are D[0:7], PINT, LREQ, CTL[0:1], PCLK, LCLK, LINKON & LPS. These signals shall be implemented by all PHY devices adhering to this specification. The DIRECT & BETA\_MODE signals are optional for the PHY device. PHY devices that implement these signals shall do so in accordance with this specification.

**12.2.1.2 Link Device Signals**

The mandatory signals for the Link device are D[0:7], PINT, LREQ, CTL[0:1], PCLK & LCLK. These signals shall be implemented by all Link devices adhering to this specification. The LINKON, LPS & DIRECT signals are optional for the Link device. Link devices that implement these signals shall do so in accordance with this specification.

The following table describes the PHY-Link interface signals in brief.

**Table 12-1— PHY-Link Interface Signal Descriptions**

Signal Name	Direction	Description
D[0:7]	Bidirectional	PHY-Link interface data bus. Mandatory 8-bit databus for all P1394b compatible PHY & Link devices
PINT	PHY Drives	PHY Interrupt. Mandatory PHY to Link interrupt & status indication
LREQ	Link Drives	Link Request. Mandatory Link to PHY request indication
CTL[0:1]	Bidirectional	PHY-Link Control bus. Mandatory 2-bit control bus for all P1394b compatible PHY & Link devices
PCLK	PHY Drives	PHY Source Clock. Mandatory PHY to Link interface serial clock source
LCLK	Link Drives	Link Source Clock. Mandatory Link to PHY interface serial clock source
LINKON	PHY Drives	Link On. Mandatory for the PHY, optional for the Link device
LPS	Link Drives	Link Power Status. Mandatory for the PHY, optional for the Link device
DIRECT	System Drives	Direct. Optional system indication of the connection type between PHY & Link
BETA_MODE	System Drives	PHY-Link Interface Mode. Optional system indication of the PHY-Link interface mode

### 12.2.1.3 Detailed Signal Descriptions

- D[0:7] - Data. This databus is used to carry 1394 packet data, packet speed & grant type information between the PHY and the Link. This is a bidirectional databus. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, data on this bus is synchronous to the PCLK source clock. When driven by the Link device, data on this bus is synchronous to the LCLK source clock.
- PINT - PHY Interrupt. This signal is always driven by the PHY. The serial information on this signal is used by the PHY to transfer status, register, interrupt and other information to the Link. The data on this signal is synchronous to the PCLK source clock.
- LREQ - Link Request. This signal is always driven by the Link. The serial information on this signal is used by the Link to request packet transmission and register/other status information from the PHY, as well as indicating the occurrence of certain Link events that are relevant to the PHY. The data on this signal is synchronous to the LCLK source clock.
- CTL[0:1] - Control. This is a bidirectional control bus between the PHY and the Link. It is used to indicate the phase of operation of the interface. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, information on this bus is synchronous to the PCLK source clock. When driven by the Link device, information on this bus is synchronous to the LCLK source clock.
- PCLK - PHY Clock. This signal is always driven by the PHY device. Following an interface reset or after power-on reset, this signal shall be either a 100 or 200 MHz clock. It is a nominally 50% duty cycle clock. The PHY device shall be an original provider of the interface source clock i.e. the PHY shall not derive its PCLK signal from the incoming LCLK signal.
- LCLK - Link Clock. This signal is always driven by the Link device. The Link device shall derive its LCLK output from the incoming PCLK signal. Depending on the PCLK frequency, LCLK will either be a 100 or 200 MHz clock. LCLK is a nominally 50% duty cycle clock.

- 1 • LINKON - Link On Event Notification. This signal is always driven by the PHY device. This signal is  
2 used to provide notification to a Link device of a received Link-On PHY packet by the PHY.
- 3 • LPS - Link Power Status Notification. This is an input signal to the PHY device. This signal is used  
4 to provide notification to a PHY device of the powered status of the Link. If this signal  
5 indicates that the Link device is powered, the Link shall be capable of maintaining  
6 communications over the PHY-Link interface as specified in this standard.
- 7 • DIRECT - Direct Connection Notification. This signal is an input to both PHY & Link devices. If it is  
8 supported, this signal is asserted to indicate that the PHY and Link devices are directly  
9 connected to each other i.e. a DC connection exists between both devices.
- 10 • BETA\_MODE - PHY-Link Mode Indication. If provided, this is an input signal to the PHY device to indicate  
11 that the PHY-Link interface is being used in a P1394b-compliant manner. When asserted, the  
12 PHY-Link interface complies with this specification. When deasserted, the PHY-Link interface  
13 complies with the P1394a specifications.

### 12.3 General Interface Characteristics

22 The operation of the PHY-Link interface is an evolution of the IEEE 1394-1995 & P1394a interface specifications.

24 Mechanisms are put in place to provide new functionality which is specific to P1394b. The interface is specified as being  
25 more symmetrical, in order to avoid any dead-lock or long latency situations where either the Link or PHY device cannot  
26 establish communications with the other while a lengthy operation is taking place.

29 In general, the PHY device is the owner of the PHY-Link interface. All 1394 bus packets are transferred to the Link  
30 device as they are received. The Link requests the use of the Serial bus via the PHY device. The PHY interprets and  
31 queues the Link transmit requests as appropriate. When the PHY is granted access to the bus, the PHY passes that grant  
32 to the Link which then transmits data as required.

34 From a functional point of view, the PHY-Link interface can be viewed as a master-slave interface. At any point in time,  
35 either the PHY or the Link is the current owner of the interface, and a handover mechanism to pass ownership from one  
36 to the other is defined.

### 12.4 Interface Clocking Rate

42 This specification describes three clocking rates for the PHY-Link interface - single-edge clocking at 100 MHz (S800  
43 capable), single-edge clocking at 200 MHz (S1600 capable) & double-edge clocking at 200 MHz (S3200 capable).

46 A P1394b PHY whose maximum speed is S800 shall always use the single-edge clocking scheme at 100 MHz.

49 A P1394b PHY whose maximum speed is S1600 shall always use the single-edge clocking scheme at 200 MHz.

51 A P1394b PHY whose maximum speed is S3200 shall always use the double-edge clocking scheme at 200 MHz.

54 A P1394b Link shall support at least one of the above clocking schemes and may support more than one. It is the  
55 responsibility of the system designer to ensure that the P1394b Link and PHY use a compatible clocking scheme.

57 The PHY shall source its interface clock (PCLK) at the appropriate frequency for its maximum speed. The Link shall  
58 derive its LCLK from the PCLK signal. In this way, PCLK & LCLK are frequency-locked, but not phase-locked.

## 12.5 Interface Initialization & Reset

The LPS input, used to indicate the powered status of the Link, is also used to request the PHY to disable or enable the PHY-Link interface. The output characteristics of LPS, if provided by the Link, depend upon the interface mode, differentiated or undifferentiated. When the interface mode is differentiated, LPS shall be a pulsed output while logically asserted. When logically deasserted, LPS shall be driven low in either interface mode. The characteristics of LPS are specified by Figure 12-2 and Table 12-2.

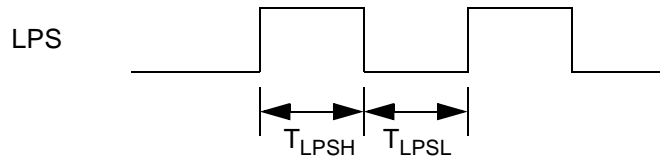


Figure 12-2—LPS waveform when differentiated

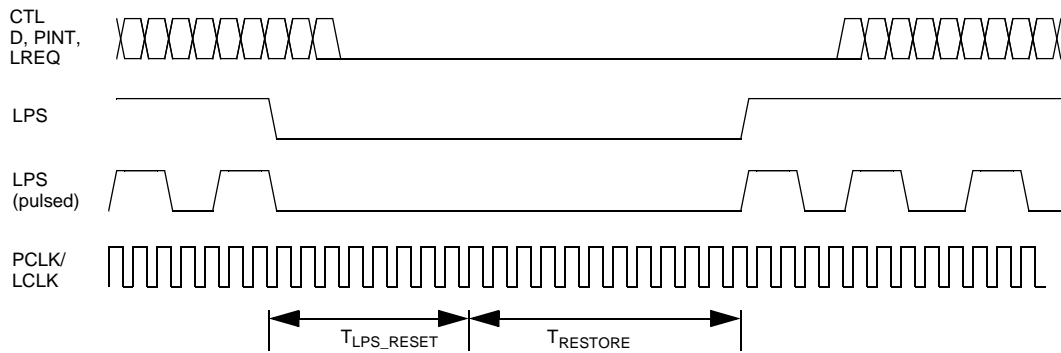
Table 12-2—LPS Timing parameters

Parameter	Description	Unit	Minimum	Maximum
$T_{LPSL}$	LPS low time (when pulsed)	$\mu\text{s}$	0.09	1.00
$T_{LPSH}$	LPS high time (when pulsed)	$\mu\text{s}$	0.09	1.00
$T_{LPS\_RESET}$	Time for PHY to recognize LPS logically deasserted and reset the interface	$\mu\text{s}$	1.2	2.75
$T_{LPS\_DISABLE}$	Time for PHY to recognize LPS logically deasserted and disable the interface	$\mu\text{s}$	25	30
$T_{RESTORE}$	Time to permit the optional differentiator and isolation circuits to restore during an interface reset	$\mu\text{s}$	15	20 <sup>a</sup>

<sup>a</sup> This maximum does not apply when the PHY-Link interface is disabled (see Figure 12-4), in which case an indefinite time may elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface it is necessary that the Link ensure that LPS is logically deasserted for less than  $T_{LPS\_DISABLE}$ .

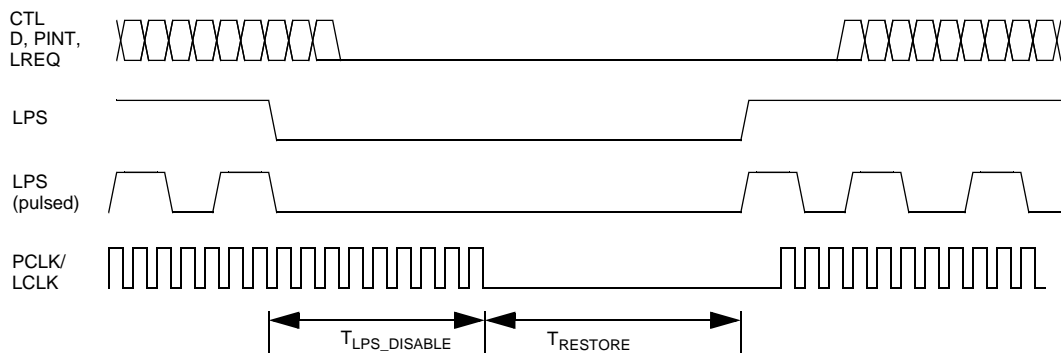
The Link requests the PHY to reset the interface by deasserting LPS. Within  $T_{LPS\_RESET(\text{min})}$  after it deasserts LPS, the Link shall place CTL[0:1] and D[0:7] in a high-impedance state and condition LREQ & LCLK according to the interface mode: if undifferentiated, LREQ & LCLK shall be driven zero otherwise they shall be placed in a high-impedance state.

If the PHY observes LPS logically deasserted for  $T_{LPS\_RESET}$ , it shall reset the PHY-Link interface. The voltage levels shown in Figure 12-3 for CTL[0:1], D[0:7], PINT and LREQ while LPS is logically deasserted are accurate only for an undifferentiated interface, but the timing relationships remain accurate for both modes. When the interface is undifferentiated, the PHY drives CTL[0:1], D[0:7] & PINT to zero. Otherwise, the PHY places the CTL[0:1], D[0:7] & PINT signals in a high-impedance state.



**Figure 12-3—PHY-Link interface reset via LPS**

If the Link continuously deasserts LPS for a longer period, it requests the PHY not only to reset but also to disable the PHY-Link interface. The Link shall condition its outputs as already described for reset.



**Figure 12-4—PHY-Link interface disable via LPS**

If the PHY observes LPS logically deasserted for  $T_{LPS\_DISABLE}$ , it shall disable the interface. The PHY has already reset the interface as described above; it now disables the interface by stopping PCLK. The voltage levels shown in Figure 12-4 for CTL[0:1], D[0:7], PINT, LREQ and PCLK while LPS is logically deasserted are accurate only for an undifferentiated interface, but the timing relationships remain accurate for both modes. When the interface is undifferentiated, the PHY disables the interface by driving PCLK to zero while continuing to drive CTL[0:1], D[0:7] & PINT to zero. Otherwise, the PHY disables the interface by placing PCLK in a high-impedance state while continuing to maintain the CTL[0:1], D[0:7] & PINT signals in a high-impedance state.

NOTE—When the PHY-Link interface is disabled and none of the PHY's ports are active or in a transitional state, the PHY may place most of its circuitry in a low power state.

When the PHY-Link interface is reset, the PHY shall cancel any outstanding bus or register read requests. Although the cancellation of bus requests may affect PHY arbitration status in ways not described in other parts of this specification, the PHY's behaviors (as observable from Serial Bus) shall be consistent with those sections. For example, the PHY may have initiated arbitration in response to a bus request but reset of the PHY-Link interface might cancel the request before it is granted. Appropriate PHY behavior would be either the transmission of a null packet or the removal of the arbitration request before it is granted.

This specification describes the PHY’s operation as if the interface to the Link is always operational. If the PHY-Link interface is reset while the Link is transmitting a packet, the PHY shall behave as if the Link had signaled IDLE and terminated the packet. Similarly, any status bit information generated by the PHY while the interface is disabled shall be zeroed and shall not cause a status transfer upon restoration of the interface.

The handshake just described either resets, or resets and then disables the interface when the Link deasserts LPS for  $T_{LPS\_RESET}$  or  $T_{LPS\_DISABLE}$  respectively. In either case (or after power reset), normal operations may be restored if the Link asserts LPS. After observing LPS, if PCLK is not already provided by the PHY, it shall resume PCLK as soon as possible. If the PHY-Link interface is differentiated and PCLK is resumed, the PHY shall commence by driving PCLK low for a minimum of 5ns. In either mode, the PHY shall ensure that clock duty cycle and period requirements are met from the first rising edge of PCLK onwards. Once PCLK is available the PHY and Link shall condition their CTL[0:1] and D[0:7] outputs in accordance with Table 12-3 . The reference point is the first rising edge of PCLK after LPS is asserted.

**Table 12-3—Initialization of the PHY-Link interface**

Device	Interface mode	
	Differentiated	Undifferentiated
PHY	For one and only one of the first six cycles of PCLK after the reference point, drive CTL[0:1], D[0:7] & PINT to zero and otherwise, for these cycles and the seventh, place them in a high-impedance state	Continue to drive CTL[0:1], D[0:7] & PINT to zero for the first seven cycles of PCLK after the reference point
Link	For one and only one of the first six cycles of PCLK after the reference point, drive CTL[0:1], D[0:7] and LREQ to zero and otherwise place them in a high-impedance state.	For one and only one of the first six cycles of PCLK after the reference point, drive CTL[0:1], D[0:7] and LREQ to zero; prior to this place them in a high-impedance state. Once these signals have been driven low, return CTL[0:1] and D[0:7] to a high-impedance state but continue to drive LREQ low until after the reset completes

NOTE—The PHY may not be able to determine its operating mode, differentiated or undifferentiated, during power reset. While the operating mode is indeterminate, the PHY shall place its outputs in a high-impedance state. The PHY shall not provide PCLK until the operating mode is determined and the PHY-Link interface is operational.

Upon the eighth PCLK cycle the PHY shall assert RECEIVE on CTL[0:1] while simultaneously providing data prefix indication on D[0:7] for at least one PCLK cycle. Upon the subsequent PCLK cycles the PHY shall continue to indicate data prefix while it is in a state in which it otherwise would be transferring data to the Link, after which it shall assert IDLE on CTL[0:1] & zero on D[0:7].

The Link may examine CTL[0:1] once it has driven CTL[0:1], D[0:7] and LREQ to zero for one cycle subsequent to the PCLK reference point. When the Link simultaneously observes RECEIVE on CTL[0:1] and data prefix on D[0:7] and subsequently observes IDLE on CTL[0:1], the reset of the PHY-Link interface is complete. No more than 10ms shall elapse from the reassertion of LPS until the interface is reset. The link shall not assert LREQ until the reset is complete.

## 12.6 Link-On Indication

The PHY LINKON output provides a method for the PHY to signal the Link at times when the Link is not active. The Link is inactive when either the LPS signal is logically deasserted (see clause 12.5) or the PHY register Link\_active bit is zero. The characteristics of the LINKON signal, specified by Table 12-4, permit the Link to detect LINKON in the absence of PCLK and also permit the signal to cross an optional isolation barrier. When LINKON is logically deasserted it shall be driven low.

**Table 12-4—LINKON timing parameters**

Description	Unit	Minimum	Maximum
Frequency	MHz	4	8
Duty cycle	%	40	60
Persistence Time, measured from the point at which both LPS is active and Link_active is one, after which the PHY shall not continue to signal LINKON	ns		500

When either LPS is logically false or the PHY register Link\_active bit is zero, a PH\_EVENT.indication of LINK\_ON shall cause the assertion of LINKON. This signal shall persist so long as the logical AND of the LPS signal and Link\_active is zero.

At other times (when the Link is active), a PH\_EVENT.indication of LINK\_ON shall be communicated to the Link by the transfer of the link-on packet that caused the event. The PHY shall not assert LINKON if the Link is already active.

The LINKON signal is also used to provide interrupt notification to an inactive Link. When any of the PHY register bits Loop, Pwr\_fail, Timeout or Port\_event is one and either LPS is logically false or the PHY register Link\_active is zero, the PHY shall assert LINKON. The PHY shall continue to assert LINKON so long as the Link remains inactive.

## 12.7 Link Requests & Notifications

The Link makes requests to the PHY to

- request asynchronous packet transmit services (other than Cycle Start)
- request a Cycle Start packet transmit service
- request isochronous packet transmit services
- request PHY register read/write operations

The Link issues notifications to the PHY to inform it of Link events that are relevant to its operation.

Link requests cannot be cancelled, and are queued within the PHY in the manner described in the following sections. If a Link wishes to effectively cancel an outstanding request, it shall abdicate its transmit opportunity when the PHY issues the relevant GRANT (see clause 12.8.1 for details)

### 12.7.1 Asynchronous Packet Transmit Requests (other than Cycle Start)

Both Link & PHY devices recognize the existence of a current fairness interval phase, either ODD or EVEN. The fairness interval phase is used to allow the Link to pipeline asynchronous transmit requests to the PHY. If the current fairness interval phase is EVEN, the Link may issue an asynchronous transmit request for the current phase or for the ODD phase,

1 and shall not issue an asynchronous transmit request for the EVEN phase. If the current fairness interval phase is ODD,  
2 the Link may issue an asynchronous transmit request for the current phase or for the EVEN phase, and shall not issue an  
3 asynchronous transmit request for the ODD phase.

4  
5 The PHY device provides notification of a fairness interval phase change via the appropriate Arbitration Reset status  
6 transfer (see Table 12-11). Upon receipt of this status transfer, the Link updates its current fairness interval phase. After  
7 an interface reset (or after power-on reset) the fairness interval phase shall be EVEN.

8  
9 The Link may have a maximum of two asynchronous transmit requests outstanding, one for the current phase and one for  
10 the next expected phase. Once the Link has made an asynchronous transmit request specifying the current phase, further  
11 requests specifying the current phase are ignored by the PHY. Once the Link has made an asynchronous transmit request  
12 specifying the next expected phase, further requests specifying the next expected phase are ignored by the PHY.

13  
14 Link asynchronous transmit requests may be made at any time. The Link request includes the requested packet speed.

### 15 16 17 18 **12.7.2 Cycle Start Transmit Requests**

19  
20 The Link uses Cycle Start transmit requests to indicate to the PHY that it requires to send a Cycle Start packet out on  
21 Serial Bus. The Link may issue a Cycle Start transmit request at any time. Once the Link has issued a Cycle Start transmit  
22 request, it shall not issue another until the first has been granted. Once the Link has made a Cycle Start transmit request,  
23 further Cycle Start transmit requests are ignored by the PHY until the first has been granted. The Link request includes  
24 the requested packet speed.

### 25 26 27 28 **12.7.3 Isochronous Packet Transmit Requests**

29  
30 The Link uses isochronous transmit requests to indicate to the PHY that it has isochronous data ready for transmission as  
31 part of the isochronous period. The Link can issue a standing isochronous transmit request to indicate to the PHY that it  
32 should arbitrate for bus access during each isochronous period. During isochronous periods where the Link requires to  
33 transmit additional isochronous information, the Link issues a normal isochronous transmit request.

34  
35 If the Link has already issued a standing isochronous transmit request, it shall not issue another standing isochronous  
36 request. Similarly, if the Link has already issued an isochronous transmit request for the current isochronous period, it  
37 shall not issue another until the first has been granted.

38  
39 Following a PHY-Link interface reset, any standing isochronous transmit request is not retained. The Link must re-issue  
40 a new standing isochronous transmit request to re-establish the pattern of isochronous packet transmission.

41  
42 The Link may issue isochronous transmit requests at any time. The Link request includes the requested packet speed. If  
43 the Link has already issued a standing isochronous request, further standing isochronous requests are ignored by the PHY.  
44 If the Link has already issued a normal isochronous transmit request, further normal isochronous transmit requests are  
45 ignored by the PHY until the first has been granted.

### 46 47 48 49 **12.7.4 PHY Register Read/Write Requests**

50  
51 The Link uses PHY register read & write requests to gain access to the PHY device's internal register space. The PHY  
52 address space is addressable via a 4-bit address, allowing for 16 register locations, each a single byte.

53  
54 The Link issues a PHY register read request to instruct the PHY to return the contents of one of its internal registers via  
55 a status transfer. The Link specifies the PHY address as part of the request. The Link shall not issue a further PHY  
56 register read request until the first has been completed via a status transfer. The PHY shall ignore further PHY register  
57 read requests until the first has been completed. PHY register reads may be initiated at any time.

58  
59 The Link issues a PHY register write request to write new contents to one of the PHY's internal registers. The Link  
60 supplies the PHY register address and the write data as part of the request. The PHY shall write the data content  
61 immediately to the appropriate PHY register. PHY register writes may be initiated at any time by the Link.

[Should PHY register writes be disallowed/ignored if a PHY register read is pending ??]

### 12.7.5 Link Request Format

The Link uses the following defined format to issue requests to the PHY device. Link requests are issued serially over the LREQ interface pin. The Link request begins with a START bit (always a '1'), followed by a 4-bit Link request type field. Depending on the Link request type, there may be a following 4-bit address and 8-bit data field. The Link request is completed with an END bit (always a '0'). Following the END bit, another Link request may be issued immediately.

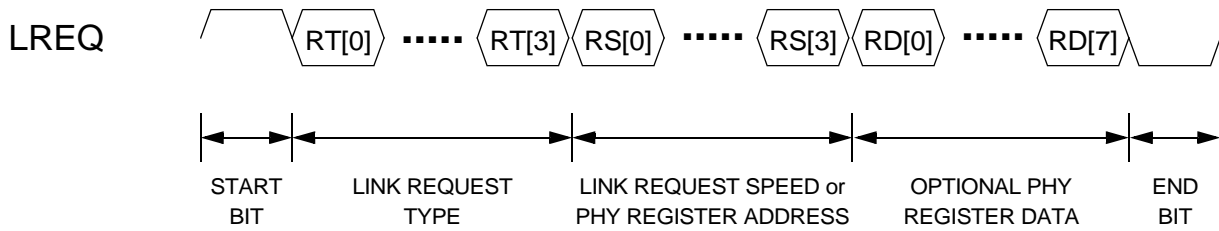


Figure 12-5— Link Request Format

NOTE—each cell in the Link Request Format represents one LCLK cycle time

Table 12-5—Link Request Type Encoding

RT[0:3] Value	Name	Meaning	Required Fields
0000	Reserved.	Reserved. The Link shall not transmit a request using this value	None
0001	Immediate	Used by the Link to request transmission of an acknowledge packet <i>(Note that the PHY assumes that the Link is requesting to transmit the acknowledge at the same speed as the current or last received packet)</i>	None
0010	Current Async.	Used by the Link to request transmission of an asynchronous packet in the current fairness interval	Request Speed
0011	Even Async.	Used by the Link to request transmission of an asynchronous packet in the even fairness interval phase	Request Speed
0100	Odd Async.	Used by the Link to request transmission of an asynchronous packet in the odd fairness interval phase	Request Speed
0101	Current Isoch.	Used by the Link to request transmission of an isochronous packet in the current isochronous period	Request Speed
0110	Standing Isoch.	Used by the Link to request that it requires to transmit isochronous packet data during each isochronous period	Request Speed
0111	Cancel Standing Isoch.	Used by the Link to cancel its request to transmit isochronous packet data during each isochronous period	None
1000	Cycle Start	Used by the Link to request transmission of a cycle start packet	Request Speed
1001	Reset	Used by the Link to request that the PHY-Link interface be reset, causing any current operation to be terminated and all outstanding requests to be cancelled	None
1010	Register Read	Used by the Link to request the contents of one of the PHY device's internal registers	Register Address

**Table 12-5—Link Request Type Encoding**

RT[0:3] Value	Name	Meaning	Required Fields
1011	Register Write	Used by the Link to write new contents to one of the PHY device's internal registers	Register Address & Data
1100	Not Used	Not Used	-
1101	Not Used	Not Used	-
1110	Not Used	Not Used	-
1111	Cycle Start Detected	Used by the Link to indicate to the PHY that a cycle start packet has been correctly received	None

[Are Beta-only requests necessary ??]

[Are Acceleration Control requests needed for P1394b ??]

**Table 12-6—Link Request Speed Encoding**

RS[0:3] Value	Meaning
0000	S100
0001	S1600
0010	S200
0011	S3200
0100	S400
0101	Reserved
0110	S800
0111-1111	Reserved

For PHY Register Read & Write operations, the RS[0:3] value represents a PHY device register location. For PHY Register Write operations, the RD[0:7] value represents the data to be written to the PHY device register.

The Link issues a Cycle Start Notification to the PHY after receiving a correctly formatted Cycle Start packet.

## 12.8 PHY-Link Interface Data Phases

The PHY-Link interface defines a number of phases of operation in order to complete data transfers from the PHY to the Link and vice versa. These phases should all be easily identifiable in real time, while retaining the use of a minimum of control pins. This is achieved by using a particular state encoding on the control lines, which allows the current state of the interface to be readily determined by looking at the current values on the control lines in conjunction with previous values on these lines.

The data operations which are carried out over the PHY-Link interface are

- 1394 Packet Transmit (data transferred from Link to PHY device)
- 1394 Packet Receive (data transferred from PHY to Link device)

NOTE— the transfer of status information from PHY to Link is accomplished over the PINT signal line.

The current phase of the PHY-Link interface is indicated by the CTL[0:1] signal lines, encoded as in the following tables

**Table 12-7—CTL[0:1] encoding when the PHY is driving**

CTL[0]	CTL[1]	Interface Phase	Phase Description
0	0	IDLE	The PHY has no information to transfer to the Link
0	1	Reserved	Reserved. The PHY shall not generate this CTL pattern
1	0	RECEIVE	The PHY is transferring packet information to the Link
1	1	GRANT	The PHY is indicating that it is handing the interface over to the Link

**Table 12-8—CTL[0:1] encoding when the Link is driving**

CTL[0]	CTL[1]	Interface Phase	Phase Description
0	0	IDLE	The Link has completed packet transmission and is handing the interface back to the PHY
0	1	TRANSMIT	The Link is transmitting packet information to the PHY
1	0	Reserved	Reserved. The Link shall not generate this CTL pattern
1	1	HOLD/ SUBACTION_END	When asserted at the start of a packet transmission, indicates that the Link is holding the PHY-Link interface while it is preparing data for transmission; when asserted at the end of a packet transmission, indicates that this packet represents the end of a subaction

Note that weak pulldowns are present on the CTL[0:1] & D[0:7] pins of the PHY-Link interface when DC coupled in order that the CTL[0:1] & D[0:7] lines assume/hold an IDLE state whenever neither PHY nor Link device is driving the interface.

### 12.8.1 1394 Packet Transmit Operation

When the Link device has requested access to the Serial Bus via the LREQ signal, the PHY device performs an arbitration. When access to the Serial Bus has been granted to the PHY, the PHY propagates this grant to the Link device. The Link device then assumes ownership of the interface data and control buses. The Link device may transmit bus holding symbols while it prepares data for transmission. The Link then transmits 1394 packet data until such time as it has completed its packet transmit operation. Once the Link device has commenced transmitting 1394 packet information, it must continue to do so in consecutive PHY-Link interface bus cycles until transmission is complete.

The packet transmission operation is described in the following timing diagram

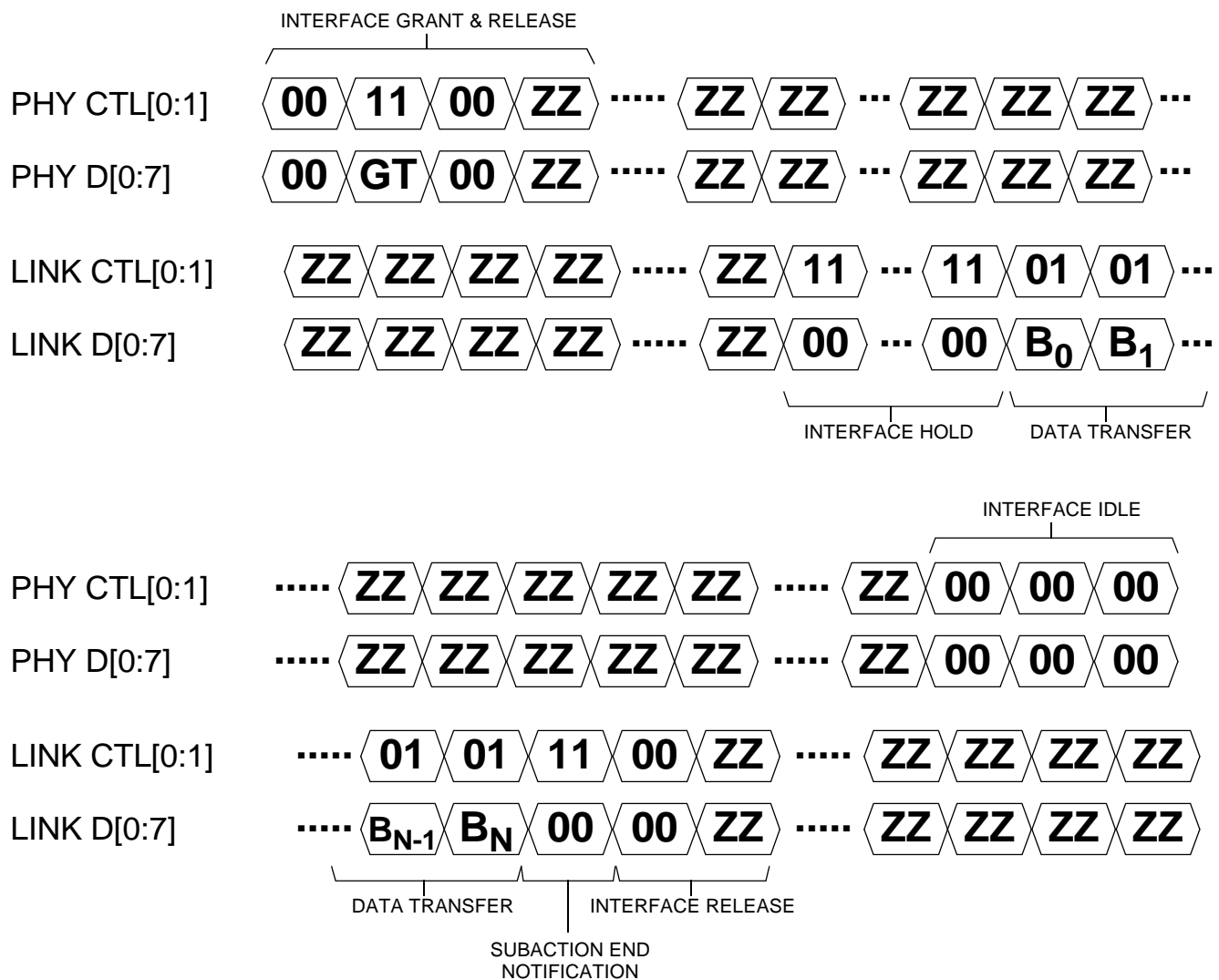


Figure 12-6—PHY-Link Packet Transmit Operation, including optional HOLD cycles

NOTE—B<sub>0</sub> - B<sub>N</sub> represent the information bytes transferred from the Link to the PHY. See clause 12.9 for a data format description.

Packet Transmission Description

- The PHY indicates that it is transferring ownership of the interface to the Link by asserting GRANT on the CTL lines for one cycle while driving the appropriate GNT value on the D lines (see Table 12-9). The PHY then pre-conditions the CTL & D lines by driving them to zero for one cycle. The PHY then releases the CTL & D lines to a high impedance state.
- The weak pulldowns hold the CTL & D lines low while the Link device completes the interface handover.
- The Link indicates that it has packet data to transmit by asserting HOLD or TRANSMIT on the CTL lines as soon as possible. If the Link does not have any data to transmit, it shall not drive any value on the CTL lines.
- The PHY monitors the CTL lines to determine if the Link has completed the interface handover. If the PHY has not detected either HOLD or TRANSMIT states within 8 PCLK cycles, the PHY will assume that the Link has abdicated its transmission opportunity and will assume control of the interface by driving IDLE.
- Assuming the Link has packet data to transmit, the Link may optionally transmit HOLD on the CTL lines while it is preparing data for transmission. The Link is not required to drive HOLD if it has data immediately ready for transmission. The Link will drive the D lines to zero during HOLD cycles.
- The Link asserts TRANSMIT on the CTL lines when it is transmitting packet data on the D lines.
- If the packet being transmitted represents the end of a subaction, the Link indicates this to the PHY by asserting SUBACTION\_END on the CTL lines and zero on the D lines for one cycle following packet data transmission.
- The Link terminates a packet transmission by asserting IDLE on the CTL lines for one cycle while driving zero on the D lines. The Link then releases the CTL & D lines to a high-impedance state.
- When the PHY detects the IDLE cycle from the Link, it shall regain ownership of the interface by driving IDLE on the CTL lines and zero on the D lines.

12.8.1.1 PHY-Link Interface Grant Types

The PHY indicates to the Link during the GRANT cycle which type of grant is being issued. This indication includes the grant type as well as the grant speed. The Link shall only use the bus grant for transmitting the granted packet type. The Link shall transmit the granted packet type only at the granted speed.

Table 12-9—GT values during Grant Cycle

D[0:3] Value during GRANT cycle	Grant Type	D[4:7] Value during GRANT cycle	Grant Speed
0000	Asynchronous Transmit Grant	0000	S100
0001	Isochronous Transmit Grant	0001	S1600
0010	Acknowledge Transmit Grant	0010	S200
0011	Cycle Start Transmit Grant	0011	S3200
0100-1111	Reserved	0100	S400
		0101	Reserved
		0110	S800
		0111-1111	Reserved

[Are Beta-only grant values necessary ??]

NOTE—Concatenated packet transmission is not supported by the PHY-Link interface

### 12.8.2 1394 Packet Receive Operation

When the PHY device detects a 1394 packet being received over the Serial Bus, it initiates a packet receive operation to the Link device. The PHY device does not perform any packet filtering on the received information. Any PHY packets originated by the PHY device as part of bus initialization are sent to its local link device in the same manner as packets received from other nodes. The Link device must be ready to receive a Serial Bus packet at any time over the PHY-Link interface. When the PHY has started to send a packet to the Link, it may send a holding pattern until such time as it has actual packet data to send. Once the PHY has started to send actual packet data, it shall send packet data information in consecutive PHY-Link interface bus cycles until transmission is complete.

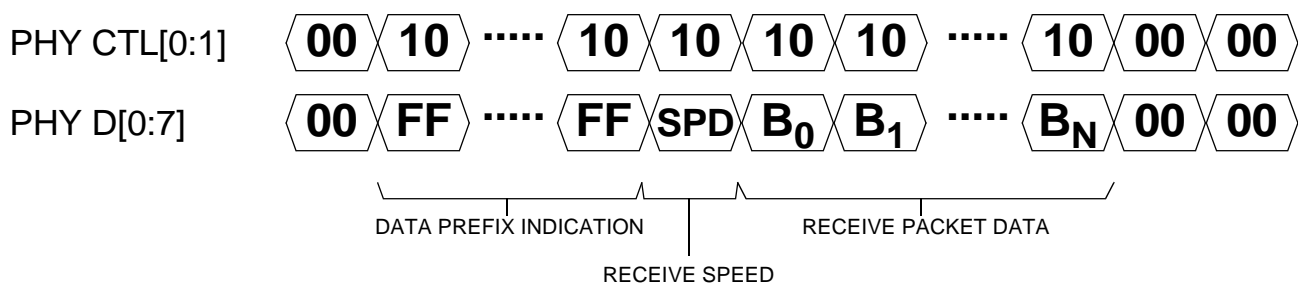


Figure 12-7—PHY-Link Packet Receive Operation

NOTE—B<sub>0</sub> - B<sub>N</sub> represent the information bytes transferred from the PHY to the Link. See clause 12.9 for a data format description.

#### Packet Receive Description

- The PHY indicates that it has packet information to send to the Link by asserting RECEIVE on the CTL lines. If there is no packet data ready for transfer to the Link at that time, the PHY will indicate this to the Link by asserting FF<sub>16</sub> on the D lines. The PHY will maintain this until such time as data is available.
- The PHY indicates the speed (hence the format - see clause 12.9 ) of the packet data by asserting a speed code on the D lines for one cycle while continuing to assert RECEIVE on the CTL lines.
- The PHY then transfers packet information to the Link on the D lines during successive cycles while continuing to assert RECEIVE on the CTL lines until the transfer is complete
- The PHY asserts IDLE on the CTL lines and 00<sub>16</sub> on the D lines to indicate the completion of the packet receive operation.

[Should there be a specification for a minimum IDLE time on the PHY-Link interface between packets ??]

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**Table 12-10—Receive Packet SPD encoding**

D[0:7] during SPD cycle	Receive Packet Speed
00000000	S100
01000000	S200
01010000	S400
01010001	S800
01010010	S1600
01010011	S3200
11111111	DATA_PREFIX
Other Values	Reserved

**12.9 Format of received & transmitted data**

The PHY and Link can transfer data to each other at the following rates : S100, S200, S400, S800, S1600 & S3200

The PHY-Link interface operates in one of three modes, depending on the maximum PHY transfer rate

- 98.304 MHz PCLK/LCLK, Single-edge clocking - S800 capable (Speed Mode 1)
- 196.608 MHz PCLK/LCLK, Single-edge clocking - S1600 capable (Speed Mode 2)
- 196.608 MHz PCLK/LCLK, Double-edge clocking - S3200 capable (Speed Mode 3)

Depending on the interface mode, data transfers between the devices are accomplished by appropriate padding of the lower rate data as described in the following sections.

**12.9.1 Speed Mode 1**

For this mode, PCLK & LCLK both run at 98.304 MHz ±100 ppm. Data transfers take place on the rising edge of PCLK & LCLK. In this mode, LREQ requests and PINT status notifications are transferred only on the rising edge of LCLK & PCLK respectively.

**12.9.1.1 S100 Data**

For packet data transmitted or received at S100, the following data delivery format is used to transfer the data to/from the PHY/Link device.

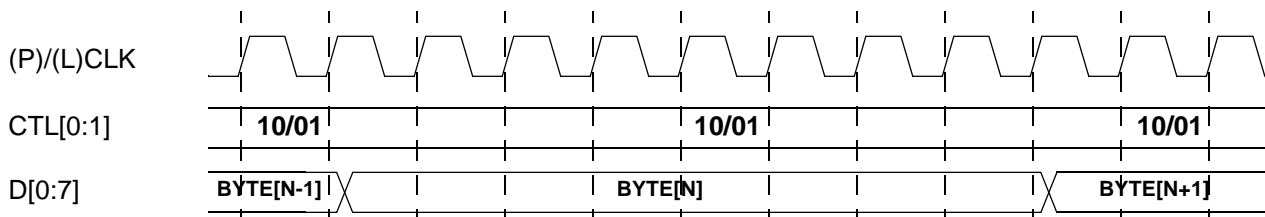


Figure 12-8—S100 Data transferred over 100 MHz, Single-edge clocking

### 12.9.1.2 S200 Data

For packet data transmitted or received at S200, the following data delivery format is used to transfer the data to/from the PHY/Link device.

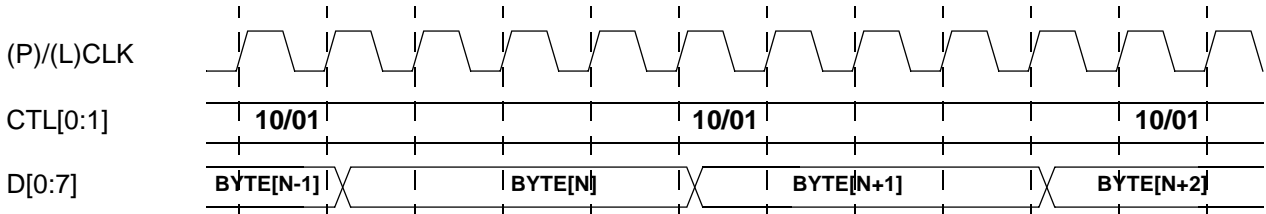


Figure 12-9—S200 Data transferred over 100 MHz, Single-edge clocking

### 12.9.1.3 S400 Data

For packet data transmitted or received at S400, the following data delivery format is used to transfer the data to/from the PHY/Link device.

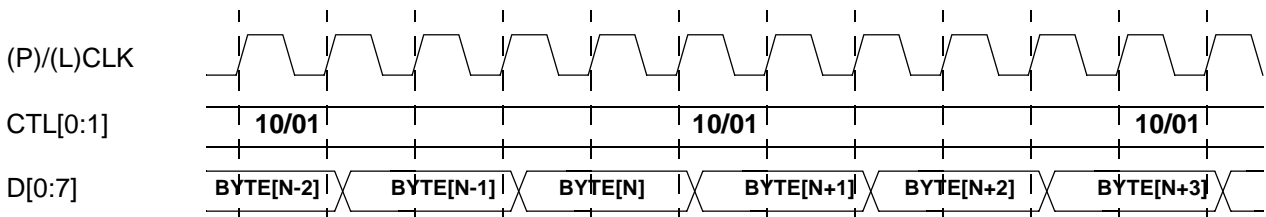


Figure 12-10—S400 Data transferred over 100 MHz, Single-edge clocking

### 12.9.1.4 S800 Data

For packet data transmitted or received at S800, the following data delivery format is used to transfer the data to/from the PHY/Link device.

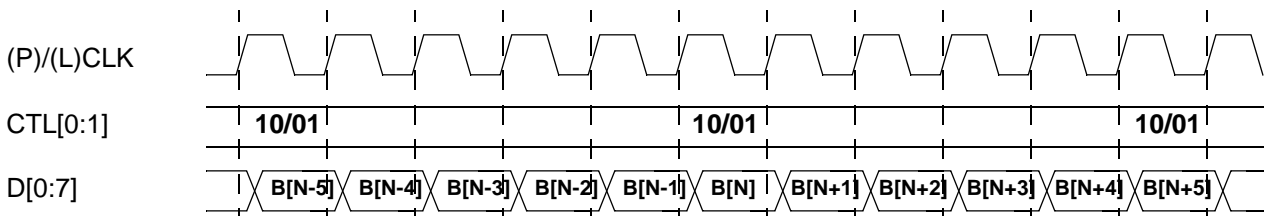


Figure 12-11—S800 Data transferred over 100 MHz, Single-edge clocking

## 12.9.2 Speed Mode 2

For this mode, PCLK & LCLK both run at 196.608 MHz  $\pm$ 100 ppm. Data transfers take place on the rising edge of PCLK & LCLK. In this mode, LREQ requests and PINT status notifications are transferred only on the rising edge of LCLK & PCLK respectively.

### 12.9.2.1 S100 Data

For packet data transmitted or received at S100, the following data delivery format is used to transfer the data to/from the PHY/Link device.

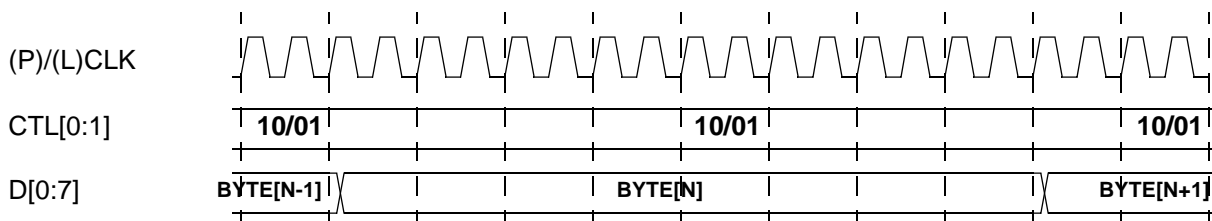


Figure 12-12—S100 Data transferred over 200 MHz, Single-edge clocking

### 12.9.2.2 S200 Data

For packet data transmitted or received at S200, the following data delivery format is used to transfer the data to/from the PHY/Link device.

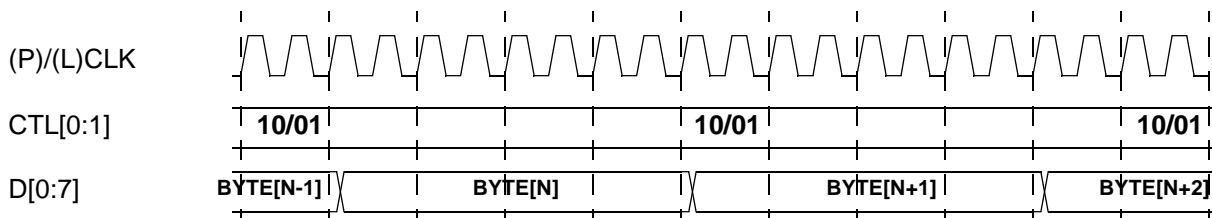


Figure 12-13—S200 Data transferred over 200 MHz, Single-edge clocking

### 12.9.2.3 S400 Data

For packet data transmitted or received at S400, the following data delivery format is used to transfer the data to/from the PHY/Link device.

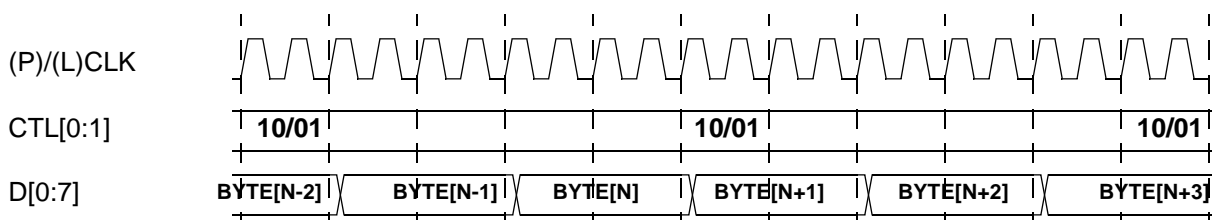


Figure 12-14—S400 Data transferred over 200 MHz, Single-edge clocking

### 12.9.2.4 S800 Data

For packet data transmitted or received at S800, the following data delivery format is used to transfer the data to/from the PHY/Link device.

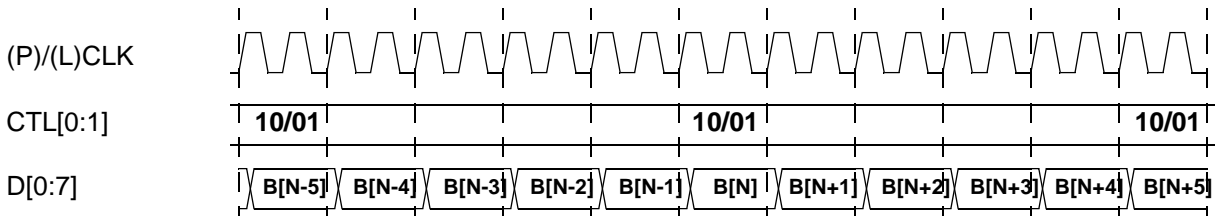


Figure 12-15—S800 Data transferred over 200 MHz, Single-edge clocking

### 12.9.2.5 S1600 Data

For packet data transmitted or received at S1600, the following data delivery format is used to transfer the data to/from the PHY/Link device.

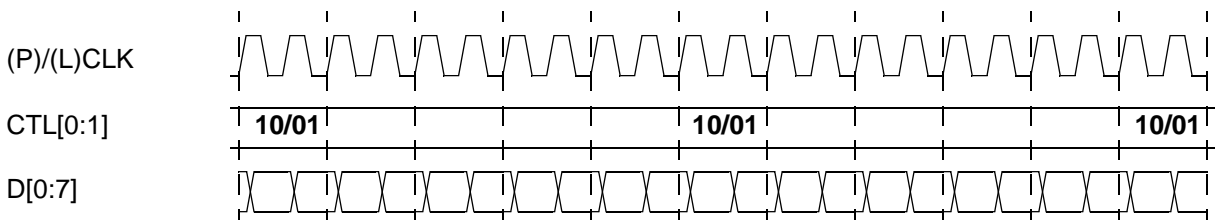


Figure 12-16—S1600 Data transferred over 200 MHz, Single-edge clocking

### 12.9.3 Speed Mode 3

For this mode, PCLK & LCLK both run at 196.608 MHz ±100 ppm. Data transfers take place on the rising & falling edge of PCLK & LCLK. In this mode, LREQ requests and PINT status notifications are transferred only on the rising edge of LCLK & PCLK respectively.

In Speed Mode 3, data transfers at S100 - S1600 take place in the same manner as Speed Mode 2.

#### 12.9.3.1 S3200 Data

For packet data transmitted or received at S3200, the following data delivery format is used to transfer the data to/from the PHY/Link device.

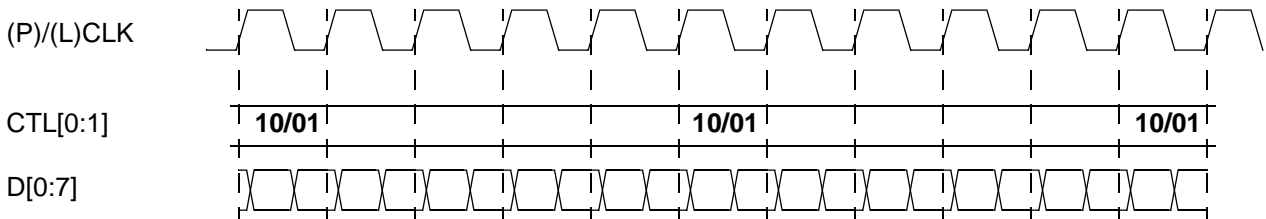


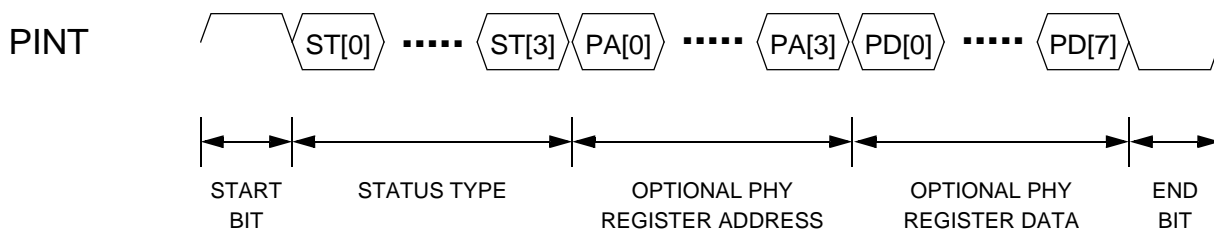
Figure 12-17—S3200 Data transferred over 200 MHz, Double-edge clocking

## 12.10 PHY Status Transfers & Notifications

The PHY issues status transfers & notifications to the Link to

- notify the Link of Serial Bus events relevant to its operation
- notify the Link of PHY events relevant to its operation
- return PHY register read data requested by the Link
- transfer the Serial Bus node ID to the Link during the Tree Identification phase

All PHY status transfers & notifications take place serially over the dedicated PINT signal. The format of the PHY status transfer depends on the information which is to be transferred.



**Figure 12-18— PHY Status/Interrupt Format**

NOTE—each cell in the Link Request Format represents one PCLK cycle time

### Status/Notification Transfer Mechanism

- The PHY begins a status transfer to the Link by asserting the PINT signal to ‘1’ for one cycle (START BIT)
- The PHY issues a 4 bit status type field serially over PINT. The status type determines if there are further fields associated with the status transfer
- If there are further fields, these are transferred serially over PINT
- The status transfer completes with the PHY deasserting the PINT signal to ‘0’ for one cycle (END BIT)

The PHY may immediately begin another status transfer following the END bit of the previous one. PHY status transfers can occur concurrently with Link requests and packet transmission/reception operations. Multiple status events are indicated by multiple status transfers. The ordering of status transfers is determined by the PHY.

**Table 12-11—PHY Status Type encoding**

ST[0:3] Value	Name	Meaning	Additional Fields
0000	Reserved	Reserved. The PHY shall not issue a status transfer of this value	None
0001	BUS_RESET	The PHY has detected the start of a Serial Bus Reset	None
0010	ARB_RESET_GAP_EVEN	The PHY has determined that an arbitration reset gap has occurred on Serial Bus. The PHY now deems the fairness interval phase to be EVEN	None
0011	ARB_RESET_GAP_ODD	The PHY has determined that an arbitration reset gap has occurred on Serial Bus. The PHY now deems the fairness interval phase to be ODD	None

**Table 12-11—PHY Status Type encoding**

ST[0:3] Value	Name	Meaning	Additional Fields
0100	SUBACTION_GAP	The PHY has determined that a subaction gap has occurred on Serial Bus	None
0101	PHY_INTERRUPT	The PHY requires the Link to read its internal register set to determine the cause of the interrupt	None
0110	PHY_RESET	The PHY has initiated a reset of the PHY-Link interface. The Link shall terminate any ongoing operation over the PHY-Link interface and shall deem all outstanding requests to have been cancelled	None
0111	REQ_IGNORED	The PHY may optionally return this status message to indicate that a Link request has been ignored because it has been incorrectly issued	None
1000	PHY_REGISTER	The PHY is returning the contents of one of its internal registers	PHY Address, PHY Data
1000 - 1111	Reserved	Reserved	None

PHY register read operations are completed by the PHY issuing a status transfer of type PHY\_REGISTER followed by the PHY address of the register being read, followed by the 8-bit data contents of the PHY register.

The PHY notifies the Link of its Node ID value during Tree ID by issuing an unsolicited PHY\_REGISTER transfer for PHY register 0. The PHY register contents contain the 6-bit Node ID value determined by the PHY as part of that process.

**12.11 PHY-Link Electrical Characteristics**

*[This section is not completed]*

**12.11.1 DC Signal Levels & Waveforms**

*[This section is not completed]*

**12.11.2 AC Timing**

*[This section is not completed]*

**12.11.3 Isolation Barrier**

*[This section is not completed]*

## 12.12 P1394a Link support

The P1394b PHY-Link interface is a superset of the P1394a signals. This allows a P1394b PHY to optionally support the existing P1394a PHY-Link interface. P1394b PHY devices are not required to support P1394a Link devices.

If the optional BETA\_MODE input to the PHY is connected to logical '0', the Beta-PHY shall operate its PHY-Link interface in accordance with the PHY-Link interface specification detailed in the P1394a specification. In this case, the P1394b PHY-Link interface pins are used as follows:

**Table 12-12—Mapping of P1394b PHY-Link signals to P1394a signals**

P1394b PHY-Link Interface pin	P1394a PHY-Link interface pin
CTL[0:1]	CTL[0:1]
D[0:7]	D[0:7]
PCLK	SCLK
LREQ	LREQ
LINKON	LINKON
LPS	LPS
LCLK	Not Used - system drives logical '0'
PINT	Not Used - PHY drives logical '0'
BETA_MODE	Not Used - system drives logical '0'

In this mode of operation, Link requests, Link & PHY packet transfers and PHY status transfers take place in the manner defined by P1394a. No P1394b specific features, such as request for next cycle, Link requested interface reset etc. are available. The existing P1394a LREQ cancellation rules also take effect.

Data transfers at S100, S200 & S400 only are supported by the PHY-Link interface in this mode.

In this mode of operation, the LCLK input to the PHY should be driven to logical '0'. The PHY PINT signal output shall be driven to logical '0' and should not be used.

To facilitate existing P1394a Link implementations using a P1394b PHY, the timing relationships defined by P1394a for the PHY-Link interface pins shall be adhered to by a P1394b PHY offering this capability.

*[Is there additional information required to allow P1394a Links to use a P1394b PHY ??]*

*[Is P1394a compatibility still required ??]*

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