

1394B B Port task group report - Houston, January 6, 1998

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To join group reflector visit www.zayante.com/p1394b and read instructions pertaining to bport task group.

1) **Padding format:** we discussed two possible formats for padding lower rate packets on higher rate ports. These were:

Bit padding: data are taken from the lower rate packet one bit data a time and placed in a higher rate byte along with the appropriate number of padding bits:

e.g. S100 packet, S800 port:

.... | pppppppd | pppppppd | pppppppd |

p=padding bit (0), d=data bit, |=byte boundary at port speed

Byte padding: data are taken from the lower rate packet one byte at a time and placed in a byte of the higher rate stream. Padding bytes are then inserted until another data byte is ready for transmission. The padding byte might in fact be represented by a control character.

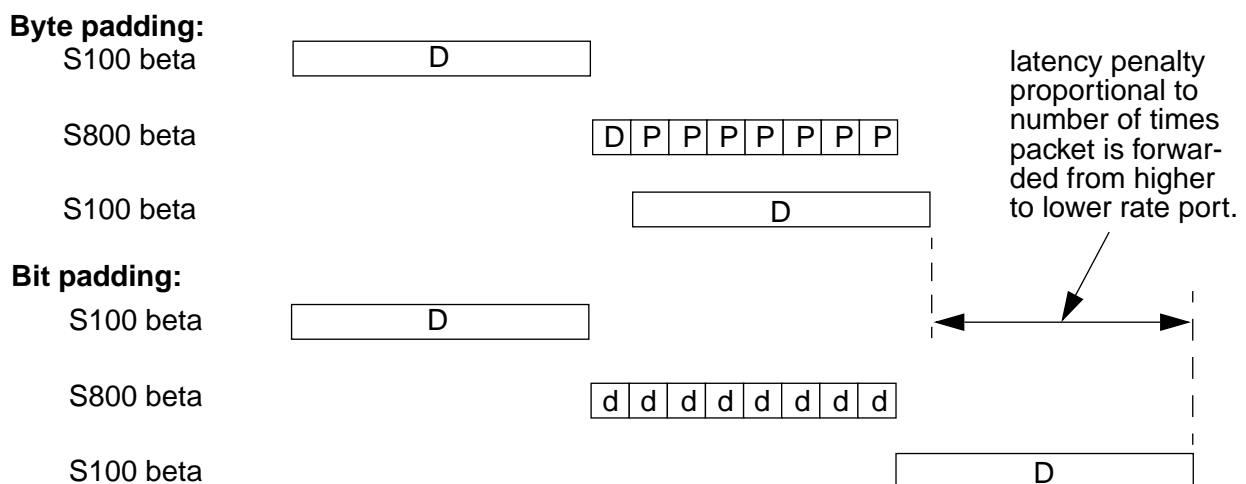
e.g. S100 packet, S800 port:

.... | D | P | P | P | P | P | P | P | D | P | P | P | P | P | P | P | D |

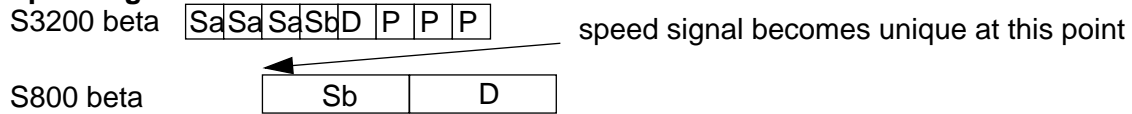
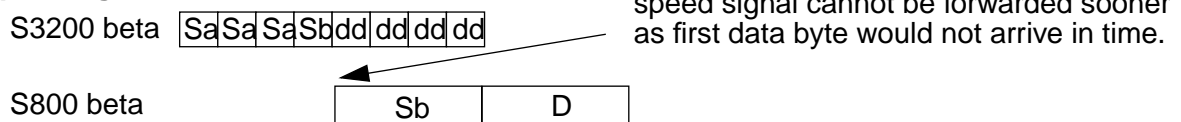
D=data byte
P=padding character

Some cases exist where the byte padding can result in lower latency:

- e.g. S100 packet sent over S100 beta link, then S800 beta link, then S100 beta link:



- e.g. S800 packet over S3200 then S800 port

Byte padding:**Bit padding:**

Conclusion: since no-one expressed any preference for bit padding, we will proceed with byte stuffing, as reflected in draft 0.06.

2) **Loop back:** we discussed the need to provide for test 'modes' within a beta PHY port. Several suggestions were made. Straightforward loopback (all data received on a port is retransmitted on the same port) was thought to be impossible due to the fact that the port's tx and rx clocks are not synchronised.

We identified a need for two types of test:

- stress test - a worst case pattern that would test PLLs at the extreme of the run length and transition density range.
- confidence test - random patterns of data and/or control signals

A test of each kind would be useful in each of two situations:

- a lab where a BERT is available to generate test patterns and analyse results.
- a plugfest where a PC would be used to generate test data and analyse results.

ACTION: Define a test method for each scenario.

3) **Error handling:** no progress to report since December's discussion, other than a data point for the level of undetected errors that might be acceptable. IDE has an error rate of 10^{-14} , which results in an undetected error 3 or 4 times per year. (Since our data rates are higher we would need to calculate the undetected error rate to achieve 3 or 4 undetected errors per year).

Next steps:

- continue email discussion
- task group will meet during February 1394B meeting in Santa Cruz.