

# Receive Equalization using Decision Feedback

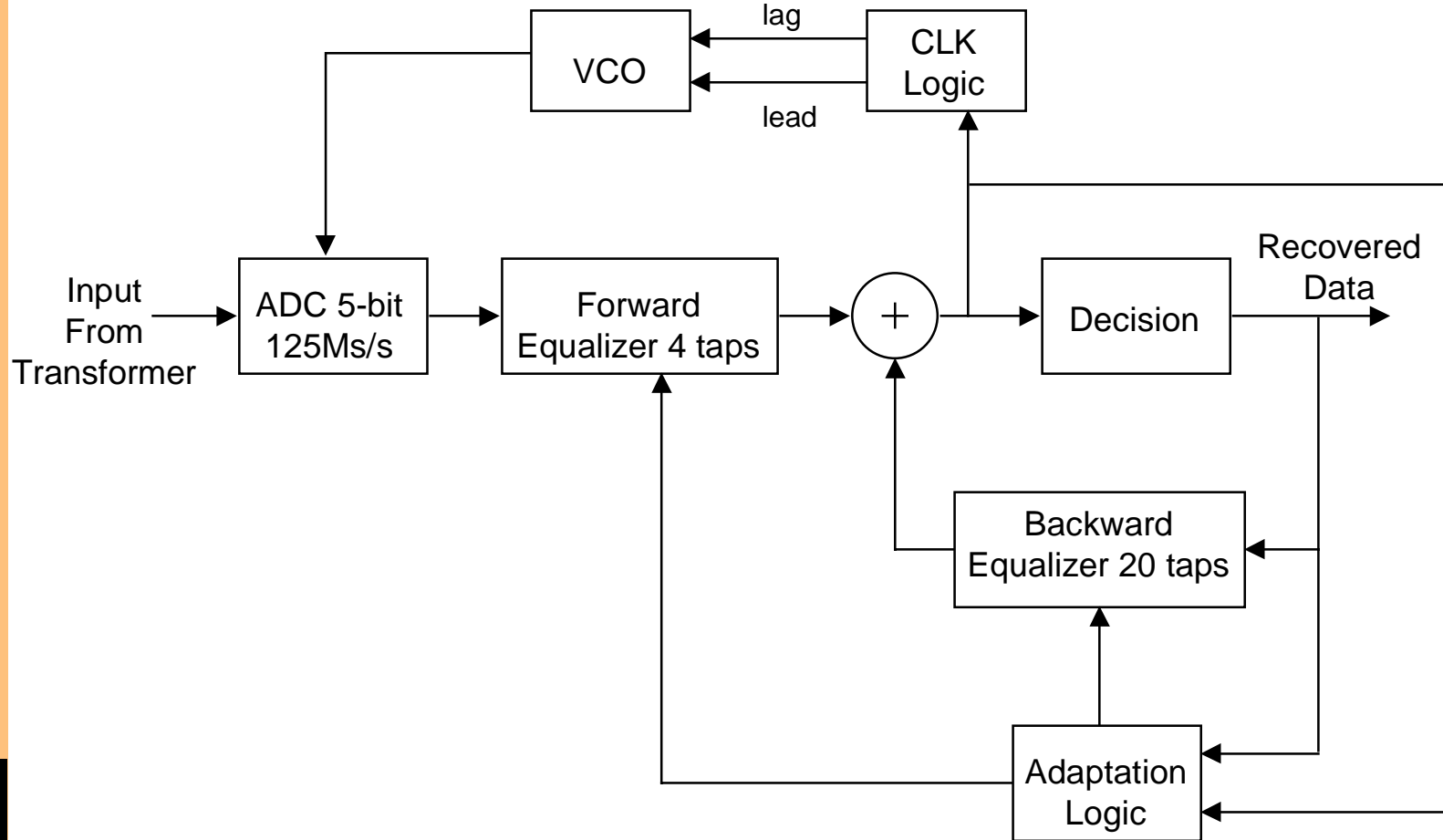
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Sept. 10, 1998

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# System Block Diagram



# Gate Counts

- Forward Equalizer - 1600 gates
- Backward Equalizer - 1800 gates
- Adder and slicer - 100 gates
- CLK recovery - 150 gates
- Adaptation logic -
  - Discrete sets of coeff. (10-16 sets) - 1500 gates
  - Continuous adaptation - 3500 gates

# Summary

- Jitter tolerance (amount of peak jitter added to the transmit signal at the transmitter while still achieving 10E-10 BER for 0 to 100 meters)
  - Discrete coeff. : +/-1.75ns minimum (estimate)
  - Continuous adaptation: +/-2.5ns worst case
- 5.2k to 7.2k gates depending upon performance target
- Much simpler clock recovery logic than edge or slicer based designs
- 4-bit ADC could also work with slightly reduced performance
- Low cost - what is 7k gates in .25 $\mu$  technology?
- Proven technology from 100Mbit Ethernet
- Better noise margin than fixed equalizers at either transmit or receive
- Detailed system simulations can be presented at next meeting