
CAT-5 P1394b Rise/Fall Time Study

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Introduction

The goal of this report is to set reasonable values for the 80% - 20% rise and fall times for CAT-5 signals in IEEE P1394b. There are several reasons for setting a maximum and minimum rise (fall) time: 1) to balance off design difficulty in both the connectors and silicon components, 2) to ensure interoperability by complete specification of the expected signals, 3) to avoid excessive radiation of EMI. Towards this goal this report presents the mathematical basis for setting the correct values.

■ Fourier Series

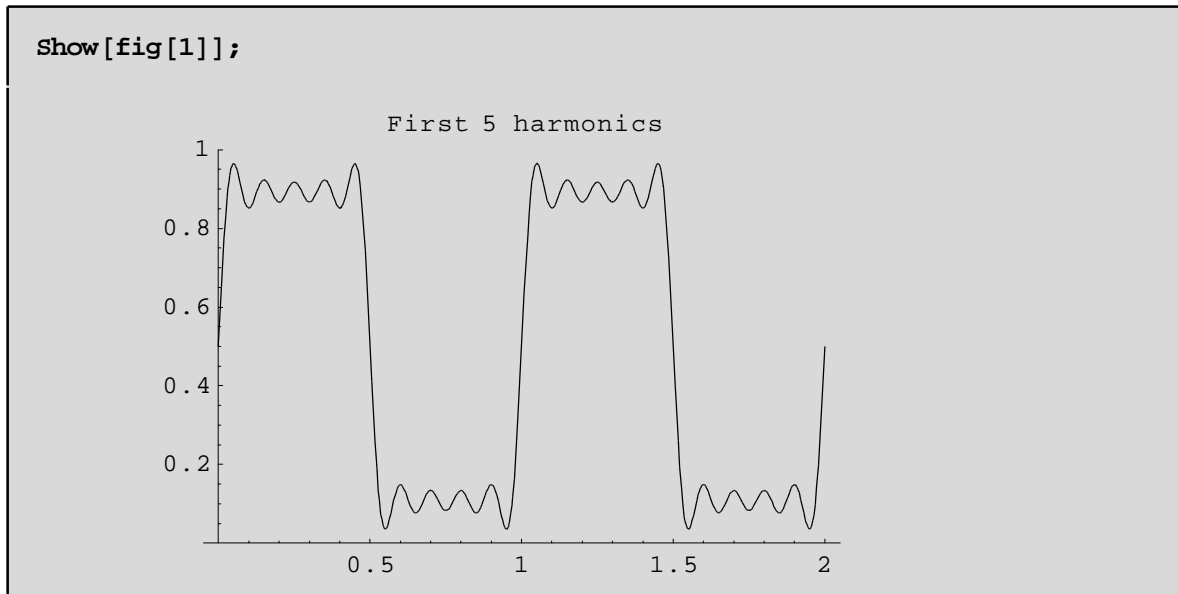
The fastest waveform we can generate onto the CAT-5 wires is an infinite series of 101010 ..., which can be defined as:

$$\text{clock waveform} = \sum_{n=0}^{\infty} \frac{\text{Sin}[2\pi(2n+1)t]}{2n+1}$$

Explicitly written out:

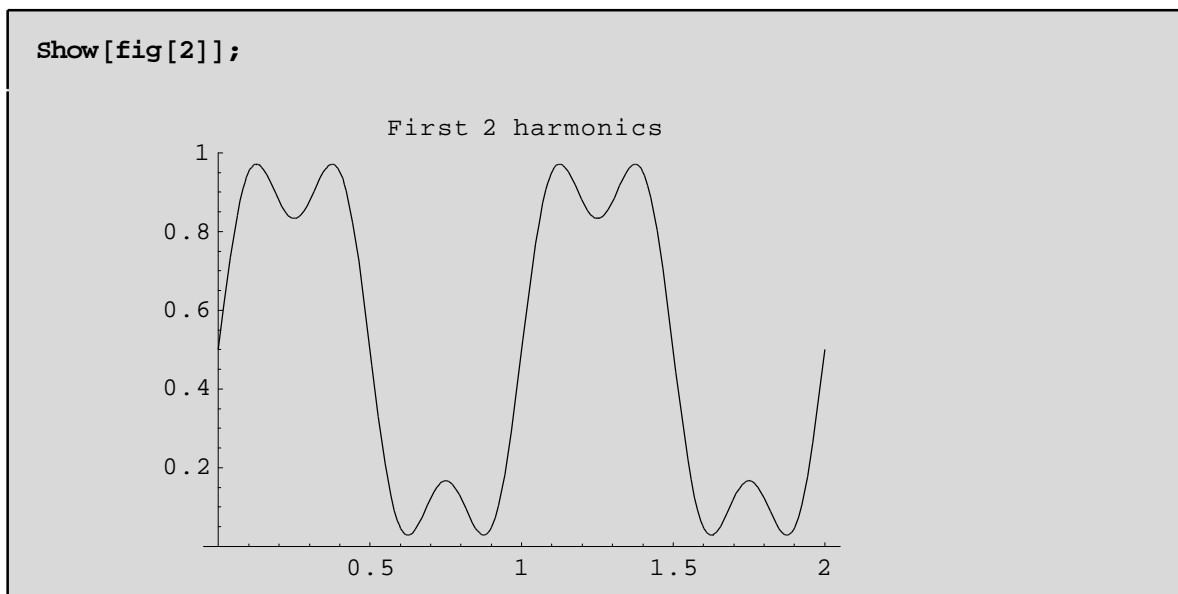
$$\text{clock waveform} = \text{Sin}[2\pi t] + \text{Sin}[6\pi t]/3 + \dots$$

If we generate a bounded number of harmonics we get:

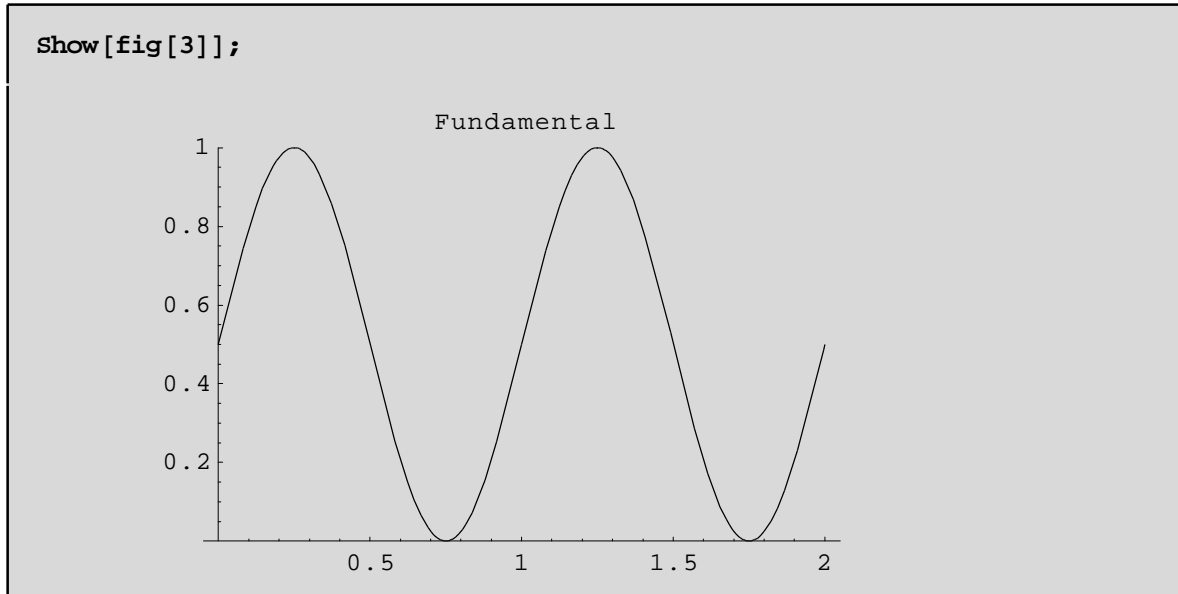


Clearly this number of Sine terms gives a waveform in time that closely approximates 101010 ..., where 1 is at 1.0 volts and 0 is 0.0 volts. As the number of terms included increases the rise/fall time of the bit edges decreases.

If we generate only the first two harmonics we get:



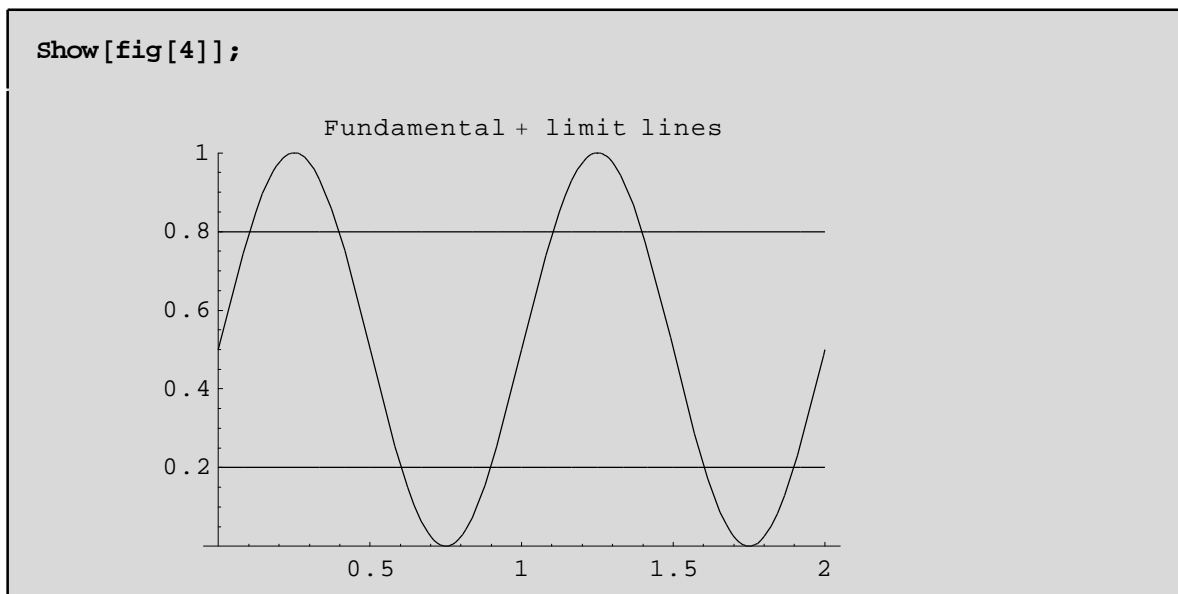
The most extreme case is to severely filter the output signal and only have the fundamental frequency present:



■ Minimum Rise Time

Rise times are measured as the amount of time it takes to rise from, say, 20% of the 1 logic level to 80% of that same level. The logic 1 level and the logic 0 level are determined by the maximum and minimum output in time from the transmitter port when running a long run of 1's and 0's. Thus for rise time logic 1 is a relative value, not an absolute voltage.

To remove excessive EMI we don't want to generate significant amounts of energy above the fundamental frequency of the clock waveform - the fastest bit pattern possible. Thus the shortest rise time should be determined by the fundamental sine wave's shape in time, i.e., the short rise time should match the rise/fall slope shape of the fundamental in the clock waveform:



Mathematically this waveform's 80-20% points are separated in time by $2 \times UI \times \text{Arcsin}[\frac{0.8-0.5}{1.0-0.5}]/\pi$, where UI is the bit duration time. For 125 MBaud this implies a rise time of 3.3 ns.

■ Maximum Rise Time

The longest rise time is determined by that value which will just trigger a worst case receiver's switching threshold under the highest case output voltage and cable length for the worst case signal, the clock waveform. The highest launch voltage is 525 mV differential and the receiver's worst case sensitivity is 50 mV differential. Again the launch voltage is measured by generating a long series of 1's and 0's.

The following matrix gives the CAT-5 cable loss specification for 100 meters length (first column is the frequency in MHz, the second column is the loss in db):

fig [5]	
0.064	0.8
0.256	1.1
0.512	1.5
0.772	1.8
1	2.5
4	4.8
10	7.5
16	9.4
20	10.5
31.25	13.1
62.5	18.4
100	23.2

The clock waveform's fundamental has a frequency of $125 \text{ MHz} / 2 = 62.5 \text{ MHz}$, thus we can expect a cable loss of 18.4 db. Given the worst case system the worst case 62.5 MHz sine wave amplitude is

$$50 \text{ mV} / 10^{-18.4/20} = 416 \text{ mV}$$

Since the biggest case launch voltage (1111 ...) is 525 mV there is room for rise time filtering to reduce the clock waveform's fundamental before the system budget is broken.

For the largest launch voltage of 525 mV the 80-20% voltage band is 315 mV. The smallest allowable clock waveform amplitude is 416 mV. Thus the longest rise time is given by the time it takes this smallest clock waveform to pass through the 315 mV voltage band:

$$\tau_{\text{rise}} = 2 \frac{\text{ArcSin}[0.315/0.416]}{2\pi \times 62.5 \text{ MHz}} = 4.37 \text{ ns}$$

■ Conclusions

Given the analysis above we have:

$$3.3 \text{ ns} \leq \tau_{\text{rise/fall}} \leq 4.4 \text{ ns}$$