

DC Biasing for IEEE P1394b Transmitters

Introduction

This white paper shows a toy driver circuit for signaling on the TpB twisted pair terminals of a bilingual P1394b PHY. The challenge is to control the common mode voltage while providing the proper differential voltage swing and while still avoiding excessive common mode excitations on the output terminals.

Circuit Context

Figure 1 shows the TpB transmitter's P1394b cable circuit:

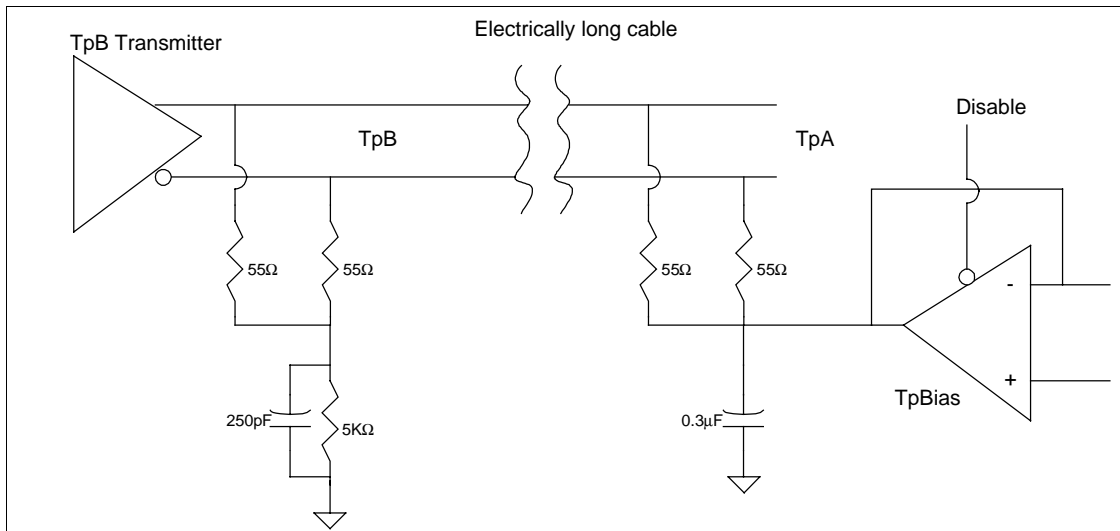


Figure 1

Circuit Assumptions

- DC biasing according to the 2.5V proposal (now obsolete)
- Tx_{cm} is between 0.9 and 1.2 volts
- Tx_{diff} is between 600 and 800 mV
- TpBias is tri-stated off to a high Z state
- This implies that $Ix_{diff} = 5.45$ to 7.27 mA,
- And $Ix_{cm} = 180$ to 240 μ A
- The cable circuit's RC time constant is $5K\Omega \times 0.3 \mu F = 1.5$ ms

The main difficulty is that the transmitter on the TpB side of the cable has no direct connection to the common mode point between the two 55 Ohms resistors. Note the TpBias directly drives this common mode point on the TpA side.

Toy Driver Circuit

(Due to a suggestion by Paul Levy)

This circuit (Figure 2) controls the differential output currents to be closely balanced and also provides an internal common mode reference voltage level for the differential signals to work off of. No attempt to accurately design sub-micron CMOS circuits is attempted here.

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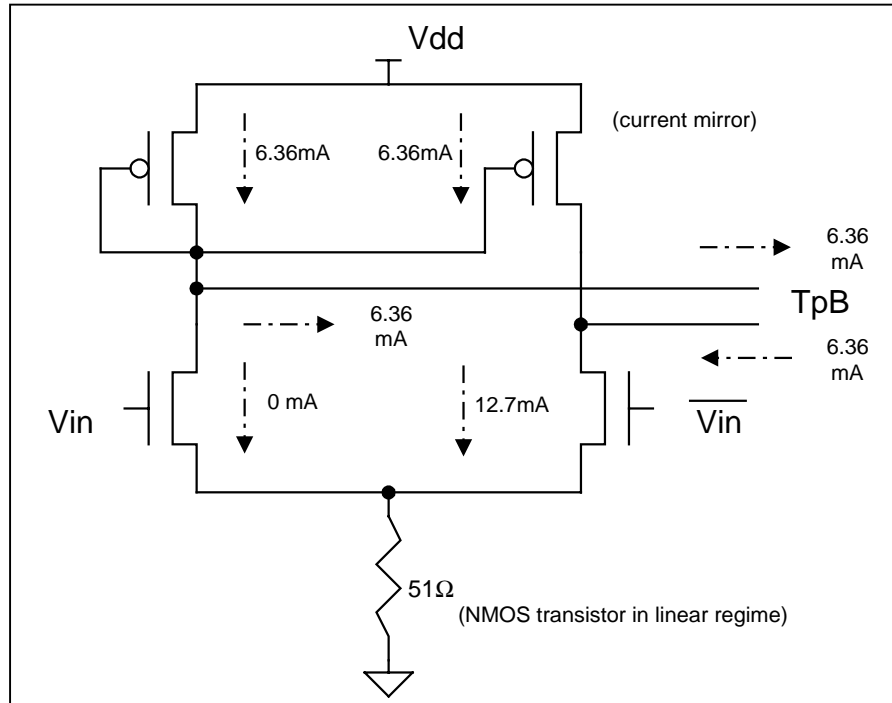


Figure 2

Circuit Assumptions

- The upper PMOS transistors are operating in the saturated regime as a symmetric current source
- The lower NMOS transistors switch between very high to very low resistance
- The lower resistor is either a resistive element or an NMOS transistor in the linear regime
- This implies that $V_{out_{lower}} = 648 \text{ mV}$

This circuit acts as a hard current path switch with carefully balanced currents in each leg of the switcher. We can use this kind of driver because the 1394 cable has resistor terminators at each end. Thus impedance matching to the cable is achieved by external components. By virtue of the hard switching and the current mirror source this circuit shows very little common mode signaling, i.e., there is a strong degree of symmetry in the magnitude of each polarity's pulse.

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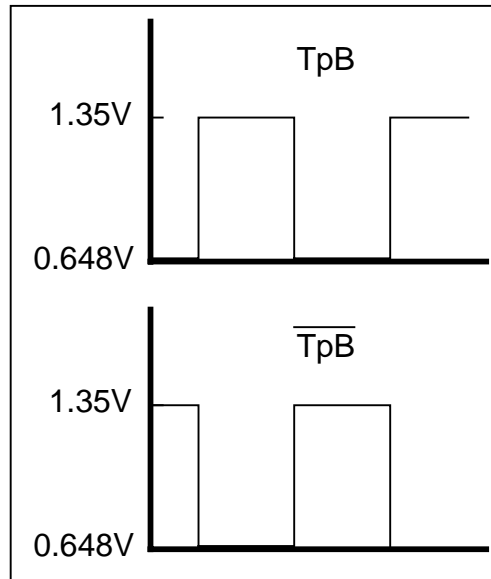


Figure 3

Figure 3 shows the voltage waveforms our driver circuit will produce. The common mode voltage will be 1.0 volts.

DC Biasing Specification (Proposed)

The sense of the last P1394b meeting was that we should have only two biasing conditions. The first requires 3.3V logic and is required for bilingual mode operations. The second is for beta only operation and allow interoperability between DC coupled PHYs that operate from 2.5V down to 1.8V.

Parameter	Bilingual Operation	Beta only Operation	Units
	3.3 volt supply	2.5 --1.8 volt supply	
Supply voltage tolerance	+/- 10%	TBD	
Transmitter common mode voltage range	1.4 - 1.7	0.7 - 1.0	volts
Transmitter high voltage	2.1	1.4	volts
Transmitter low voltage	1.0	0.3	volts
Receiver common mode voltage range	0.9 - 2.1	0.7 - 1.0	volts
Receiver high voltage	2.6	1.4	volts
Receiver low voltage	0.5	0.3	volts