12. 1394b PHY – Link interface specification

This section specifies the signalling, protocol & electrical characteristics of the PHY-Link interface. The interface is described independently of other operational characteristics of either PHY or Link devices. The PHY-Link interface specifies a point-to-point communications mechanism between a single 1394b Link and PHY device for the purpose of transfer of 1394 packet and status information between these two devices.

Implementation of the PHY-Link interface at speeds up to S800 may be achieved by using a 8-bit parallel interface which is closely modelled on the existing interface defined in IEEE 1394a-1999. The parallel interface describes mechanisms to support communication between discrete PHY & Link devices at speeds of S100, S200, S400 & S800. For all of these cases, the interface pinout is identical. Lower transfer speeds than the maximum are accommodated by data padding/repetition.

The parallel 1394b PHY-Link interface is an evolution of the interface specified in the IEEE 1394-1995 & associated 1394a-1999 standards. The 1394b interface is a superset of the signals defined in those standards, and supports the operation of 1394a-compliant links. In this mode of operation, the complete set of functionality provided by the 1394b PHY will not be available. The purpose of this backwards-compatibility is to provide a migration path for existing 1394a Link applications.

Implementation of the PHY-Link interface at all speeds, including speeds in excess of S800, may be achieved using a serial data interface closely related to the serial port specification in 1394b. Such operation may be supported by using an integrated PHY and Link, communicating by means of an internal interface whose specification is beyond the scope of this standard, which would then communicate with an external PHY via a standard 1394b serial bus connection supplemented with the PHY-Link control signals. The characteristics of such a mode of connection are described later in this chapter as a modification of the parallel interface.

12.1 1394b PHY-Link Interface Characteristics

The following are the characteristics of the 1394b PHY-Link interface

- provides for bi-directional 1394 packet data transfer at S100, S200, S400 & S800 speeds on the parallel interface, and up to S3200 on the serial interface
- provides a mechanism for status information transfer from the PHY to the Link
- provides a mechanism for the Link to access a register space within the PHY
- provides a means for the Link to request services from the PHY
- provides a means for the PHY to interrupt the Link during an operation
- supports an optional isolation interface to allow separate PHY & Link device power supply domains
- supports operation by a 1394a-compliant link device
- supports a minimum distance of 20 cm between PHY & Link discrete devices using the parallel interface

12.2 Parallel 1394b PHY to 1394b Link Interface Pinout

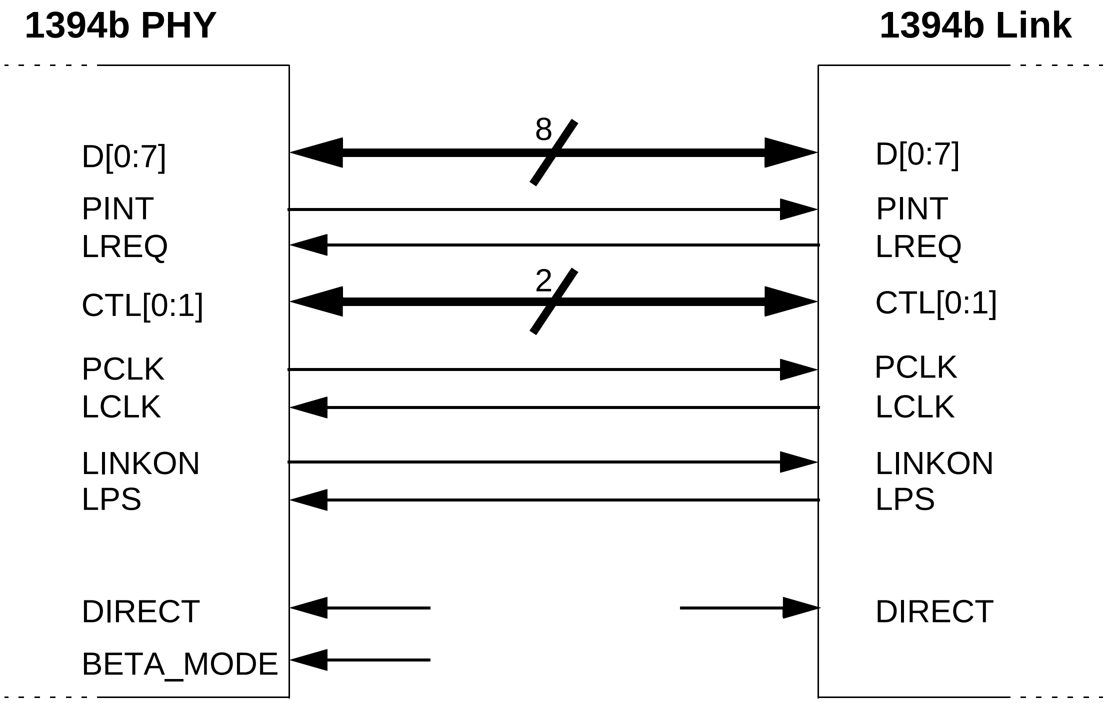

Figure 12-1—PHY-Link Interface Logical Signalling

NOTE—this diagram indicates the logical signalling required between the PHY & Link devices and does not imply a DC connection between the two devices.

12.2.1 Interface Signal Descriptions

The signals of the 1394b PHY-Link interface for devices implementing the parallel interface are divided into mandatory and optional signals for the PHY & Link devices.

12.2.1.1 PHY Device Signals

The mandatory signals for the PHY device are D[0:7], PINT, LREQ, CTL[0:1], PCLK, LCLK, LINKON & LPS. These signals shall be implemented by all PHY devices adhering to this specification. The DIRECT & BETA_MODE signals are optional for the PHY device. PHY devices that implement these signals shall do so in accordance with this specification.

12.2.1.2 Link Device Signals

The mandatory signals for the Link device are D[0:7], PINT, LREQ, CTL[0:1], PCLK & LCLK. These signals shall be implemented by all Link devices adhering to this specification. The LINKON, LPS & DIRECT signals are optional for the Link device. Link devices that implement these signals shall do so in accordance with this specification.

The following table describes the PHY-Link interface signals in brief.

Table 12-1— PHY-Link Interface Signal Descriptions

Signal Name	Direction	Description
D[0:7]	Bidirectional	PHY-Link interface data bus. Mandatory 8-bit databus for all 1394b compatible PHY & Link devices
PINT	PHY Drives	PHY Interrupt. Mandatory PHY to Link interrupt & status indication
LREQ	Link Drives	Link Request. Mandatory Link to PHY request
CTL[0:1]	Bidirectional	PHY-Link Control bus. Mandatory 2-bit control bus for all 1394b compatible PHY & Link devices
PCLK	PHY Drives	PHY Sourced Clock. Mandatory PHY to Link interface clock
LCLK	Link Drives	Link Sourced Clock. Mandatory Link to PHY interface clock
LINKON	PHY Drives	Link On. Mandatory for the PHY, optional for the Link device
LPS	Link Drives	Link Power Status. Mandatory for the PHY, optional for the Link device
DIRECT	Externally Driven	Direct. Optional external indication of the connection type between PHY & Link
BETA_MODE	Externally Driven	PHY-Link Interface Mode. Optional external indication of the PHY-Link interface mode

12.2.1.3 Detailed Signal Descriptions

- D[0:7] - Data. This databus is used to carry 1394 packet data, packet speed and grant type information between the PHY and the Link. This is a bidirectional databus. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, data on this bus is synchronous to the PCLK source clock. When driven by the Link device, data on this bus is synchronous to the LCLK source clock.
- PINT - PHY Interrupt. This signal is always driven by the PHY. The serial information on this signal is used by the PHY to transfer status, register, interrupt and other information to the Link. The data on this signal is synchronous to the PCLK source clock.
- LREQ - Link Request. This signal is always driven by the Link. The serial information on this signal is used by the Link to request packet transmission, to read and write PHY registers, and to indicate the occurrence of certain Link events that are relevant to the PHY. The data on this signal is synchronous to the LCLK source clock.
- CTL[0:1] - Control. This is a bidirectional control bus between the PHY and the Link. It is used to indicate the phase of operation of the interface. Upon a reset of the interface, this bus is driven by the PHY device. When driven by the PHY device, information on this bus is synchronous to the PCLK source clock. When driven by the Link device, information on this bus is synchronous to the LCLK source clock.
- PCLK - PHY Clock. This signal is always driven by the PHY device. Following an interface reset or after power-on reset, this signal shall be a nominal 98.304 MHz clock with a nominal 50% duty cycle. The PHY device shall be an original provider of the interface source clock i.e. the PHY shall not derive its PCLK signal from the incoming LCLK signal.
- LCLK - Link Clock. This signal is always driven by the Link device. The Link device shall derive its LCLK output from the incoming PCLK signal. In this way, PCLK & LCLK are frequency-locked, but not phase-locked

- LINKON - Link On Event Notification. This signal is always driven by the PHY device. This signal is used to provide notification to a Link device of a received Link-On PHY packet by the PHY.
- LPS - Link Power Status Notification. This is an input signal to the PHY device. This signal is used to provide notification to a PHY device of the powered status of the Link. If this signal indicates that the Link device is powered, the Link shall be capable of maintaining communications over the PHY-Link interface as specified in this standard.
- DIRECT - Direct Connection Notification. This signal is an input to both PHY & Link devices. If DC isolation is supported, this signal is required and is asserted to indicate that the PHY and Link devices are directly connected to each other i.e. a DC connection exists between both devices.
- BETA_MODE - PHY-Link Mode Indication. If not provided, or if provided and asserted, the PHY-Link interface complies with this specification. When provided but deasserted, the PHY-Link interface complies with the 1394a specifications.

12.3 General Interface Characteristics

[Rework, and move to Chapter 4 (P1394b introduction)]

The operation of the PHY-Link interface is an evolution of the IEEE 1394-1995 & 1394a interface specifications.

Mechanisms are put in place to provide new functionality which is specific to 1394b. The interface is specified as being more symmetrical, in order to avoid any dead-lock or long latency situations where either the Link or PHY device cannot establish communications with the other while a lengthy operation is taking place.

In general, the PHY device is the owner of the PHY-Link interface. All 1394 bus packets are transferred to the Link device as they are received. The Link requests the use of the Serial bus via the PHY device. The PHY interprets and queues the Link transmit requests as appropriate. When the PHY is granted access to the bus, the PHY passes that grant to the Link which then transmits data as required.

From a functional point of view, the PHY-Link interface can be viewed as a master-slave interface. At any point in time, either the PHY or the Link is the current owner of the interface, and a handover mechanism to pass ownership from one to the other is defined.

12.4 Interface Initialization & Reset

[Ed, this may need a small amount of updating to be consistent (copy of) 1394a].

The LPS input, used to indicate the powered status of the Link, is also used to request the PHY to disable or enable the PHY-Link interface. The output characteristics of LPS, if provided by the Link, depend upon the interface mode, differentiated or undifferentiated. When the interface mode is differentiated, LPS shall be a pulsed output while logically asserted. When logically deasserted, LPS shall be driven low in either interface mode.

The characteristics of LPS are specified by Figure 12-2 and Table 12-2.

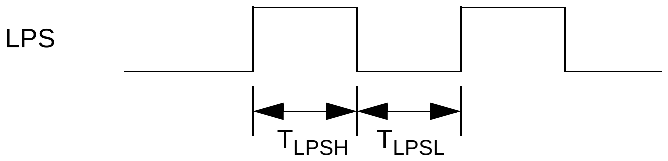

Figure 12-2—LPS waveform when differentiated

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Table 12-2—LPS Timing parameters

Parameter	Description	Unit	Minimum	Maximum
T_{LPSL}	LPS low time (when pulsed)	µs	0.09	1.00
T_{LPSH}	LPS high time (when pulsed)	µs	0.09	1.00
T_{LPS_RESET}	Time for PHY to recognize LPS logically deasserted and reset the interface	µs	1.2	2.75
$T_{LPS\_DISABLE}$	Time for PHY to recognize LPS logically deasserted and disable the interface	µs	25	30
$T_{RESTORE}$	Time to permit the optional differentiator and isolation circuits to restore during an interface reset	µs	15	20[a]

[a] This maximum does not apply when the PHY-Link interface is disabled (see Figure 12-4), in which case an indefinite time may elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface it is necessary that the Link ensure that LPS is logically deasserted for less than $T_{LPS\_DISABLE}$.

The Link requests the PHY to reset the interface by deasserting LPS. Within $T_{LPS\_RESET(min)}$ after it deasserts LPS, the Link shall place CTL[0:1] and D[0:7] in a high-impedance state and condition LREQ & LCLK according to the interface mode: if undifferentiated, LREQ & LCLK shall be driven zero otherwise they shall be placed in a high-impedance state.

If the PHY observes LPS logically deasserted for T_{LPS_RESET}, it shall reset the PHY-Link interface. The voltage levels shown in Figure 12-3 for CTL[0:1], D[0:7], PINT and LREQ while LPS is logically deasserted are accurate only for an undifferentiated interface, but the timing relationships remain accurate for both modes. When the interface is undifferentiated, the PHY drives CTL[0:1], D[0:7] & PINT to zero. Otherwise, the PHY places the CTL[0:1], D[0:7] & PINT signals in a high-impedance state.

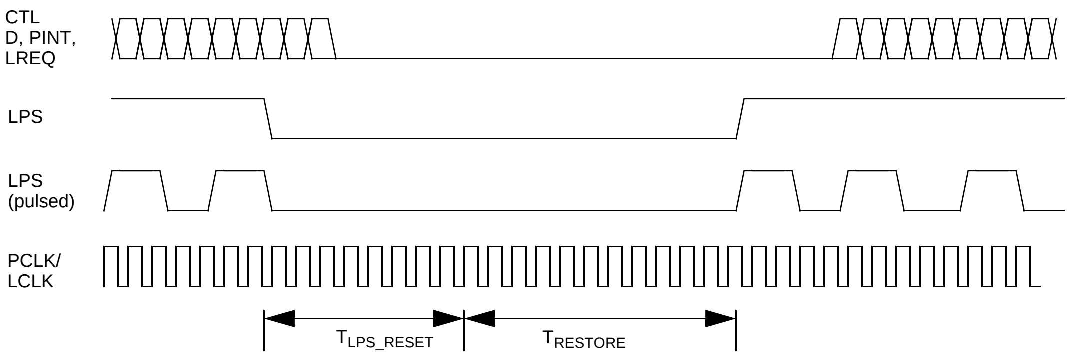

Figure 12-3—PHY-Link interface reset *via* LPS

If the Link continuously deasserts LPS for a longer period, it requests the PHY not only to reset but also to disable the PHY-Link interface. The Link shall condition its outputs as already described for reset.

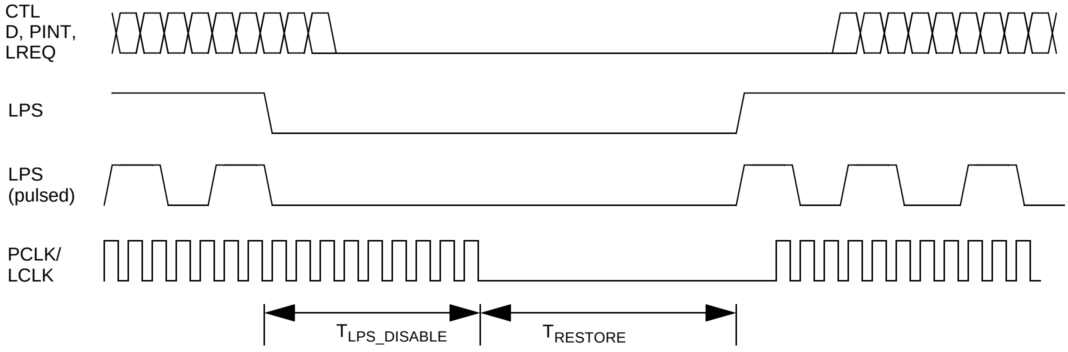

Figure 12-4—PHY-Link interface disable *via* LPS

If the PHY observes LPS logically deasserted for $T_{LPS\_DISABLE,}$ it shall disable the interface. The PHY has already reset the interface as described above; it now disables the interface by stopping PCLK. The voltage levels shown in Figure 12-4 for CTL[0:1], D[0:7], PINT, LREQ and PCLK while LPS is logically deasserted are accurate only for an undifferentiated interface, but the timing relationships remain accurate for both modes. When the interface is undifferentiated, the PHY disables the interface by driving PCLK to zero while continuing to drive CTL[0:1], D[0:7] & PINT to zero. Otherwise, the PHY disables the interface by placing PCLK in a high-impedance state while continuing to maintain the CTL[0:1], D[0:7] & PINT signals in a high-impedance state.

NOTE—When the PHY-Link interface is disabled and none of the PHY's ports are active or in a transitional state, the PHY may place most of its circuitry in a low power state.

When the PHY-Link interface is reset, the PHY shall cancel any outstanding bus or register read requests. Although the cancellation of bus requests may affect PHY arbitration status in ways not described in other parts of this specification, the PHY's behaviors (as observable from Serial Bus) shall be consistent with those sections. For example, the PHY may have initiated arbitration in response to a bus request but reset of the PHY-Link interface might cancel the request before it is granted. Appropriate PHY behavior would be either the transmission of a null packet or the removal of the arbitration request before it is granted.

This specification describes the PHY's operation as if the interface to the Link is always operational. If the PHY-Link interface is reset while the Link is transmitting a packet, the PHY shall behave as if the Link had signaled IDLE and terminated the packet. Similarly, any status bit information generated by the PHY while the interface is disabled shall be zeroed and shall not cause a status transfer upon restoration of the interface.

The handshake just described either resets, or resets and then disables the interface when the Link deasserts LPS for T_{LPS_RESET} or $T_{LPS\_DISABLE}$ respectively. In either case (or after power reset), normal operations may be restored if the Link asserts LPS. After observing LPS, if PCLK is not already provided by the PHY, it shall resume PCLK as soon as possible. If the PHY-Link interface is differentiated and PCLK is resumed, the PHY shall commence by driving PCLK low for a minimum of 5ns. In either mode, the PHY shall ensure that clock duty cycle and period requirements are met from the first rising edge of PCLK onwards. Once PCLK is available the PHY and Link shall condition their CTL[0:1] and D[0:7] outputs in accordance with Table 12-3 . The reference point is the first rising edge of PCLK after LPS is asserted.

Table 12-3—Initialization of the PHY-Link interface

Device	Interface mode	
	Differentiated	Undifferentiated
PHY	For one and only one of the first six cycles of PCLK after the reference point, drive CTL[0:1], D[0:7] & PINT to zero and otherwise, for these cycles and the seventh, place them in a high-impedance state	Continue to drive CTL[0:1], D[0:7] & PINT to zero for the first seven cycles of PCLK after the reference point
Link	For one and only one of the first six cycles of PCLK after the reference point, drive CTL[0:1], D[0:7] and LREQ to zero and otherwise place them in a high-impedance state.	For one and only one of the first six cycles of PCLK after the reference point, drive CTL[0:1], D[0:7] and LREQ to zero; prior to this place them in a high-impedance state. Once these signals have been driven low, return CTL[0:1] and D[0:7] to a high-impedance state but continue to drive LREQ low until after the reset completes

NOTE—The PHY may not be able to determine its operating mode, differentiated or undifferentiated, during power reset. While the operating mode is indeterminate, the PHY shall place its outputs in a high-impedance state. The PHY shall not provide PCLK until the operating mode is determined and the PHY-Link interface is operational.

Upon the eighth PCLK cycle the PHY shall assert RECEIVE on CTL[0:1] while simultaneously providing data prefix indication on D[0:7] for at least one PCLK cycle. Upon the subsequent PCLK cycles the PHY shall continue to indicate data prefix while it is in a state in which it otherwise would be transferring data to the Link, after which it shall assert IDLE on CTL[0:1] & zero on D[0:7].

The Link may examine CTL[0:1] once it has driven CTL[0:1], D[0:7] and LREQ to zero for one cycle subsequent to the PCLK reference point. When the Link simultaneously observes RECEIVE on CTL[0:1] and data prefix on D[0:7] and subsequently observes IDLE on CTL[0:1], the reset of the PHY-Link interface is complete. No more than 10ms shall elapse from the reassertion of LPS until the interface is reset. The link shall not assert LREQ until the reset is complete.

12.5 Link-On Indication

[May need editing to latest 1394a spec]

The PHY LINKON output provides a method for the PHY to signal the Link at times when the Link is not active. The Link is inactive when either the LPS signal is logically deasserted (see clause 12.4) or the PHY register Link_active bit is zero. The characteristics of the LINKON signal, specified by Table 12-4, permit the Link to detect LINKON in the absence of PCLK and also permit the signal to cross an optional isolation barrier. When LINKON is logically deasserted it shall be driven low.

Table 12-4—LINKON timing parameters

Description	Unit	Minimum	Maximum
Frequency	MHz	4	8
Duty cycle	%	40	60
Persistence Time, measured from the point at which both LPS is active and Link_active is one, after which the PHY shall not continue to signal LINKON	ns		500

When either LPS is logically false or the PHY register Link_active bit is zero, a PH_EVENT.indication of LINK_ON shall cause the assertion of LINKON. This signal shall persist so long as the logical AND of the LPS signal and Link_active is zero.

At other times (when the Link is active), a PH_EVENT.indication of LINK_ON shall be communicated to the Link by the transfer of the link-on packet that caused the event. The PHY shall not assert LINKON if the Link is already active.

The LINKON signal is also used to provide interrupt notification to an inactive Link. When any of the PHY register bits Loop, Pwr_fail, Timeout or Port_event is one and either LPS is logically false or the PHY register Link_active is zero, the PHY shall assert LINKON. The PHY shall continue to assert LINKON so long as the Link remains inactive.

12.6 Link Requests & Notifications

The Link makes requests to the PHY to

- request asynchronous packet transmit services (other than Cycle Start)
- request a Cycle Start packet transmit service
- request isochronous packet transmit services
- request PHY register read/write operations

The Link issues notifications to the PHY to inform it of Link events that are relevant to its operation.

Link requests, once issued, cannot be explicitly cancelled. The PHY is not required to maintain an internal queue of requests. Thus, only a single asynchronous bus request and a single isochronous bus request may be outstanding within the PHY. If a Link wishes to effectively cancel an outstanding request, it shall abdicate its transmit opportunity when the PHY issues the relevant GRANT (see clause 12.7.1 for details)

12.6.1 Asynchronous Packet Transmit Requests (other than Cycle Start)

Both Link & PHY devices recognize the existence of a current fairness interval phase, either ODD or EVEN. The fairness interval phase is used to allow the Link to pipeline asynchronous transmit requests to the PHY. If the current fairness interval phase is EVEN, the Link may issue an asynchronous transmit request for the current phase or for the ODD phase,

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and shall not issue an asynchronous transmit request for the EVEN phase. If the current fairness interval phase is ODD, the Link may issue an asynchronous transmit request for the current phase or for the EVEN phase, and shall not issue an asynchronous transmit request for the ODD phase.

The PHY device provides notification of a fairness interval phase change via the appropriate Arbitration Reset status transfer (see Table 12-16). Upon receipt of this status transfer, the Link updates its current fairness interval phase. After an interface reset (or after power-on reset) the fairness interval phase shall be EVEN.

The Link may only have one asynchronous transmit request outstanding at any time. If a new asynchronous transmit request is issued by the Link, this is deemed to supersede the previous request. In this way, if a Link has issued a request for the next fairness interval (EVEN or ODD), and then determines that it has further information to transfer within the current fairness interval, it may issue a new current asynchronous request. This new request supersedes the request for the next fairness interval, which must be re-issued by the Link when appropriate.

There is sufficient information in the asynchronous grant issued by the PHY to the Link in order for the Link to determine which request is being granted by the PHY.

Link asynchronous transmit requests may be made at any time. The Link request includes the requested packet speed.

12.6.2 Cycle Start Transmit Requests

The Link uses Cycle Start transmit requests to indicate to the PHY that it requires to send a Cycle Start packet out on Serial Bus. The Link may issue a Cycle Start transmit request at any time. If the Link has already made a Cycle Start transmit request, further Cycle Start transmit requests supersede the current Cycle Start transmit request. The Link Cycle Start request includes the requested packet speed.

12.6.3 Isochronous Packet Transmit Requests

The Link uses isochronous transmit requests to indicate to the PHY that it has isochronous data ready for transmission as part of the isochronous period. The Link can issue isochronous requests for either the current or ODD/EVEN isochronous period. In the same manner as for asynchronous requests, only one isochronous Link transmit request need be stored by the PHY. Any new isochronous request supersedes the previous one.

There is sufficient information in the isochronous grant issued by the PHY to the Link in order for the Link to determine which request is being granted by the PHY.

The Link may issue isochronous transmit requests at any time. The Link request includes the requested packet speed.

12.6.4 PHY Register Read/Write Requests

The Link uses PHY register read & write requests to gain access to the PHY device’s internal register space. The PHY address space is addressable via a 4-bit address, allowing for 16 directly addressable register locations, each a single byte.

The Link issues a PHY register read request to instruct the PHY to return the contents of one of its internal registers via a status transfer. The Link specifies the PHY address as part of the request. The Link shall not issue a further PHY register read request until the first has been completed via a status transfer. The PHY shall ignore further PHY register read requests until the first has been completed. PHY register reads may be initiated at any time.

The Link issues a PHY register write request to write new contents to one of the PHY’s internal registers. The Link supplies the PHY register address and the write data as part of the request. The PHY shall write the data content immediately to the appropriate PHY register. PHY register writes may not be initiated by the Link while a PHY register read is pending. Any PHY register write which is issued while a register read is pending is ignored by the PHY.

12.6.5 Link Notifications

The Link issues notifications to the PHY Device to inform it of events that have been observed that are relevant to the PHY's operation.

The only Link notification currently defined is a notification to the PHY that a Cycle Start packet has been received by the Link. The Link passes this information to the PHY to allow it to correctly perform border functionality.

12.6.6 Miscellaneous Link Requests

The Link makes a number of miscellaneous requests to the PHY to request an interface reset or to select the appropriate mode of packet transmission to be used to future packets.

Transmit Requests by the Link to the PHY may be interpreted as either Beta-only requests, indicating that the Link has sufficient information to believe that the entire packet path from source to destination will be via Beta-capable nodes, or as Legacy-only requests, indicating that the Link does not have sufficient information to determine this. The Link issues a Select Beta-Only request to the PHY to indicate that further transmit requests should use the Beta-only format, and issues a Select Legacy-Only request to indicate that further transmit requests should use the Legacy format. Upon interface reset, the Legacy-Only mode of operation is in effect.

12.6.7 Link Request Format

The Link uses the following defined format to issue requests and notifications to the PHY device. Link requests and notifications are issued serially over the LREQ interface pin. The Link request begins with a START bit (always a '1'), followed by a 4-bit Link request type field. Depending on the Link request type, there may be a following 4-bit address and 8-bit data field. The Link request is completed with an END bit (always a '0'). Following the END bit, another Link request may be issued immediately.

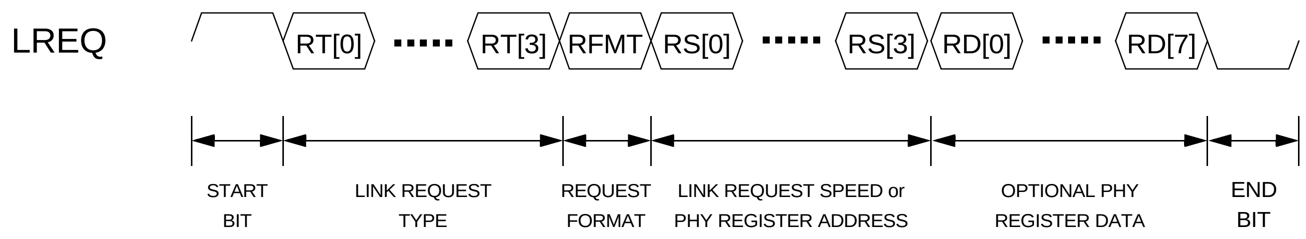


Figure 12-5— Link Request Format

NOTE—each cell in the Link Request Format represents one LCLK cycle time

12.6.7.1 Beta-Only Link Requests

If the Link has prior knowledge that the entire packet transmission path from source node to destination node traverses only Beta-capable nodes, it may issue a transmit request requesting the PHY to use the Beta packet format. This request is accomplished by setting the RFMT (Request Format) bit as part of the LREQ request stream.

If the Link does not have knowledge that the entire packet transmission path is via all Beta-capable nodes, then it shall not explicitly request the PHY to use the Beta-only format. This is accomplished by resetting the RFMT bit as part of the LREQ request stream. Note that in this case, it may be possible for the PHY to have determined for itself that the transmission path is via Beta-only nodes, in which case it will use the Beta packet format.

Table 12-5—Link Request Type Encoding

RT[0:3] Value	Name	Meaning	Required Fields
0000	Reserved.	Reserved. The Link shall not transmit a request using this value	None
0001	IMMEDIATE	Used by the Link to request immediate access to the Serial Bus (generally used for transmission of an acknowledge packet)	Request Format, Request Speed
0010	CURRENT_ASYNC	Used by the Link to request transmission of an asynchronous packet in the current fairness interval	Request Format, Request Speed
0011	EVEN_ASYNC	Used by the Link to request transmission of an asynchronous packet in the even fairness interval phase	Request Format, Request Speed
0100	ODD_ASYNC	Used by the Link to request transmission of an asynchronous packet in the odd fairness interval phase	Request Format, Request Speed
0101	CURRENT_ISOCH	Used by the Link to request transmission of an isochronous packet in the current isochronous period	Request Format, Request Speed
0110	ODD_ISOCH	Used by the Link to request transmission of an isochronous packet in the next Odd isochronous period	Request Format, Request Speed
0111	EVEN_ISOCH	Used by the Link to request transmission of an isochronous packet in the next Even isochronous period	Request Format, Request Speed
1000	CYCLE_START	Used by the Link to request transmission of a cycle start packet	Request Format, Request Speed
1001	RESET	Used by the Link to request that the PHY-Link interface be reset, causing any current operation to be terminated and all outstanding requests to be cancelled	None
1010	REGISTER_READ	Used by the Link to request the contents of one of the PHY device’s internal registers	Register Address
1011	REGISTER_WRITE	Used by the Link to write new contents to one of the PHY device’s internal registers	Register Address & Data
1100	Not Used	Not Used	-
1101	Not Used	Not Used	-
1110	Not Used	Not Used	-
1111	CYCLE_ST_DET	Used by the Link to indicate to the PHY that a cycle start packet has been correctly received	None

Table 12-6—Link Request Format Encoding

RFMT Value	Meaning
0	The Link is not explicitly requesting that the PHY use either Beta or Legacy packet format for packet transmission
1	The Link is explicitly requesting that the PHY use the Beta packet format for packet transmission

Table 12-7—Link Request Speed Encoding

RS[0:3] Value	Meaning
0000	S100
0001	S1600[a]
0010	S200
0011	S3200[a]
0100	S400
0101	Reserved
0110	S800
0111-1111	Reserved

[a] these speeds are not defined for transmission over the discrete PHY-Link interface

For PHY Register Read & Write operations, the RS[0:3] value represents a PHY device register location.

For PHY Register Write operations, the RD[0:7] value represents the data to be written to the PHY device register.

The Link issues a Cycle Start Notification to the PHY after receiving a correctly formatted Cycle Start packet.

12.7 PHY-Link Interface Data Phases

The PHY-Link interface defines a number of phases of operation in order to complete data transfers from the PHY to the Link and vice versa. These phases should all be easily identifiable in real time, while retaining the use of a minimum of control pins. This is achieved by using a particular state encoding on the control lines, which allows the current state of the interface to be readily determined by looking at the current values on the control lines in conjunction with previous values on these lines.

The data operations which are carried out over the PHY-Link interface are

- 1394 Packet Transmit (data transferred from Link to PHY device)
- 1394 Packet Receive (data transferred from PHY to Link device)

NOTE— the transfer of status information from PHY to Link is accomplished over the PINT signal line.

The current phase of the PHY-Link interface is indicated by the CTL[0:1] signal lines, encoded as in the following tables

Table 12-8—CTL[0:1] encoding when the PHY is driving

CTL[0]	CTL[1]	Interface Phase	Phase Description
0	0	IDLE	The PHY has no information to transfer to the Link
0	1	Reserved	Reserved. The PHY shall not generate this CTL pattern
1	0	RECEIVE	The PHY is transferring packet information to the Link
1	1	GRANT	The PHY is indicating that it is handing the interface over to the Link

Table 12-9—CTL[0:1] encoding when the Link is driving

CTL[0]	CTL[1]	Interface Phase	Phase Description
0	0	IDLE	The Link has completed packet transmission and is handing the interface back to the PHY
0	1	TRANSMIT	The Link is transmitting packet information to the PHY
1	0	Reserved	Reserved. The Link shall not generate this CTL pattern
1	1	HOLD/ PACKET_END	When asserted at the start of a packet transmission, indicates that the Link is holding the PHY-Link interface while it is preparing data for transmission; when asserted at the end of a packet transmission, indicates that D[0:7] contains information on the packet being completed, and possibly an embedded Link request for another packet transmission

Note that weak pulldowns are present on the CTL[0:1] & D[0:7] pins of the PHY-Link interface when DC coupled in order that the CTL[0:1] & D[0:7] lines assume/hold an IDLE state whenever neither PHY nor Link device is driving the interface.

12.7.1 1394 Packet Transmit Operation

When the Link device has requested access to the Serial Bus via the LREQ signal, the PHY device performs an arbitration. When access to the Serial Bus has been granted to the PHY, the PHY propagates this grant to the Link device. The Link device then assumes ownership of the interface data and control buses. The Link device may transmit bus holding symbols while it prepares data for transmission. The Link then transmits 1394 packet data until such time as it has completed its packet transmit operation. Once the Link device has commenced transmitting 1394 packet information, it must continue to do so in consecutive PHY-Link interface bus cycles until transmission is complete.

The packet transmission operation is described in the following timing diagram

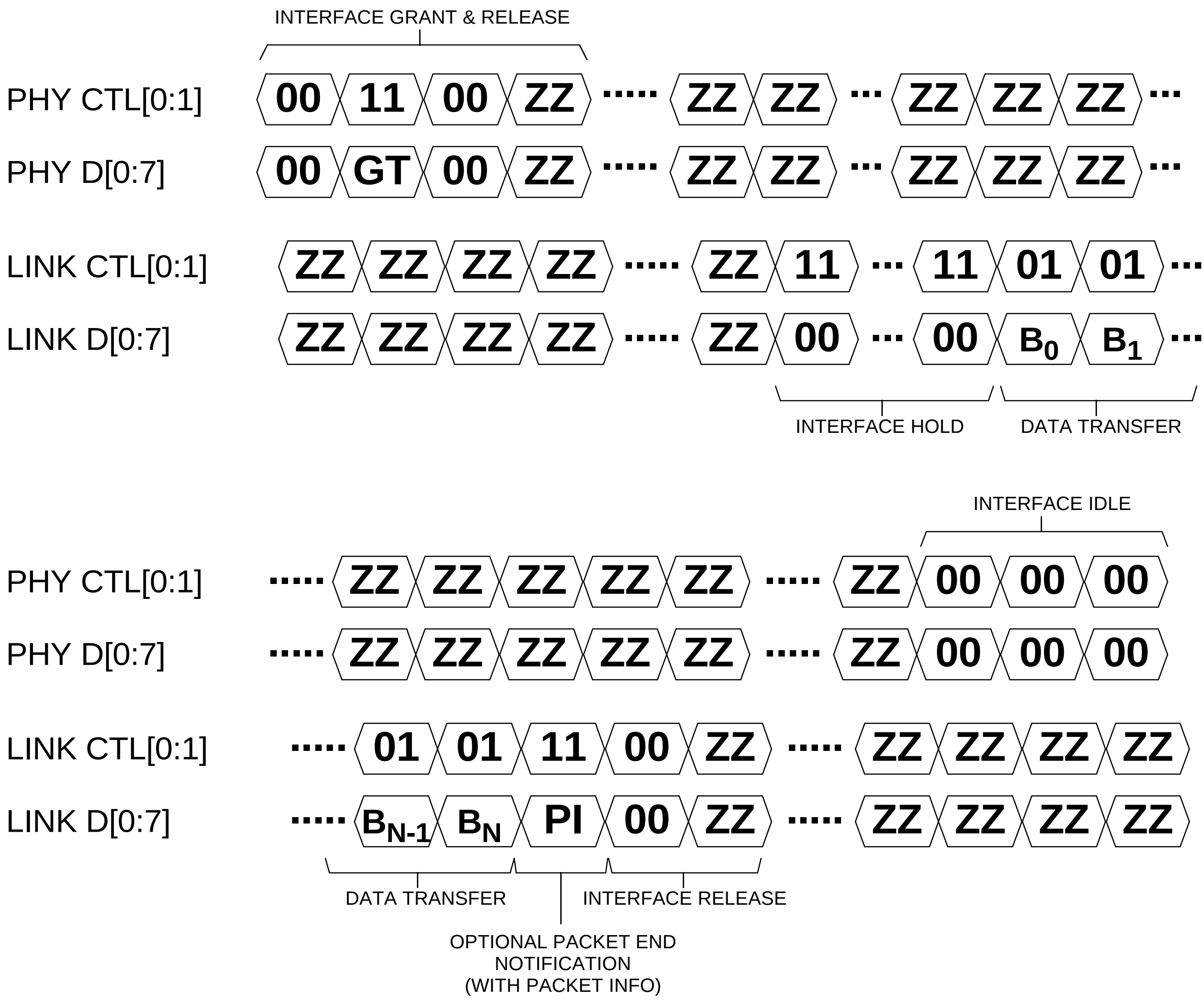


Figure 12-6—PHY-Link Packet Transmit Operation, including optional HOLD cycles

NOTE—B_0 - B_N represent the information bytes transferred from the Link to the PHY. See clause 12.8 for a data format description.

Packet Transmission Description

- The PHY indicates that it is transferring ownership of the interface to the Link by asserting GRANT on the CTL lines for one cycle while driving the appropriate GNT value on the D lines (see Table 12-10). The PHY then preconditions the CTL & D lines by driving them to zero for one cycle. The PHY then releases the CTL & D lines to a high impedance state.
- The weak pulldowns hold the CTL & D lines low while the Link device completes the interface handover.
- The Link indicates that it has packet data to transmit by asserting HOLD or TRANSMIT on the CTL lines as soon as possible. If the Link does not have any data to transmit, it shall not drive any value on the CTL lines.
- The PHY monitors the CTL lines to determine if the Link has completed the interface handover. If the PHY has not detected either HOLD or TRANSMIT states within 8 PCLK cycles, the PHY will assume that the Link has abdicated its transmission opportunity and will assume control of the interface by driving IDLE.
- Assuming the Link has packet data to transmit, the Link may optionally transmit HOLD on the CTL lines while it is preparing data for transmission. The Link is not required to drive HOLD if it has data immediately ready for transmission. The Link will drive the D lines to zero during HOLD cycles.
- The Link asserts TRANSMIT on the CTL lines when it is transmitting packet data on the D lines.
- After the last byte of the packet being transmitted, the Link may provide Packet Information to the PHY. The Link indicates this by asserting PACKET_END on the CTL lines while driving the relevant packet information (PI value defined in Table X-X) on the D[0:7] lines.
- The Link terminates a packet transmission by asserting IDLE on the CTL lines for one cycle while driving zero on the D lines. The Link then releases the CTL & D lines to a high-impedance state.
- When the PHY detects the IDLE cycle from the Link, it shall regain ownership of the interface by driving IDLE on the CTL lines and zero on the D lines.

NOTE— If the packet does not represent the end of a subaction, the Link only drives IDLE on the CTL lines and zero on the D for one cycle before releasing the signals to a high-impedance state.

12.7.1.1 PHY-Link Interface Grant Types

The PHY indicates to the Link during the GRANT cycle which type of grant is being issued. This indication includes the grant type as well as the grant speed. The Link shall only use the bus grant for transmitting the granted packet type. The Link shall transmit the granted packet type only at the granted speed.

Table 12-10—GT values during Grant Cycle

D[0:3] Value during GRANT cycle	Grant Type	D[4:7] Value during GRANT cycle	Grant Speed
0000	Asynchronous Grant	0000	S100
0001	Isochronous Grant	0001	S1600[a]
0010	Immediate Grant	0010	S200
0011	Cycle Start Grant	0011	S3200[a]
0100 - 1111	Reserved	0100	S400
		0101	Reserved
		0110	S800
		0111-1111	Reserved

[a]. these speeds are not defined for transmission over the discrete 1394b PHY-Link interface

NOTE—Concatenated packet transmission is not supported by the 1394b PHY-Link interface

12.7.1.2 Packet End Information Encoding

At the end of transmitting a packet, the Link may provide packet information and a further Link request before releasing the PHY-Link interface back to the PHY. The Link accomplishes this by driving PACKET_END on the CTL lines for a single cycle following packet data transmission, while driving the D[0:7] lines as follows

Table 12-11—Subaction End Notification during PACKET_END cycle

D[0] Value during PACKET_END cycle	Meaning
0	The packet which has been transmitted does not represent the end of a subaction
1	The packet which has been transmitted representes the end of a subaction

Table 12-12—Link Request type during PACKET_END cycle

D[1:2] Value during PACKET_END cycle	Meaning
00	No request
01	Isochronous Request - equivalent to CURRENT_ISOCH
10	Asynchronous Request - equivalent to CURRENT_ASYNC
11	Cycle Start Request

Table 12-13—Beta-format request type PACKET_END cycle

D[3] Value during PACKET_END cycle	Meaning
0	The Link is not explicitly requesting that the PHY use either Beta or Legacy packet format for packet transmission
1	The Link is explicitly requesting that the PHY use the Beta packet format for packet transmission

Table 12-14—Link Request Speed during PACKET_END cycle

D[4:7] Value during PACKET_END cycle	Request Speed
0000	S100
0001	S1600[a]
0010	S200
0011	S3200[a]
0100	S400
0101	Reserved
0110	S800
0111-1111	Reserved

[a] these speeds are not defined for transmission over the discrete 1394b PHY-Link interface

12.7.2 1394 Packet Receive Operation

When the PHY device detects a 1394 packet being received over the Serial Bus, it initiates a packet receive operation to the Link device. The PHY device does not perform any packet filtering on the received information. Any PHY packets originated by the PHY device as part of bus initialization are sent to its local link device in the same manner as packets received from other nodes. The Link device must be ready to receive a Serial Bus packet at any time over the PHY-Link interface. When the PHY has started to send a packet to the Link, it may send a holding pattern until such time as it has actual packet data to send. Once the PHY has started to send actual packet data, it shall send packet data information in consecutive PHY-Link interface bus cycles until transmission is complete.

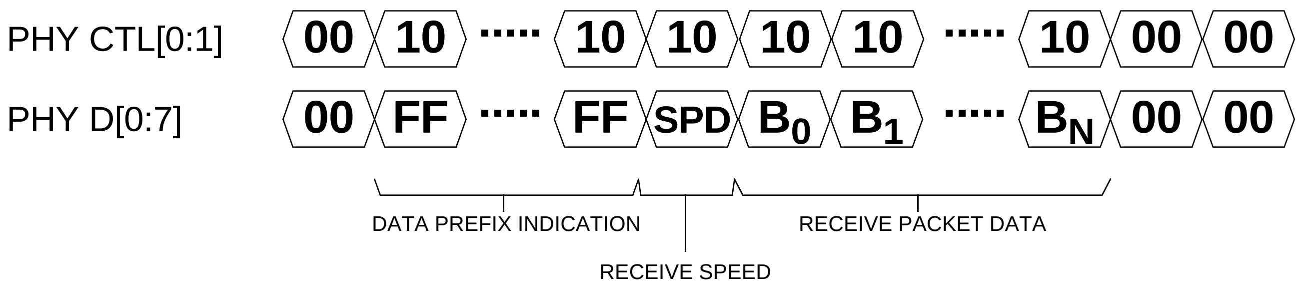


Figure 12-7—PHY-Link Packet Receive Operation

NOTE—B_0 - B_N represent the information bytes transferred from the PHY to the Link. See clause 12.8 for a data format description.

Packet Receive Description

- The PHY indicates that it has packet information to send to the Link by asserting RECEIVE on the CTL lines. If there is no packet data ready for transfer to the Link at that time, the PHY will indicate this to the Link by asserting FF_{16} on the D lines. The PHY will maintain this until such time as data is available.
- The PHY indicates the speed (hence the format - see clause 12.8) of the packet data by asserting a speed code on the D lines for one cycle while continuing to assert RECEIVE on the CTL lines.
- The PHY then transfers packet information to the Link on the D lines during successive cycles while continuing to assert RECEIVE on the CTL lines until the transfer is complete
- The PHY asserts IDLE on the CTL lines and 00_{16} on the D lines to indicate the completion of the packet receive operation.

NOTE—the PHY shall drive the PHY-Link interface to IDLE for a minimum of the number of interface cycles necessary to transfer one quadlet of packet information at the last received packet speed between consecutive Packet Receive operations.

Table 12-15—Receive Packet SPD encoding

D[0:7] during SPD cycle	Receive Packet Speed
00000000	S100
01000000	S200
01010000	S400
01010001	S800
01010010	S1600[a]
01010011	S3200
11111111	DATA_PREFIX
Other Values	Reserved

[a] these speeds are not defined for transmission over the discrete PHY-Link interface

12.8 Format of received & transmitted data

The PHY and Link can transfer data to each other at the following rates : S100, S200, S400 & S800

The PHY-Link interface operates in one mode

- 98.304 MHz PCLK/LCLK, Single-edge clocking - S800 capable

Data transfers between the devices are accomplished by appropriate padding of the lower rate data as described in the following sections. Data on the D[0:7] signal lines should be latched by the receiving device at the end of the first cycle in a repeating series for data transfers at S400 & below. The transmitting device should drive the same data on D[0:7] for all cycles of a repeating series.

PCLK & LCLK both run at 98.304 MHz ±100 ppm. Data transfers take place on the rising edge of PCLK & LCLK. LREQ requests and PINT status notifications are transferred only on the rising edge of LCLK & PCLK respectively.

NOTE—In the following diagrams, the values shown on D[0:7] are those which would be seen on an undifferentiated interface. In the case of a differentiated interface, the transmitting device drives the D[0:7] signal lines for only the first cycle of a repeated series, and the D[0:7] signals are undriven for the remainder of the byte time.

12.8.1 S100 Data

For packet data transmitted or received at S100, the following data delivery format is used to transfer the data to/from the PHY/Link device.

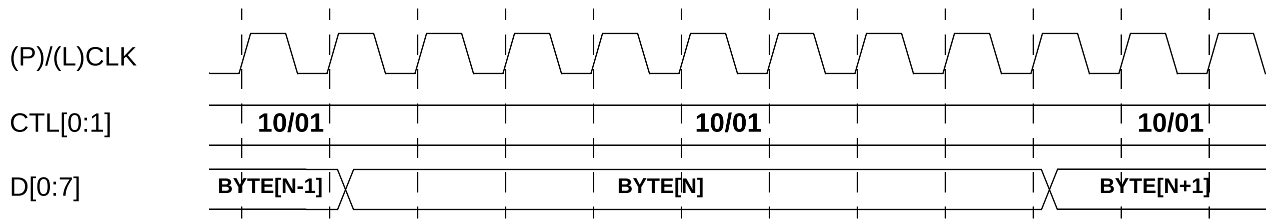


Figure 12-8—S100 Data transferred over 100 MHz, Single-edge clocking

12.8.2 S200 Data

For packet data transmitted or received at S200, the following data delivery format is used to transfer the data to/from the PHY/Link device.

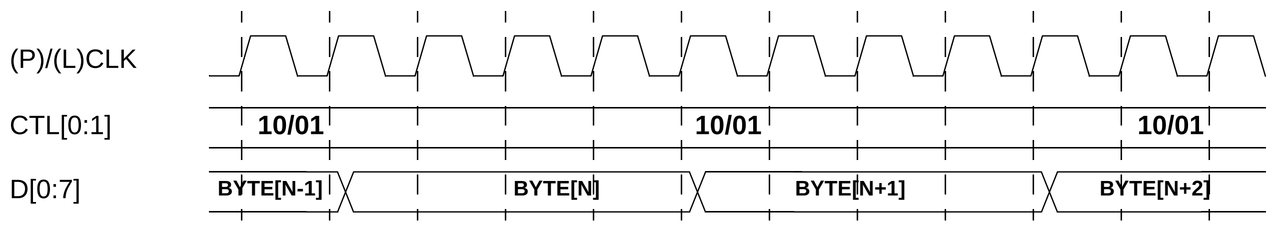


Figure 12-9—S200 Data transferred over 100 MHz, Single-edge clocking

12.8.3 S400 Data

For packet data transmitted or received at S400, the following data delivery format is used to transfer the data to/from the PHY/Link device.

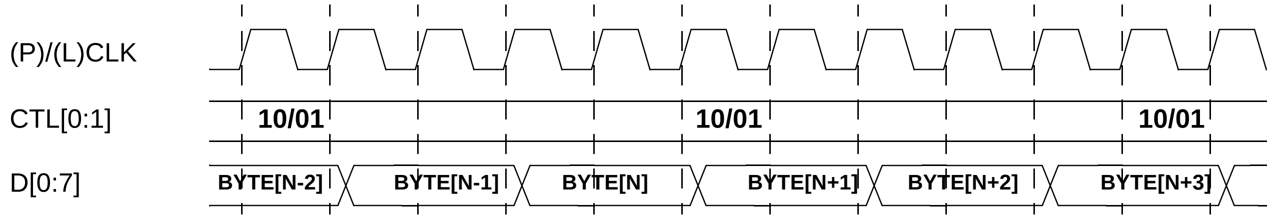


Figure 12-10—S400 Data transferred over 100 MHz, Single-edge clocking

12.8.4 S800 Data

For packet data transmitted or received at S800, the following data delivery format is used to transfer the data to/from the PHY/Link device.

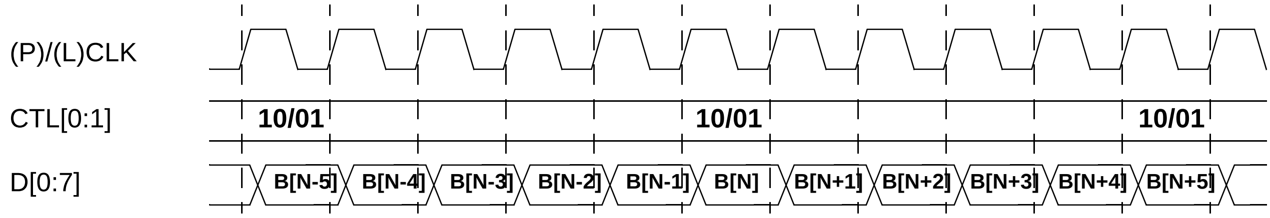


Figure 12-11—S800 Data transferred over 100 MHz, Single-edge clocking

12.9 PHY Status Transfers & Notifications

The PHY issues status transfers & notifications to the Link to

- notify the Link of Serial Bus events relevant to its operation
- notify the Link of PHY events relevant to its operation
- return PHY register read data requested by the Link
- transfer the Serial Bus node ID to the Link during the Tree Identification phase

12.9.1 PHY Status Format

All PHY status transfers & notifications take place serially over the dedicated PINT signal. The format of the PHY status transfer depends on the information which is to be transferred.

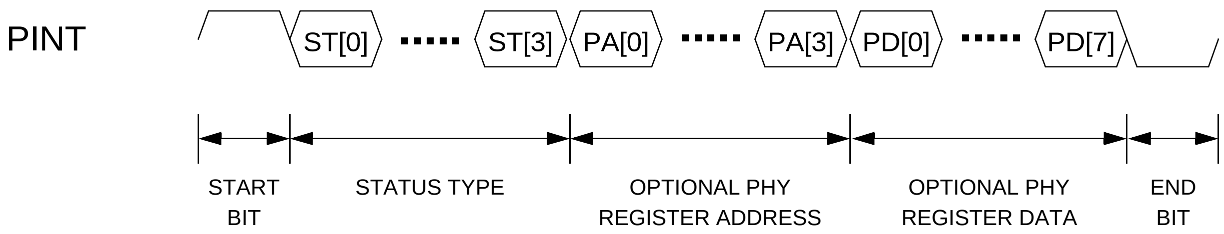


Figure 12-12— PHY Status/Interrupt Format

NOTE—each cell in the Link Request Format represents one PCLK cycle time

Status/Notification Transfer Mechanism

- The PHY begins a status transfer to the Link by asserting the PINT signal to ‘1’ for one cycle (START BIT)
- The PHY issues a 4 bit status type field serially over PINT. The status type determines if there are further fields associated with the status transfer
- If there are further fields, these are transferred serially over PINT
- The status transfer completes with the PHY deasserting the PINT signal to ‘0’ for one cycle (END BIT)

The PHY may immediately begin another status transfer following the END bit of the previous one. PHY status transfers can occur concurrently with Link requests and packet transmission/reception operations. Multiple status events are indicated by multiple status transfers. The ordering of status transfers is determined by the PHY.

Table 12-16—PHY Status Type encoding

ST[0:3] Value	Name	Meaning	Additional Fields
0000	Reserved	Reserved. The PHY shall not issue a status transfer of this value	None
0001	BUS_RESET	The PHY has detected the start of a Serial Bus Reset	None
0010	ARB_RESET_GAP_EVEN	The PHY has determined that an arbitration reset gap has occurred on Serial Bus. The PHY now deems the fairness interval phase to be EVEN	None
0011	ARB_RESET_GAP_ODD	The PHY has determined that an arbitration reset gap has occurred on Serial Bus. The PHY now deems the fairness interval phase to be ODD	None
0100	SUBACTION_GAP	The PHY has determined that a subaction gap has occurred on Serial Bus	None
0101	PHY_INTERRUPT	The PHY requires the Link to read its internal register set to determine the cause of the interrupt	None
0110	PHY_RESET	The PHY has initiated a reset of the PHY-Link interface. The Link shall terminate any ongoing operation over the PHY-Link interface and shall deem all outstanding requests to have been cancelled	None
0111	PHY_REGISTER_SOL	The PHY is returning the contents of one of its internal registers as a result of the Link having explicitly requested such a read	PHY Address, PHY Data
1000	PHY_REGISTER_UNSOL	The PHY is returning the contents of one of its internal registers without having been requested by the Link to do so	PHY Address, PHY Data
1001	CYCLE_START_EVEN	The PHY has received an EVEN cycle start token	None
1010	CYCLE_START_ODD	The PHY has received an ODD cycle start token	None
1011	RESTORE_NO_RESET	The PHY has restored from a standby state without having detected a Serial Bus Reset	None
1100	RESTORE_RESET	The PHY has restored from a standby state and has detected a Serial Bus Reset	None
1101 - 1111	Reserved	Reserved	-

PHY register read operations are completed by the PHY issuing a status transfer of type PHY_REGISTER followed by the PHY address of the register being read, followed by the 8-bit data contents of the PHY register.

The PHY notifies the Link of its Node ID value during Tree ID by issuing an unsolicited PHY_REGISTER transfer for PHY register 0. The PHY register contents contain the 6-bit Node ID value determined by the PHY as part of that process.

12.10 1394a Link support

The 1394b PHY-Link interface is a superset of the 1394a signals. This allows a 1394b PHY to optionally support the existing 1394a PHY-Link interface. 1394b PHY devices are not required to support 1394a Link devices.

If the optional BETA_MODE input to the PHY is connected to logical '0', the Beta-PHY shall operate its PHY-Link interface in accordance with the PHY-Link interface specification detailed in the 1394a specification. In this mode, the PHY sources an interface clock of 49.152 Mhz in accordance with the 1394a specifications. In this case, the 1394b PHY-Link interface pins are used as follows:

Table 12-17—Mapping of 1394b PHY-Link signals to 1394a signals

1394b PHY-Link Interface pin	1394a PHY-Link interface pin
CTL[0:1]	CTL[0:1]
D[0:7]	D[0:7]
PCLK	SCLK
LREQ	LREQ
LINKON	LINKON
LPS	LPS
LCLK	Not Used by 1394a - PHY holds to logical '0'
PINT	Not Used by 1394a - PHY drives logical '0'
BETA_MODE	System drives logical '0'

In this mode of operation, Link requests, Link & PHY packet transfers and PHY status transfers take place in the manner defined by 1394a. No 1394b specific features, such as request for next cycle, Link requested interface reset etc. are available. The existing 1394a LREQ cancellation rules also take effect.

Data transfers at S100, S200 & S400 only are supported by the PHY-Link interface in this mode.

In this mode of operation, the LCLK input to the PHY will be held to logical '0' by the PHY. The PHY PINT signal output shall be driven to logical '0' by the PHY and should not be used.

To facilitate existing 1394a Link implementations using a 1394b PHY, the timing relationships defined by 1394a for the PHY-Link interface pins shall be adhered to by a 1394b PHY offering this capability.

12.11 PHY integrated with Link Interface Model - High-Speed & Isolation

In order to support higher transfer rates than S800 and to provide a more flexible approach to interface isolation, this section describes an interface model which may be used to achieve data transfers at S1600 & S3200 data rates and which is more readily applicable to electrical isolation than the discrete PHY-Link interface.

In this mode of operation, a Beta-only 1394b PHY and a 1394b Link are integrated into a single device. The PHY & Link communicate via an unspecified internal interface which may support data transfers at speeds up to S1600 & S3200. In a system where electrical isolation is not a requirement, this combination can then be directly connected to another node via a standard 1394b Beta-only Serial Bus connection. In a system where electrical isolation is a concern, this PHY-Link combination can be connected via an isolated Serial Bus Beta-only connection to another PHY device, which can be independently powered, and which serves as a fanout device.

12.11.1 Operating Model

The operating model is such that the integrated PHY & Link device operates as an effective Link, while the fanout PHY device operates as the effective PHY in the system. In this arrangement, the combination of integrated PHY & Link and fanout PHY operates as a single node on the network. This requires that the integrated PHY & Link has a means of getting read & write access to the fanout PHY device's PHY register set.

Consideration has been given in this mode of operation to ensuring that using a fanout PHY device presents the same operational model from a system software point of view i.e. from a software point of view, the fanout PHY device does not represent a separate node in the network for power management or other purposes.

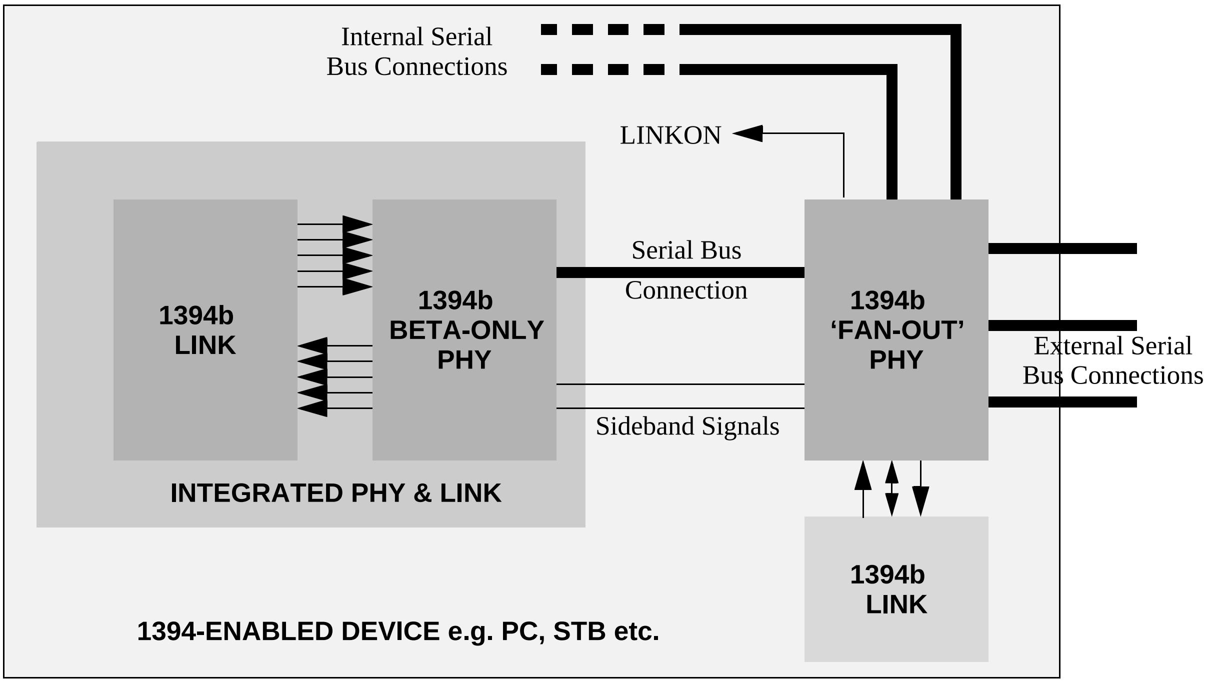


Figure 12-13— Possible System Configuration using a fanout PHY Device

To achieve this goal of software transparency, it is necessary to define a set of sideband signals between the integrated PHY & Link and the fanout PHY device. In the fanout mode of operation, the integrated PHY & Link act effectively as the Link would in the discrete case. The fanout PHY device is operating as the effective PHY. In order for the integrated PHY-Link combination to have access to the fanout PHY device's internal PHY register set, a set of sideband signals is defined to allow this information to be transferred. These sideband signals are defined such that they can easily cross an electrical isolation barrier.

A fanout PHY device may optionally provide a discrete PHY-Link interface. If a Link is directly attached to a fanout PHY device, such a device represents a distinct node on the network.

In the absence of a discrete PHY-Link interface, or in the case where no Link is directly attached to the fanout PHY device, the effective PHY-Link interface is defined as the highest numbered Serial Bus port connection on the fanout PHY. Any signalling/toning activity on this highest-numbered port is regarded as being logically equivalent to the Link LPS signal being asserted. The absense of any signalling on this highest-numbered port is regarded as being logically equivalent to the Link LPS signal being deasserted.

The fanout PHY device shall provide a LINKON signal, as defined in this section, which is used in the system to notify the effective Link that a PHY_EVENT.indication of LINK_ON has been received.

12.11.2 Sideband Signals

A pair of signals are used to communicate PHY register read & writes between the integrated PHY & Link and the fanout PHY device. These signals are FOP_REQ & FOP_INT. FOP_REQ is generated by the integrated PHY & Link and indicates to the fanout PHY that a PHY register read or write is needed, together with any associated data. FOP_INT is generated by the fanout PHY device and is used to return PHY register information to the integrated PHY & Link.

In order to cross an optional isolation barrier, FOP_REQ & FOP_INT are generated as Manchester-Encoded signals, as indicated in the following diagram

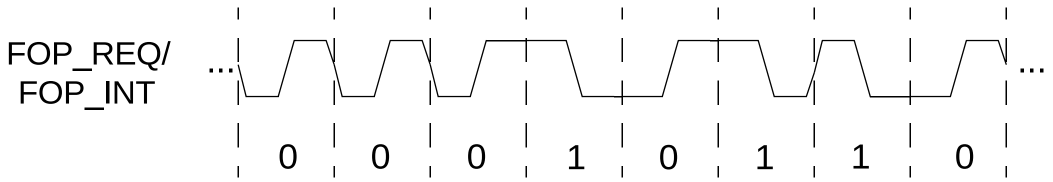


Figure 12-14— Encoding of FOP_REQ & FOP_INT Sideband signals

Following connection of the integrated PHY & Link and the fanout PHY, both devices generate a stream of logical ‘0’s on the sideband signals as a training sequence during the period when toning and synchronization is occuring on the Serial Bus connection. This training process concludes when Serial Bus synchronization is achieved between the integrated PHY & Link and the fanout PHY.

Table 12-18—FOP_REQ & FOP_INT Signal Characteristics

Characteristic	Units	Min.	Typical	Max.	Comments
Bit Period	ns	18	20	22	
Signal Slew Rate	V/s	-	-	-	
V_{OH}	V	-	-	-	Conditions ?
V_{OL}	V	-	-	-	Conditions ?
V_{IH}	V	-	-	-	Conditions ?
V_{IL}	V	-	-	-	Conditions ?
Training Period	bits	-	-	-	Both devices drive logical ‘0’ during this period

12.11.3 Sideband Register Requests & Responses

12.11.3.1 FOP_REQ Request Format

The integrated PHY & Link uses the FOP_REQ signal to request read or write access to the fanout PHY device's PHY register map. The format of the FOP_REQ request is the same as is specified for the LREQ request (see clause 12.6.7 for details). Note that for the FOP_REQ request, the only valid values for RT (Request Type) are REGISTER_READ & REGISTER_WRITE. All other values of RT are ignored by the fanout PHY device.

For a PHY register write operation, the integrated PHY & Link device provides the PHY register address and the write data as part of the FOP_REQ signal sequence in the same manner as for an LREQ request.

For a PHY register read operation, the integrated PHY & Link device provides the PHY register address as part of the FOP_REQ signal sequence in the same manner as for an LREQ request.

12.11.3.2 FOP_INT Response Format

The fanout PHY device uses the FOP_INT signal to return PHY register read data to the integrated PHY & Link and also to provide the fanout PHY's Node ID at bus initialization time. The format of the FOP_INT signal sequence is the same as is specified for the PINT signal sequence (see clause 12.9.1 for details). Note that for FOP_INT, the only valid values for ST (Status Type) are PHY_REGISTER_SOL & PHY_REGISTER_UNSOL. All other values of ST are ignored by the integrated PHY & Link device.

12.11.4 LINKON Signalling

In this mode of operation, the fanout PHY is required to provide a LINKON signal, which may be used within the system to notify the integrated PHY & Link that a PHY_EVENT.indication of LINK_ON has been received. The characteristics of this LINKON signal are identical to those specified for the LINKON signal in the discrete PHY & Link case (see clause 12.5 for details)

12.11.5 Mode Discovery

It is the intent of this operating model that the fanout PHY device may be implemented by a standard 1394b PHY, which may also serve a non-fanout application as a discrete PHY. There is no mechanism defined in this specification to allow for doscovery of the required mode of operation in the system. It is the system designer's responsibility to ensure that the fanout PHY is configured in such a manner so as to serve the appropriate purpose.

Note that during the Tree ID and Bus Initialization process, the PHY which is part of the integrated PHY & Link does not take part in this process i.e. does not issue a self-id packet of its own. This reflects its function as part of an effective Link in the system. It is the system designer's responsibility to ensure that the integrated PHY behaves in this manner.

12.12 PHY-Link Electrical Characteristics

CHECK FOR ALL TAGS WITH ??? these are questions.

12.12.1 This is a section from the 1394.a spec and I do not see equivalent in 1394B

NOTE—In cases where the PHY and link are powered independently of each other, the link implementation should be able to detect the loss of PClk from an otherwise initialized and operational PHY/link interface.

12.12.2 Isolation requires signal value differentiators to work with the capacitive isolation that differentiates signals.

NOTE—Differentiators may be required when the PHY and link are connected through an optional isolation barrier; see annex A for a discussion of electrical isolation in the cable environment. A digital differentiator drives its output signal for one clock period whenever the input signal changes, but places the output signal in a high-impedance state so long as the input signal remains constant. Figure 12-13 illustrates this signal transformation.

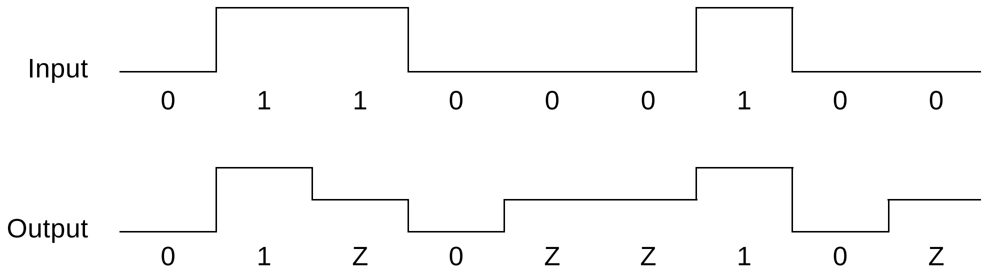


Figure 12-15 — Digital differentiator signal transformation

When the interface is running at PClk of 98 MHz and the incoming data is S100 which of the 8 clock cycles should be the driven cycle. I would assume the FIRST cycle and then tri-state for the rest. But the previous diagrams imply all cycles driven which is a problem in differentiated mode..

12.12.3 Initialization and reset

The previous section on reset discusses preconditioning signals by driving a 0 (zero) during one of the first 6 PClk cycles is only applicable for cable applications. For backplane applications, the speed code is set to 00xxxxxx.

12.12.4 Electrical characteristics (cable environment)

This clause specifies the signal and timing characteristics of the interface between a discrete PHY and link.

12.12.5 DC signal levels

The basic assumptions in this section are that all interfaces are 3.3V I/O complaint. The I/O voltage compatibility of future IC processes will be assumed to handle 3.3V I/O signals. The signal levels will be targeted to be CMOS signals that swing rail to rail. All inputs will be tolerant of 3.3V signals when they are powered down and will not cause either permanent damage or inconsistent behavior when powered while inputs are driven.

The 1394.a link can be connected to a 1394B Phy. When a 1394.a link is connected to a 1394B PHY the signaling will conform to 1394.a specification for both differentiated and undifferentiated signaling. (reference section 12.12)

DC parametric attributes of the PHY/link interface signals are specified by Table 12-13. Input levels may be greater than the power supply level (*e.g.*, a 3.3V output driving V_{OH} in differentiated mode); tolerance of differentiated input levels is optional. Devices not tolerant of differentiated input levels but which otherwise meet the requirements below are compliant with this standard. V_{DD} is defined to be 3.3V ± 10%.

Table 12-19 — DC specifications 1394B mode PHY/link interface

Name	Description	Conditions	Unit	Minimum	Maximum
V_{DD}	I/O supply voltage level		V	3.3 ± 10%	
V_{OH}	Output high voltage (undifferentiated)	I_{OH} = -4 mA	V	2.7	
V_{OHD}	Output high voltage (differentiated)	I_{OH} = -9 mA at V_{DD} = 3 V	V	V_{DD} - 0.4	
V_{OL}	Output low voltage (undifferentiated)	I_{OL} = 4 mA	V		0.4
V_{OLD}	Output low voltage (differentiated)	I_{OL} = 9 mA at V_{DD} = 3 V	V		0.4
V_{IH}	Input high voltage (undifferentiated)		V	2.6	V_{DD}[a]+10%
V_{IL}	Input low voltage (undifferentiated)		V		0.7
V_{LIT+}	Input rising threshold (LinkOn and LPS)		V		V_{LREF} + 1[b]
V_{LIT-}	Input falling threshold (LinkOn and LPS)		V	V_{LREF} + 0.2[b]	
V_{IT+}	Hysteresis input rising threshold (differentiated)[c]		V	V_{REF} + 0.3	V_{REF} + 0.9[d]
V_{IT-}	Hysteresis input falling threshold (differentiated)[c]		V	V_{REF} - 0.9[d]	V_{REF} - 0.3
V_{REF}	Reference voltage[e]		V	V_{DD}/2 ± 1%	
V_{LREF}	Reference voltage[f] (LinkOn and LPS inputs)		V	0.5	1.6
C_{IN}	Input capacitance		pF		5.0

a. Allows for driving device’s power supply

b. The LinkOn and LPS receiver parameters are based on a swing of 2.4 V for the received signal. Links which only depend on receiving the initial edge of LinkOn may be capable of operating with less constrained values.

c. When the PHY/link interface is in differentiated mode, the PClk LClk input shall meet the V_{IT+} and V_{IT-} requirements.

d. When designing a device capable of both undifferentiated and differentiated operation, V_{IH} and V_{IL} effectively constrain these V_{IT+} and V_{IT-} values to V_{REF} + 0.8 V and V_{REF} - 0.8 V, respectively.

e. For some applications, a device can be compliant with these DC specifications even if a different V_{REF} is chosen. (??? should we leave this is this really true????)

f. For a particular application, there is a single value for each device’s nominal bias point, V_{LREF}, which shall be within the range specified. V_{LREF} should be chosen in conjunction with the receiver parameters so that a loss of power by the transmitting device is perceived as zero by the receiving device.

12.12.6 Phy-Link measurement definitions

All Phy-link ac timing measurements are made at the Phy-link receiver input and are specified relative to the $V_{IL(\text{max})}$ and $V_{IH(\text{min})}$ thresholds (undifferentiated) or $V_{IT\text{-}(\text{max})}$ and $V_{IT+(\text{min})}$ thresholds.

The (P)/(L)CLK parameters t_{PERIOD}, t_{HIGH}, and t_{LOW} are defined in Figure 12-14. The (P)/(L)CLK parameters t_R and t_F and other transient performance specifications are defined in Figure 12-15. These parameters and the (P)/(L)CLK rising and falling slew rates are measured using the "Phy-link Point-to-Point Test Circuit" shown in Figure 5-5.

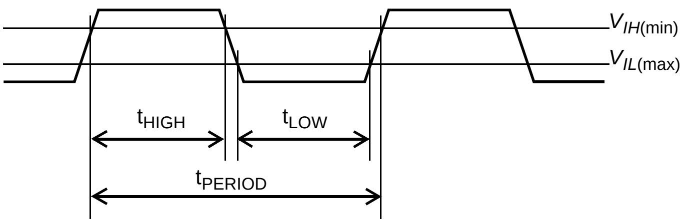
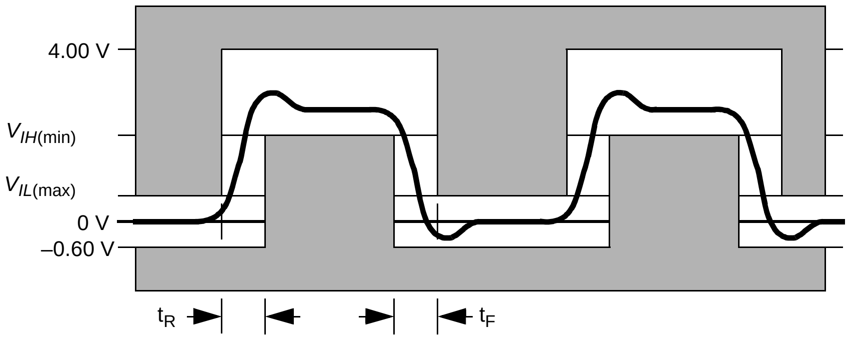


Figure 12-16 — PCLK and LCLK timing parameters at receiver input



NOTE—As measured at input measurement point

Figure 12-17 — Phy-link receiver input potential template (undifferentiated)

The t_{SETUP} and t_{HOLD} parameters are defined in Figure 12-16. These parameters are measured using the "Phy-link Setup and Hold Time Test Circuit" shown in Figure 12-18.

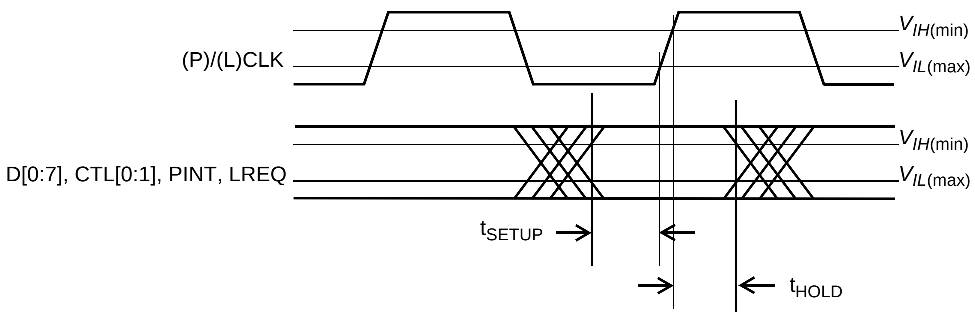


Figure 12-18 — Phy-link signal timing at receiver input

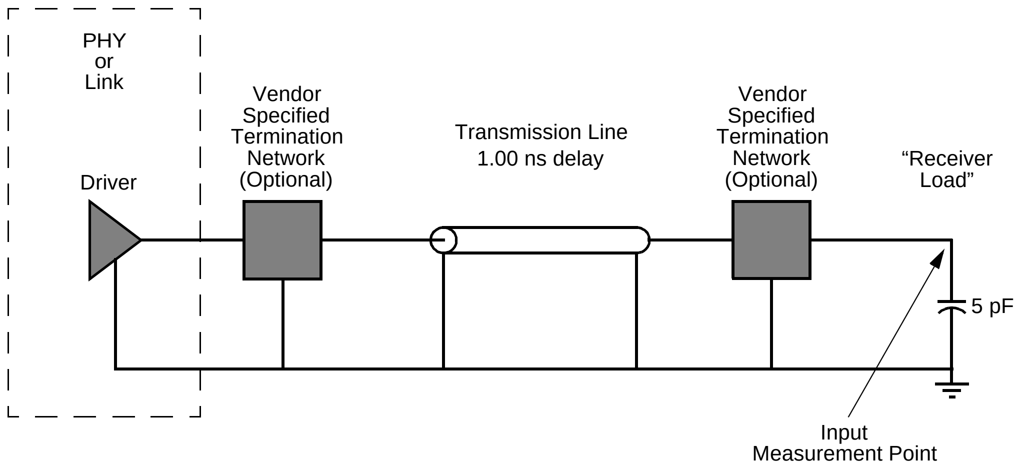


Figure 12-19 — Phy-link point-to-point test circuit

The rise and fall time measurement definitions, t_R and t_F, for PCLK, LCLK, Ctl[0:1], D[0:7] and LReq are shown in Figure 12-15.

The “Phy-link Point-to-Point Test Circuit” specifies a 1 ns transmission line. In a Phy-link implementation, the circuit board traces between the PHY and link are not restricted to a delay of 1 ns.

The “Phy-link Setup and Hold Time Test Circuit” is defined in Figure 12-18. The circuit is comprised of the source of the synchronous Phy-link signal under test and its clock (the link or the PHY) and two “Phy-link Point-to-Point Test Circuits.” One of the test circuits includes the Phy-link driver for the signal under test, the other test circuit includes the Phy-link driver for the clock that provides timing for the signal under test. The signal under test is measured at the “Signal Measurement Point” relative to its clock, which is measured at the “Clock Measurement Point” as defined in Figure 12-18.

12.12.7 Phy-link AC specifications

A Phy-link driver, when used in combination with the termination networks specified by the implementor of the driver for a specific Phy-link topology, shall produce a potential at the input pin of any Phy-link receiver in that topology that complies with the input potential template shown in Figure 12-15. This requirement applies for all Phy-link signals and any Phy-link topology.

To ensure that all Phy-link devices support point-to-point links, a Phy-link driver, when driving the “Phy-link Point-to-Point Test Circuit” shown in Figure 5-5, shall produce a potential at the “Input Measurement Point” of the “Phy-link Point-to-Point Test Circuit” that complies with the input potential template shown in Figure 12-15.

All Phy-link signal sources, including the Phy-link drivers, Phy-link receivers and Phy-link signals shall comply with the specifications in Table 12-13 for signal levels and Table 12-14 for AC timing.

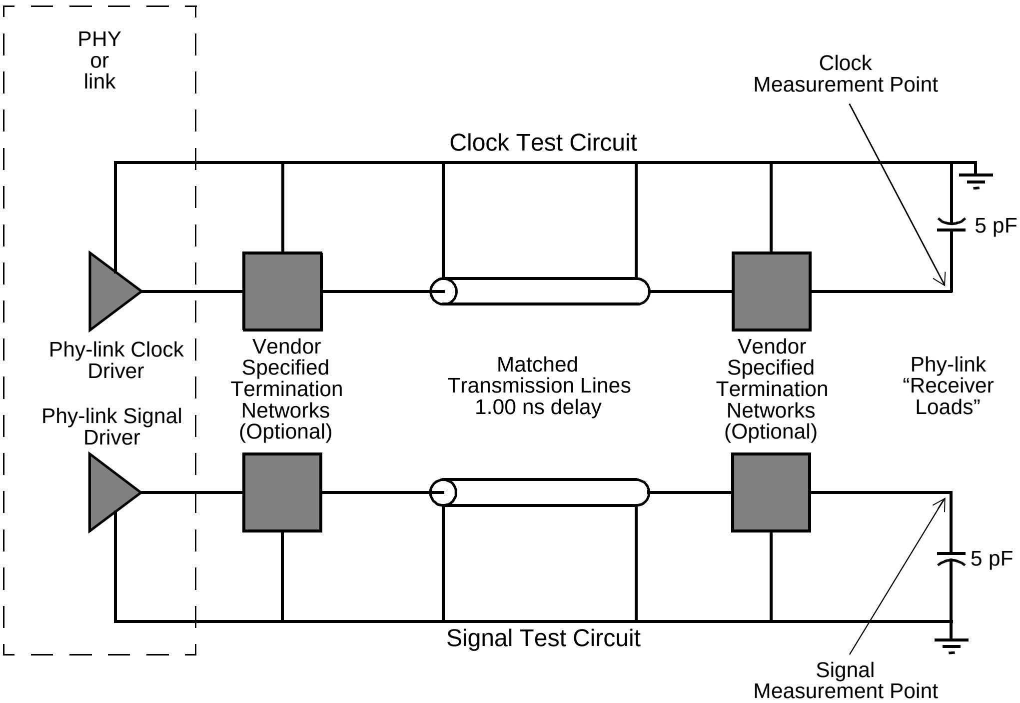


Figure 12-20 — Phy-link setup and hold time test circuit

Two sets of setup and hold time parameters are specified in Table 12-14. The first set, t_{SETUP} and t_{HOLD}, applies to the source of a synchronous Phy-link signal and its clock and is measured using the "Phy-link Setup and Hold Time Test Circuit," which has transmission lines with matched propagation delays in the "clock" and "signal" paths. The second set, $t_{SETUP(RCVR)}$ and $t_{HOLD(RCVR)}$, applies to the Phy-link receiver and specifies the minimum setup and hold times available to the Phy-link receiver at its input pins. The difference between the two sets of setup and hold time parameters provides margin for a small amount of mismatch in the propagation delays of the "clock" path and the "signal" paths in Phy-link applications.

The Phy-link AC specifications in Table 12-14 and the transient performance specifications in Figure 12-15 shall be met under all combination of worst-case Phy-link driver process and supply potential variation, ambient temperature, transmission line impedance variation, and termination network component impedance variation.

Other signal characteristics of the PHY/link interface are specified by Table 12-14. If an isolation barrier is implemented it shall cause neither delay nor skew in excess of the values specified. AC measurements shall be taken from the $V_{IH(min)}$ level of PClk or LClk to the input of Ctl[0:1], D[0:7] or LReq levels and shall assume a load C_{in} as specified.

Table 12-20 — AC timing parameters

Name	Description	Unit	Minimum	Maximum
	PCLK or LCLK Frequency	MHz	98.304 ± 100 ppm	
t_{period}	PCLK or LCLK Period	ns	10.0	10.4
t_{high}	PCLK or LCLK Time High	ns	3.00	
t_{low}	PCLK or LCLK Time Low	ns	3.00	
t_r	PCLK or LCLK Rise Time	ns	--	1.0
t_f	PCLK or LCLK	ns	--	1.0
-	Magnitude of PCLK, LCLK slew rate [a]	V/ns	0.6[a]	--
t_{setup}	D[0:7], Ctl[0:1], Lreq Setup to ↑ PCLK or LCLK	ns	2.50	--

Table 12-20 — AC timing parameters (Continued)

Name	Description	Unit	Minimum	Maximum
t_{hold}	D[0:7], Ctl[0:1], Lreq Setup to ↑ PCLK or LCLK	ns	0.50	--
t_{setup} (RCVR)	D[0:7], Ctl[0:1], Lreq Setup to ↑ PCLK or LCLK	ns	2.00	--
t_{hold} (RCVR)	D[0:7], Ctl[0:1], Lreq Setup to ↑ PCLK or LCLK	ns	0.00	--
idel	Delay through isolation barrier	ns	0	2
	Skew through isolation barrier	ns	0	0.5
	Isolation barrier recovery time	µs	0	10

[a] Clock slew rates is the instantaneous change of clock potential with respect to time (dV/dT) not an average over the entire rise or fall time interval. Conformance with this specification guarantees that the clock signals will rise and fall monotonically through the switching region

The Current tables only specify the parameters for 3.3V operation, as discussed earlier. In addition The AC and timing parameters are specified for the link/Phy interface running at up to S800 speeds. The link/Phy electrical specification for DISCRETE components running at higher speeds is not included in this draft. It is assumed that the higher speeds will be implemented using an integrated 1394B link in Beta only mode connected to a fanout Phy for the for seeable future.

12.12.8 AC timing (informative)

IS THIS STILL TRUE??

The protocol of this interface is designed such that all inputs and outputs at this interface can be registered immediately before or after the I/O pad and buffer. No state transitions need be made that depend directly on the chip inputs; chip outputs can come directly from registers without combinational delay or additional loading. This configuration provides generous margins on setup and hold time.

???? is the above really true in 1394B I assume so but I want to confirm that since this was lifted from 1394.a?????

In the direction from the PHY to the link, timing follows normal source-clocked signal conventions. A 0.5 ns allowance is made for skew through an (optional) isolation barrier.

12.12.9 Isolation barrier (informative)

The example circuits shown in this clause demonstrate how to achieve galvanic isolation between a discrete PHY and link by means of a capacitive isolation barrier. For applications that require isolation, other methods may be used. When capacitive isolation is used between the PHY and the link, the grounds of both devices must be coupled as shown in Figure 12-19. The details of this ground coupling are omitted from figures 12-20 through 12-24.

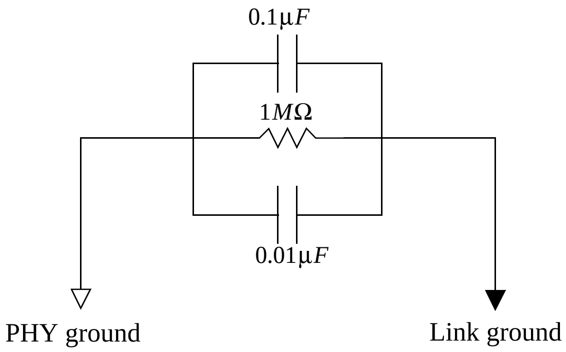


Figure 12-21 — Ground coupling circuit example

The isolation design in the following circuits have a signal sag of approximately 0.3% per nanosec. The sag may cause a signal to exceed the power supply on the input during the next transition. Depending on the longest duration of a one or zeros this may be a problem at the next transition of a signal. The resulting overshoot could impact the RFI (radio frequency interference). In addition, inputs should be specified to be tolerant of signals that exceed the power supply rail.

Caution should be exercised since capacitive isolation will pass through any high frequency transients such as ESD (electrostatic discharge) events at the PHY cable interface. The inputs on both sides of the link Phy interface should have robust ESD performance.

The ability to match the center of the hysteresis for the inputs and the nominal bias voltage from the resistive dividers is critical.

The example circuits that follow illustrate different requirements of the various signals of the PHY/link interface.

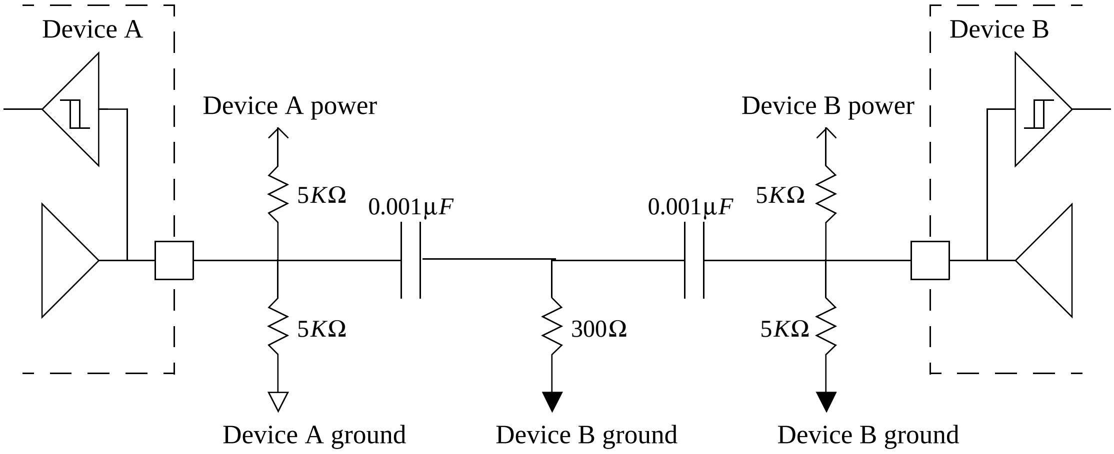


Figure 12-22 — Capacitive isolation barrier circuit example for Ctl[0:1] and D[0:*n*]

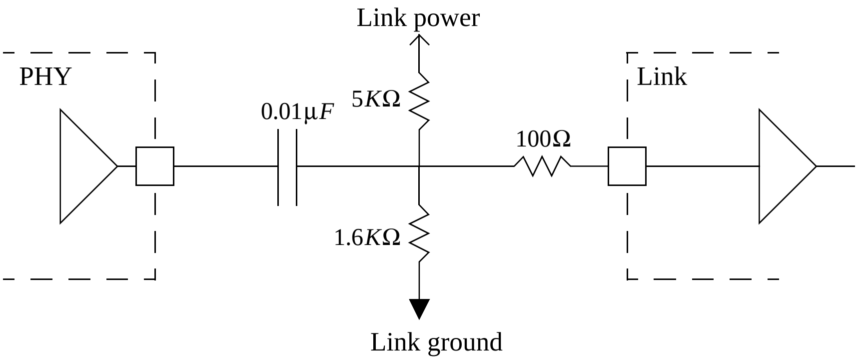


Figure 12-23 — Capacitive isolation barrier circuit example for LinkOn

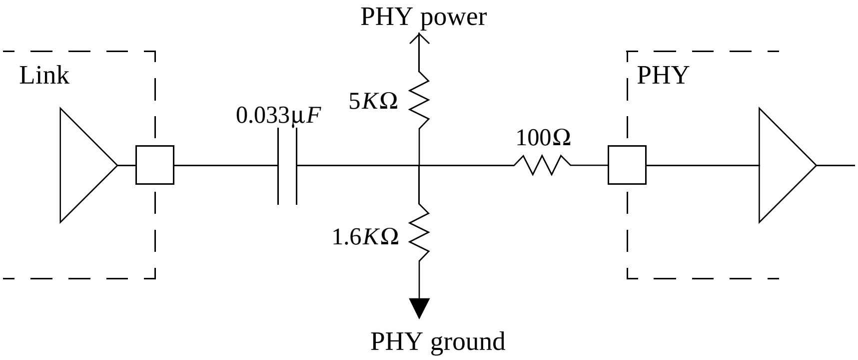


Figure 12-24 — Capacitive isolation barrier circuit example for LPS

 This is an unapproved standards draft, subject to change

NOTE—In figures 12-23 and 12-24, the values of the resistors between signal and ground or signal and power should be chosen to suit the implemented value of V_{LREF}. The values shown are appropriate when V_{LREF} is nominally 0.8 V.

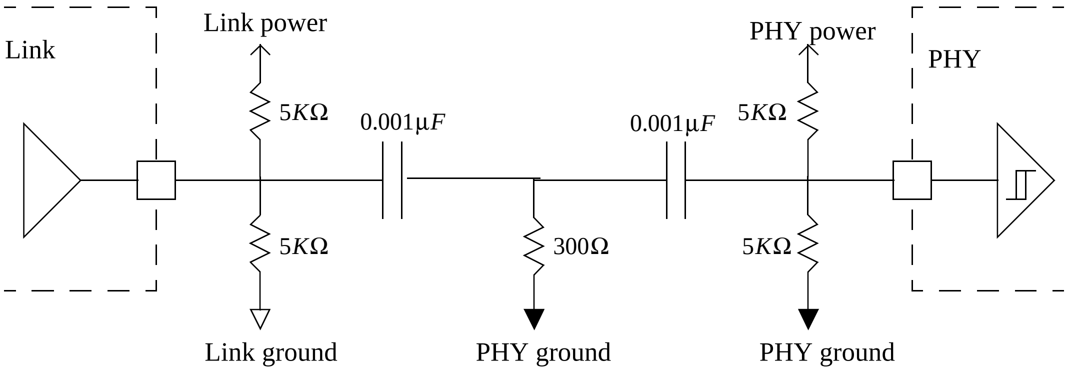


Figure 12-25 — Capacitive isolation barrier circuit example for LReq

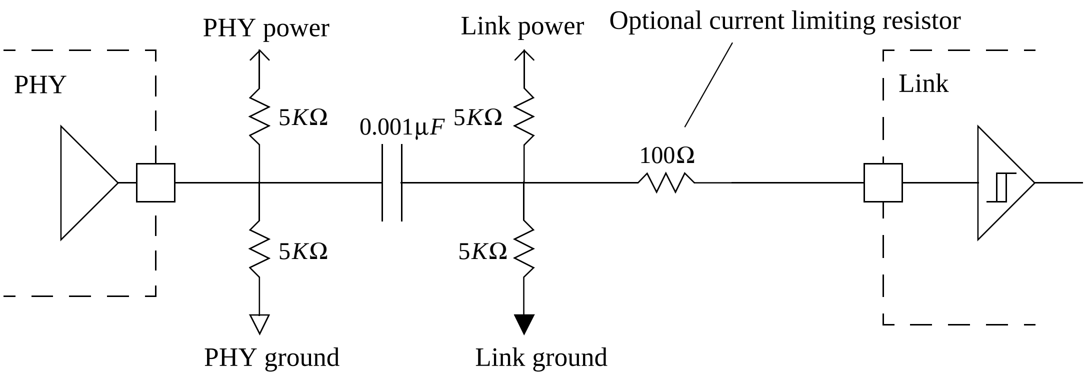


Figure 12-26 — Capacitive isolation barrier circuit example for SClk

[This section is not completed]

12.12.10 DC Signal Levels & Waveforms

[This section is not completed]

12.12.11 AC Timing

[This section is not completed]

12.12.12 Isolation Barrier

[This section is not completed]