

Agenda
IEEE p1394b
Working Group
Plenary Meeting - June 8, 1999

1. Review Agenda
 2. Review of April Meeting Minutes
 3. Procedures
 - 3.1. Voting
 - 3.2. Price/Pricing
 - 3.3. Call For Patents
 4. Review Old Action Items
 5. Meeting Schedule
 - 5.1. July 20, Briarcliff, NY
 - 5.2. August 24, Portland (?)
 - 5.3. Sept -- Need Invitation (San Jose)
 6. Votes
 - 6.1. Elimination of Speed Map
 - 6.2. Hardwire MAX_SPEED register to 111b
 - 6.3. Eliminate the "Other (not defined by this specifications)" row in Table 11-1 ("Media dependent Beta mode speed requirements")
 7. Presentations
 - 7.1. BOSS Arbitration - Colin Whitby-Strevens
 - 7.2. Border Nodes - Jerry Hauck
 - 7.3. PHY/Link Interface - Tony Foster
 - 7.4. Beta Connector - Max Bassler
 8. Task Group Reports (As required)
 9. New Issues
 - 9.1. Specification Completion Schedule
 - 9.2.
 - 9.3.
 10. Review of Action Items
 11. Adjournment
-
-

MEETING MINUTES

Review of agenda and call for agenda additions.

Accept previous meeting minutes: Max Bassler moved to accept, seconded by Colin Whitby-Strevens. Passed without objection.

Voting, price/pricing, Call for Patents - all presented in the usual, professional manner by the group chair.

Review of Action Items from previous meetings:

AI: David Wooten – work on getting loop healing issues resolved in preparation for inclusion in the draft specification. Report progress at next Plenary - **DONE**

AI: David Wooten: Address the link people to determine minimum packet separation needed. **NOT DONE**

AI: Colin to announce provisional acceptance of crossover on the reflector. If no scream response, it will become part of the draft. **DONE**

AI: Colin to review crossover proposal and evaluate implementation for upstarts. **DONE and in the draft specification (0.17)**

Meeting schedule reviewed.

July will be in Briarcliff (White Plains), NY on July 20th. August meeting will be hosted by HP in Portland, Oregon (Brian Batchelder). David James (Sony) has suggested San Jose may be a possibility. In selecting a date for September, Max suggested consideration of PC EXPO the 7th through the 10th EIA-J is the 30th of September.

VOTES

Elimination of the Speed Map.

The speed map defined in IEEE 1394-1995 has been deprecated in IEEE 1394a-1999. John Fuller moved that the IEEE p1394b draft standard be silent on the topic of speed map. Seconded by Steve Bard., Colin Whitby-Strevens requested a friendly amendment "...pending further consideration of the speed map by the IEEE 1394a-1999." David Wooten suggested the friendly amendment be withdrawn. The friendly amendment was withdrawn.

Vote Taken: 9 favor; 0 opposed; 8 abstain

Moving on to agenda item 6.2, this is the register that states precisely what the PHY maximum speed supports. The state machine uses this value at self ID-time as the first value used during speed negotiation.

Jerry initiated some discussion as to whether the group believed it would be a good idea to (in a beta network) that when the speed field of the self-ID packet is 11b that the speed of the cable connection between the PHY and its parent node be contained in the MAX_SPEED register. Currently, the two bit field is set to 11b for anything above S400 (which is to be interpreted as "go read register three" for the speed information).

John Fuller suggested that if the MAX_SPEED register was written with the parent port speed it might make the intent of what was done in 1394a a bit more logical. Jerry commented that if the MAX_SPEED register is always read with a PHY Register Read packet, its contents will always be accurate. If it is read from the link with a PHY register Read (LREQ) there may be a synchronization problem. John Fuller said it would be best that text be added to the draft standard that words

After a bit more discussion, Colin Whitby-Strevens moved to that the MAX_SPEED register shall be hard wired to contain 11b for all "B" compliant PHYs. Seconded by Jerry Hauck.

Note to Colin: a general clean-up of the quantity of port speed registers in the PHY port register map is needed.

Vote Taken: 11 Affirmative; 0 Negative; 4 abstentions.

Colin moved that agenda item 6.3 be endorsed and done (e.g. eliminate the applicable role in table 11-1. Seconded by Jerry Hauck.

Vote taken: 5 affirmative; 0 negative; 9 abstentions.

Colin took the action to remove the table entry and he has done so.

Reports & Presentations

Copperheads - Max Bassler

There was a correction to the April minutes for the correct keying of the Beta/bilingual socket.

There was new material presented on the beta plug/socket:

There were controversial discussions concerning the use of two CSD pins on the proposal for resolving plug present, speed capability of the cable (<=S800, <=S1600 and <=S3200).

In response to Max's question "Are there any other (additional) requirements for the beta/bilingual socket/plug?" The group returned none to add to those presented. Plenary members were implored to review the Copperheads

presentation (either contained herein (see below) or by downloading their own personal copy from the ftp repository).

Max's presentation foils:



1394-Beta Connector Proposal Part 2

1999 June 07

Max Bassler

Dave Brunker

John Lopata

Molex - 1394-Beta Connector Proposal - 1999 June 07



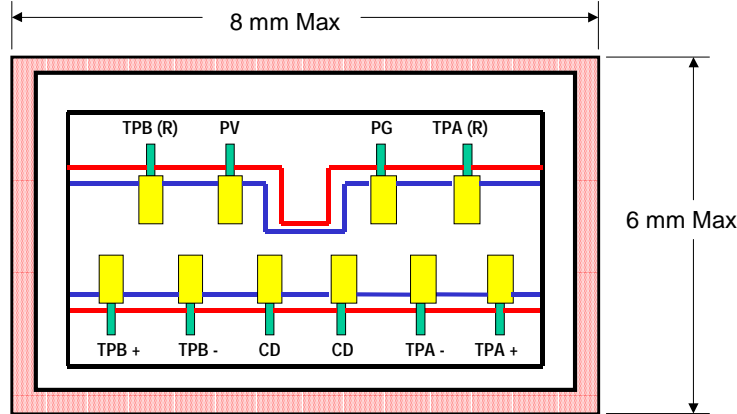
1394-Beta Connector Proposal

- **Electrical**
 - Voltage: **30 VDC** maximum
 - Current: **1.5 A** per contact
 - Data Rate: up to **S400-S3200**
 - Impedance: **110 +/- 25 Ohms** through a **100 ps** exception window
 - Cross Talk: **less than 5%**
 - Skew:
 - Intrapair < **10 ps**
 - Interpair < **15 ps**
- **Target Cost**
 - Connector: Equivalent to current high performance sockets
 - Cable Assembly: Equivalent to current high performance cable assemblies at given speeds (**S800, S1600, S3200**)

Molex - 1394-Beta Connector Proposal - 1999 June 07

1394-Beta Connector Proposal

(Bilingual will be keyed differently)



█ Cable Plug Movable Contact Position
 █ Fixed Contact Position PCB Socket

Molex - 1394-Beta Connector Proposal - 1999 June 07

1394-Beta Connector Proposal Pin Out



Note: Final determination of TPA (+/-) and TPB (+/-) pin position will be determined by the silicon pin out and routing.

- TPA + Twisted Pair A (Plus)
- TPA - Twisted Pair A (Minus)
- TPA (R) Twisted Pair A (Return)
- TPB + Twisted Pair B (Plus)
- TPB - Twisted Pair B (Minus)
- TPB (R) Twisted Pair B (Return)
- PV Power (Voltage)
- PG Power (Ground)
- CD Cable Detect
- CD Cable Detect

Molex - 1394-Beta Connector Proposal - 1999 June 07



1394-Beta Connector Proposal

Possible Cable Detect Pin States

1- No Connection- **Cable Presence detect for "Upstarts"**

2- Legacy Cable Systems- **Protocol**

1394-1995 6 Circuit Connector

1394a 4 Circuit Connector

3- High Speed Serial Data Cable Systems

S 800 maximum cable data speed

S1600 maximum cable data speed

S3200 maximum cable data speed

4- Future Designations

~~Security~~

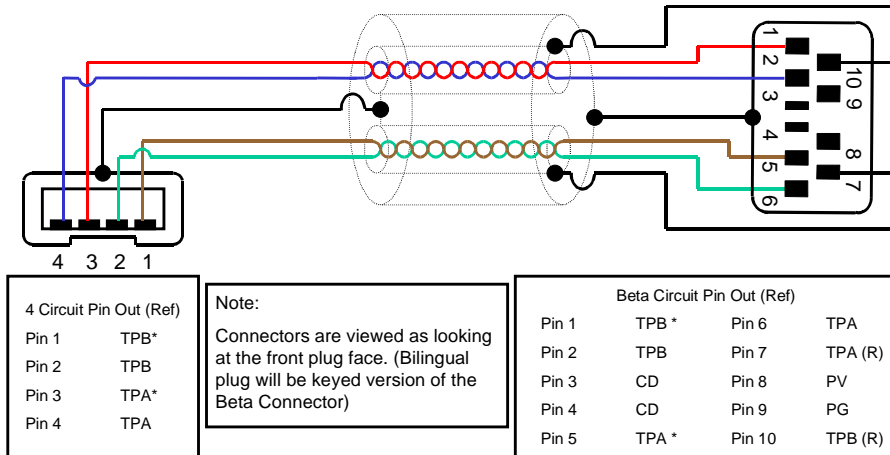
Manufacturers proprietary coding

(Note- Assumption is ALL cables will support legacy S400)

Molex - 1394-Beta Connector Proposal - 1999 June 07



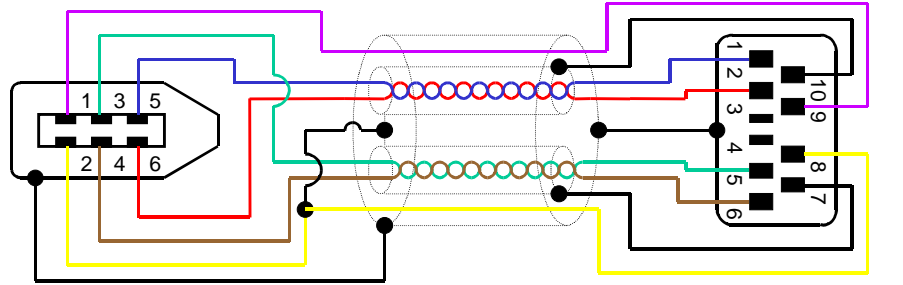
1394a 4 Circuit to Bilingual Cable Assembly (Legacy)



Molex - 1394-Beta Connector Proposal - 1999 June 07



1394-1995 6 Circuit to Bilingual Cable Assembly (Legacy)



6 Circuit Pin Out (Ref)	
Pin 1	VP
Pin 2	VG
Pin 3	TPB*
Pin 4	TPB
Pin 5	TPA*
Pin 6	TPA

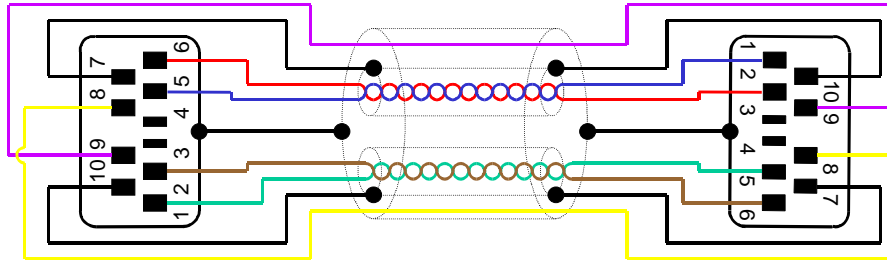
Note:
Connectors are viewed as looking at the front plug face. (Bilingual plug will be keyed version of the Beta Connector)
Power is mandated in this cable

Beta Circuit Pin Out (Ref)			
Pin 1	TPB *	Pin 6	TPA
Pin 2	TPB	Pin 7	TPA (R)
Pin 3	CD	Pin 8	PG
Pin 4	CD	Pin 9	PV
Pin 5	TPA *	Pin 10	TPB (R)

Molex - 1394-Beta Connector Proposal - 1999 June 07



Beta to Beta Cable Assembly



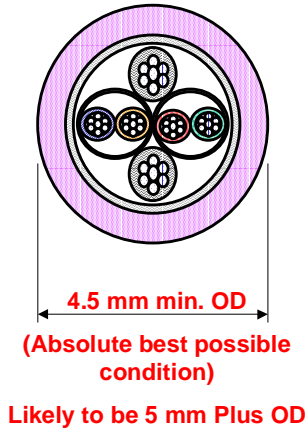
Note:
Connectors are viewed as looking at the front plug face.
Power is mandated in this cable

Beta Circuit Pin Out (Ref)			
Pin 1	TPB *	Pin 6	TPA
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Pin 3	CD	Pin 8	PG
Pin 4	CD	Pin 9	PV
Pin 5	TPA *	Pin 10	TPB (R)

Molex - 1394-Beta Connector Proposal - 1999 June 07



Beta 2.0 Meter Cable Construction (Reference)



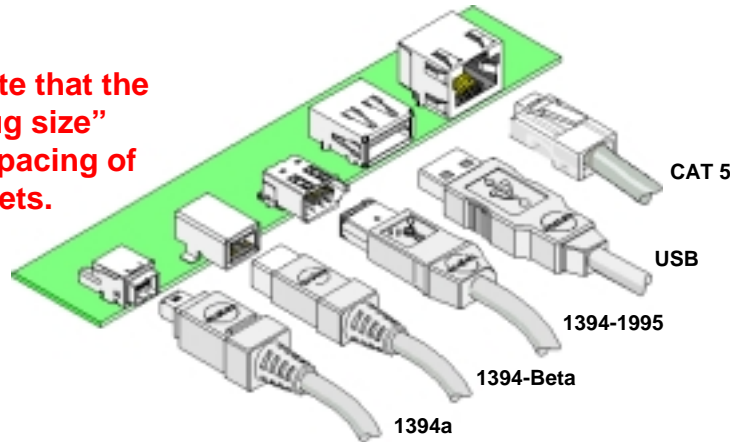
- Power Wires
 - Voltage [26 AWG]
 - Ground [26 AWG]
- Two High Speed Data Pairs
 - Twisted Pair [30 AWG]
 - Braided copper shield with polyester tape isolation
- Outer Shield
 - Braided copper shield with polyester tape isolation from the internal conductors

Molex - 1394-Beta Connector Proposal - 1999 June 07



1394-Beta Connector Proposal (Connector size reference)

Please note that the "cable plug size" dictates spacing of PCB sockets.

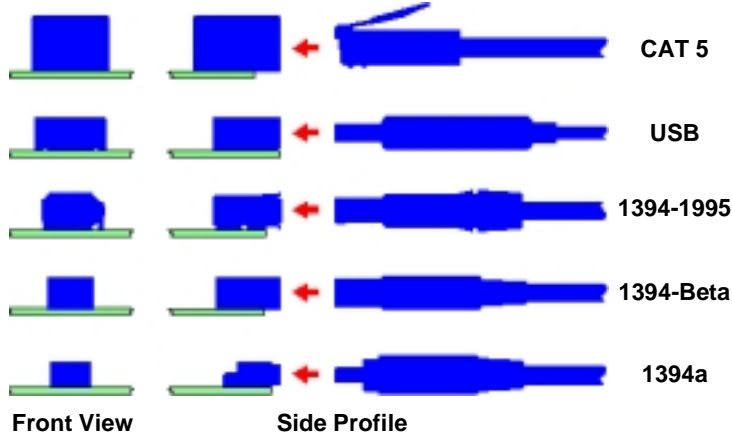


Molex - 1394-Beta Connector Proposal - 1999 June 07



1394-Beta Connector Proposal

(Connector size reference)

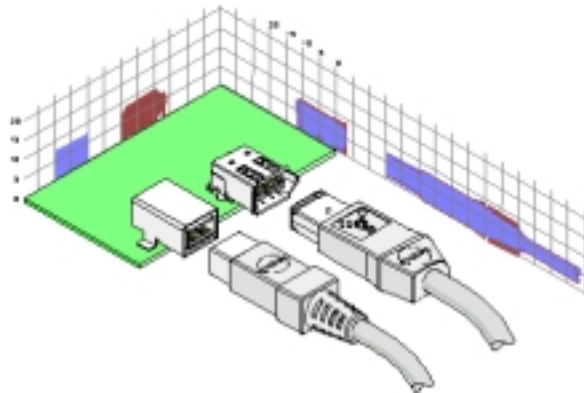


Molex - 1394-Beta Connector Proposal - 1999 June 07



1394-Beta Connector Proposal 1394-Beta and 1394-1995

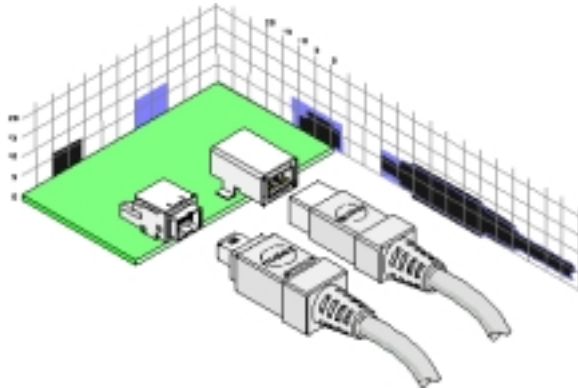
(Connector size reference)



Grid = 5 mm per division

Molex - 1394-Beta Connector Proposal - 1999 June 07

1394-Beta Connector Proposal 1394a and 1394-Beta (Connector size reference)



Grid = 5 mm per division

Molex - 1394-Beta Connector Proposal - 1999 June 07



1394-Beta Connector Proposal

- The Copperheads will be closing the requirements for the Beta/Bilingual connector after 14 days of this posting
- Please review and send any additional comments to the “Copperheads reflector”- copperheads@zayante.com
- All “red” text inputs are updates and feedback during the 99/June/7-8th IEEE 1394b meeting

Molex - 1394-Beta Connector Proposal - 1999 June 07

PHY/Link Electricals - Tony Foster

Voltage swing/signaling shall be 3.3 volts for the foreseeable future (5 years?) when considering the parallel PHY/Link interface.

All integrated circuit processes in foreseeable future 3.3 Volt I/O pads (implying multiple power supply sources)

Isolation mode - same time constants (nothing changes from IEEE 1394a-1999)

Set up and holds are new: rise/fall times; slew rate instead of using 10 to 90% for the fall and rise times, they have been changed to V_{IL} and V_{IH} . Tony will email setup and hold budget for link and PHY to the reflector.

PIL/FOP specs: 1394b signals; side band signals - "LREQ" and "PINT"

Must return to a "Z" state after a transition on the Link-PHY interface when operating in isolation mode. All signaling diagrams are "logical" signaling in presentation and the actual signal on the wire may be different dependent upon your implementation (e.g. isolation mode).

Plenary members are strongly encouraged to read the PHY/Link chapter in the latest draft standard (0.60) - there have been a number of changes and additions.

Tony's presentation foils:



1394B June Phy Link Electrical

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DC/AC Signal Swings

- Assume all IC processes for foreseeable future support 3.3V I/O signaling.
- Advantages
 - reuse of existing 1394.a specification
 - supports isolation with 1394.a model
- Disadvantages
 - requires multiple power supplies for $V_{core} < 3.3V$

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Setup and Hold times

- All setup and hold times are changed
 - Link Phy interface running at 100Mhz
 - Rise/Fall time is specified as minimum “slew rate”
 - Rise/Fall specified from V_{IL} to V_{IH}
- I will email the timing delays and skews that contribute to the Setup and Hold time analysis

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PIL to FOP signals

- Integrated Phy to Fan out Phy
 - Primary channel is 1394B “cable” specification
 - Some registers not available through 1394B Phy port
 - Use “sideband” signals to access register data
 - “LREQ” and “PINT” functions
 - Sideband signal electrical specs will be added to draft
 - signal levels for these signals
 - timing of the signals and clocking

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Link-Phy Isolation 1394B

- Isolation leveraged from 1394.a
- link-Phy bus uses data padding for $sXXX < s800$
 - Logical signals are “padded”
 - Physical signals use first clock period
 - Remaining logical time is Physical Z state
- The isolation barrier circuits in the draft
 - Control of the Schmidt trigger center critical

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Setup&Hold Measurements

- Signal measurement fixtures specified

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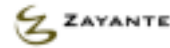
1394b BOSS Arbitration - Colin Whitby-Strevens

This presentation was delivered at the most recent 1394 Trade Association Developer's Conference.



1394b Boss arbitration

Michael Johas Teener
Colin Whitby-Strevens
Jerry Hauck



Outline

- 1394a: improvements in efficiency
 - Arbitration acceleration
 - Reset improvements
 - Suspend/resume
 - Miscellaneous
- 1394b: the next step in speed and distance
 - New connection model
 - Additional media
 - Arbitration improvements
 - Miscellaneous



Summary

- IEEE 1394-1995 arbitration incurs overheads
 - arbitration gaps
 - do not scale
- IEEE 1394a introduces techniques to reduce overheads in certain cases
 - fly-by concatenation, ACK-accelerated arbitration
- IEEE 1394b overlaps arbitration with packet transmission
 - scheme known as Boss
 - allow pipelining of arbitration requests
 - removes need for gaps

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Background: 1394-1995 link operation

- wait for idle bus
- arbitrate
- end packet
- responder sends ack



(wait for ack to arrive)

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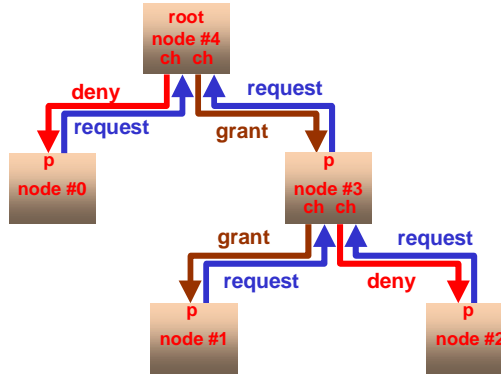
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1394-1995 arbitration - 1

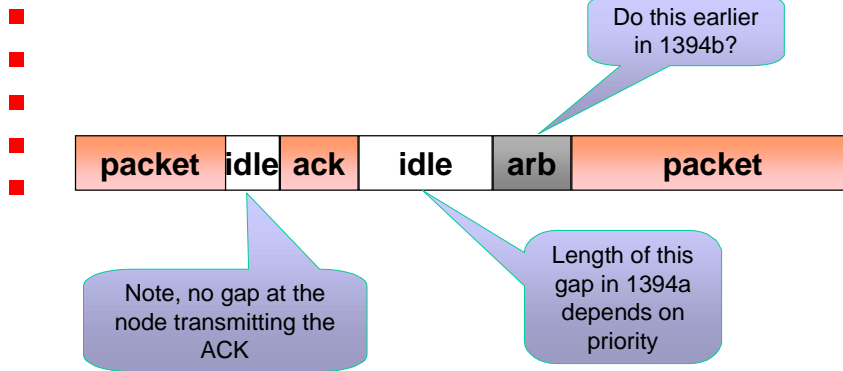
Every node has the capability to take arbitration decisions.

- One node is elected as root
- root
 - nodes along the path to the root arbitrate between their children (when granted by their parents)
 - root takes the final arbitration decision

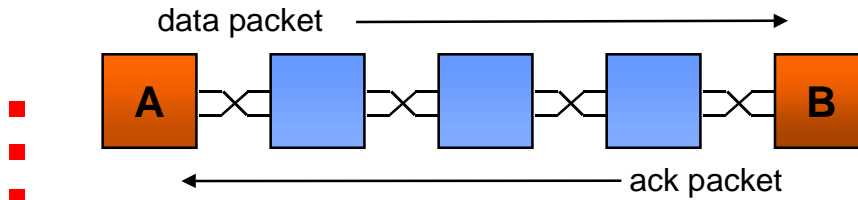


1394-1995 arbitration - 2

- In 1394-1995, arbitration for the next transmission has to wait until the bus goes idle



Bus timing for asynchronous arbitration

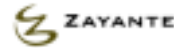


- Subaction gap time must be greater than round trip delay time for most distant pair of nodes on a 1394 bus
- For asynchronous arbitration, waiting a Subaction gap time after passage of last packet before start of new arbitration ensures that new arbitration will not interfere with an ack

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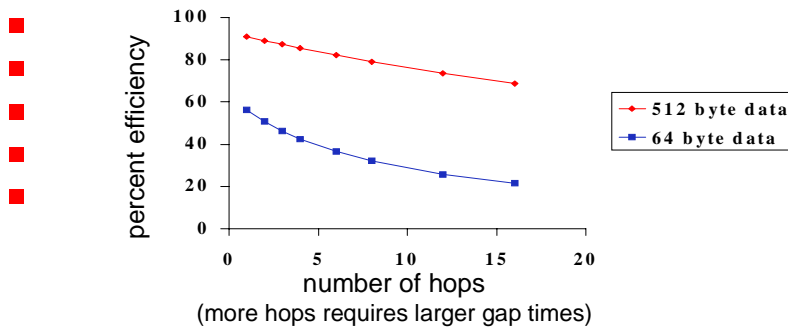


Efficiency effects of gap time

(Asynchronous bandwidth without 1394a improvements)

- OK for large packets, terrible for small ones

100 Mbit/sec



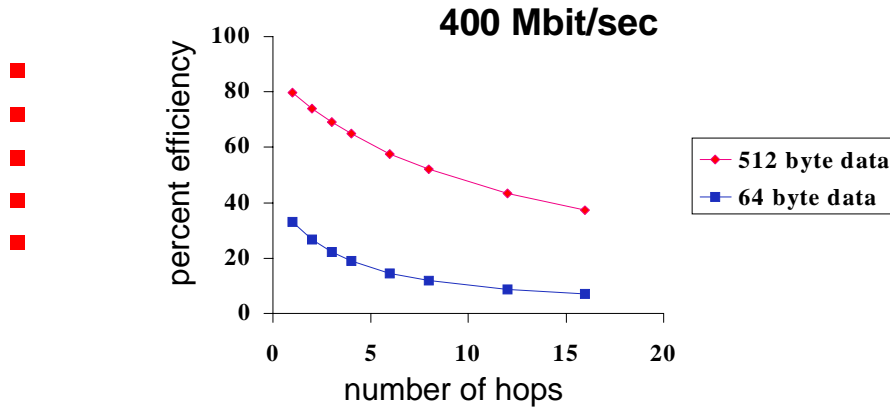
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Gets worse for high speeds



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Solutions from P1394a

- Ack accelerated arbitration
- Fly-by concatenation
- Priority arbitration

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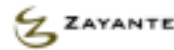
P1394b: the next step

- Full backwards compatibility with 1394-1995 and P1394a
- Extend speed ranges to 800 and 1600 Mbit/sec
 - 3200 Mbit/sec and higher architectural support
- • Support long distance systems
 - UTP5 @ S100 for 100m
 - Plastic optical fiber (POF) @ S200 for 50m
 - Hard-polymer-clad fiber (HPCF) @ S200 for 100m
 - Multimode glass fiber (GOF) @ S3200 for 100m
- • All P1394b connections operate using full-duplex signaling
 - can we take advantage of this?

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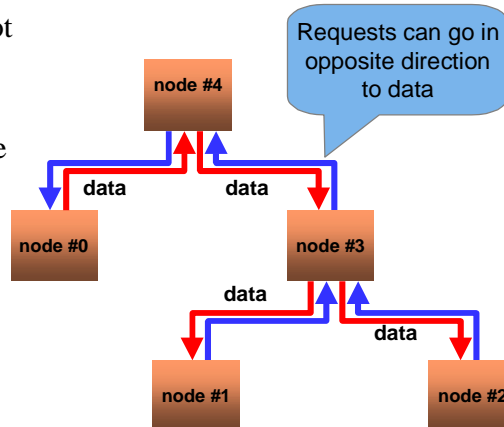
11

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1394b arbitration - 1

- In general, there's not a reverse path to the root
- • But there is a reverse path to the node which is currently transmitting data
- • Arbitration requests don't need to wait until a gap after data



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1394b arbitration - 2

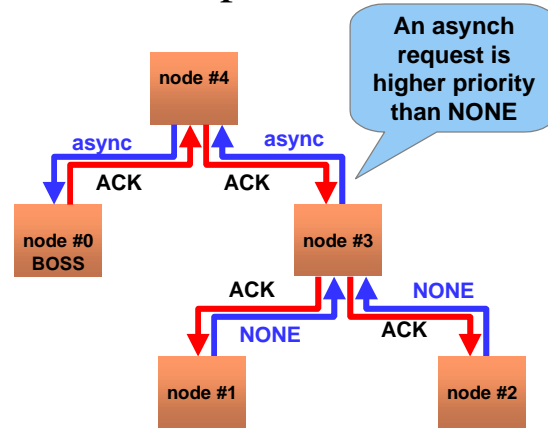
- In 1394b, arbitration requests are routed along the reverse path to the node which is currently transmitting data
- • This node is known as the BOSS (Bus Owner / Supervisor / Selector)
- • This node takes the final arbitration decision
- • Boss can issue a grant at the end of a sub-action
 - – further rules to allow simple implementation of border nodes (nodes which have some ports operating using 1394-1995 or 1394a DS signaling)

1394b arbitration - 3

- Arbitration requests are allocated priorities
 - nominal NONE requests
- • A node listens on all ports and its local link for arbitration requests
 - – one port or the link may be sending it data
 - – identifies the highest priority from among the various requests being received
- • A non-Boss node transmits the highest priority arbitration request on all ports which it is not using to transmit data
 - at least one, only one if the node is repeating data
- Boss node grants the highest priority at the end of the subaction

1394b arbitration simplified example - 1

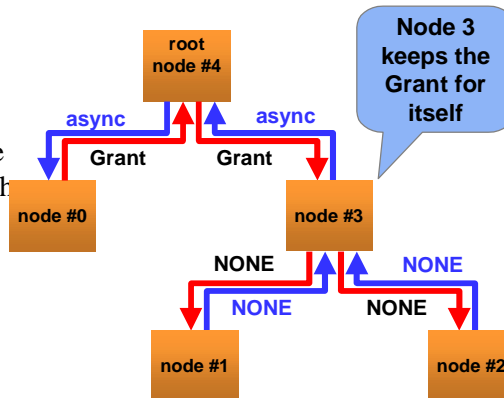
- Boss is transmitting an ACK packet
- Node 3 has a local async request
- This is higher priority than the requests being received on its ports
- Async request is routed to the Boss



Note: there are several different Asynchronous requests - see next few slides

1394b arbitration simplified example - 2

- After the end of the ACK packet, Boss immediately transmits a Grant
- Each node routes the Grant to the port with the highest priority request
- Or perhaps keeps it for itself (if no port has a higher priority than the local link)



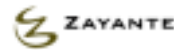
Fairness

- 1394b retains the concept of a fairness interval
 - in 1394a, a node has to wait for an arb reset gap
- A node may pipeline a request for the next interval
 - as well as making a request for the current interval
- Implemented using ODD and EVEN intervals
- A node may arbitrate for the CURRENT fairness interval and/or the NEXT_EVEN or the NEXT_ODD
- In the EVEN interval, Boss will grant NEXT_EVEN requests (pipelined during the previous ODD interval), then CURRENT requests and
- In the ODD interval, Boss will grant NEXT_ODD requests, then CURRENT requests

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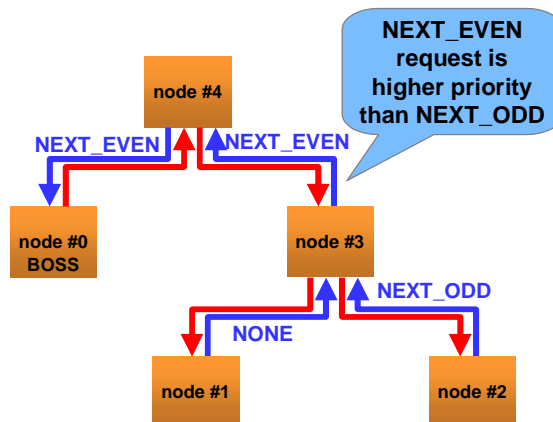
17

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Fairness - example

- EVEN phase
- Node 2 has had its turn, but pipelines a request for the next phase (ODD)
- Node 3 still has a local request for this phase (EVEN)
- This request can be granted



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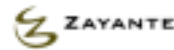
Fairness - advancing the interval - 1

- If there are no requests for the current interval, then Boss will advance to the next interval
 - issues an ARB_RESET_EVEN or ARB_RESET_ODD token
 - avoids having to wait for an arb_reset_gap (the longest type of gap in 1394a)
- ARB_RESET_X token is propagated to all nodes
 - update the local knowledge of the current interval
- Boss rules ensure that all nodes remain synchronized

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Fairness - advancing the interval - 2

- Assume in the EVEN interval
- Boss decides to advance to ODD
- Must ensure that all nodes have seen the token and are in ODD before advancing to EVEN again!
 - Use NONE_EVEN and NONE_ODD requests
 - If a node has no requests to make, then it transmits the NONE_X request for the phase it thinks it is in.
- If a node is in the EVEN phase, but receives a NONE_ODD, this means that the other node has not yet caught up
 - node must forward the old phase request in preference to a NODE request for its phase.

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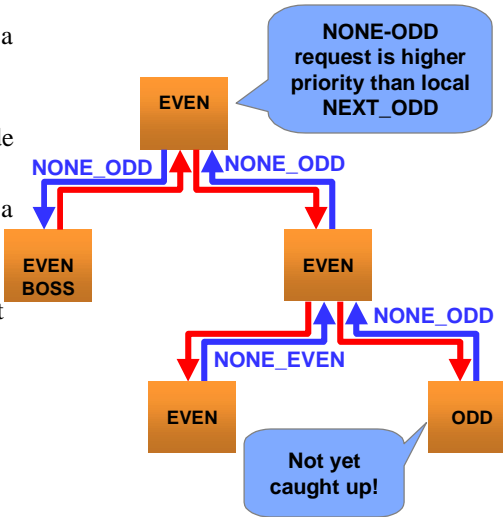
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Advancing the interval - 3

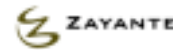
- If in the EVEN phase, then a NONE_ODD takes priority over a NONE_EVEN
 - - wait for some other node to catch up
- If in the EVEN phase, then a NONE_ODD takes priority over a NEXT_ODD
 - - cannot move to the next interval to grant the NEXT_ODD until all nodes have caught up



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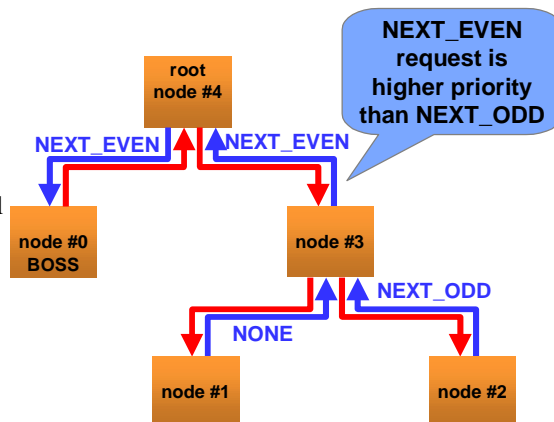
21

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Fairness - example - 2

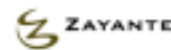
- EVEN phase
- Node 2 has had its turn, but pipelines a request for the next phase (ODD)
 -
 -
- Node 3 still has a local request for this phase (EVEN)
 -
 -
- This request can be granted



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Boss privileges at subactions

- A node receiving a directed asynchronous subaction responds immediately with an ACK
- So although the node transmitting the asynchronous packet is nominally the Boss, it cannot exercise Boss privileges immediately
- • In effect, it loses the privileges, as the node transmitting the ACK
- • becomes Boss by virtue of being the new transmitting node
- • Boss can only issue a Grant at the end of a subaction, which occurs after transmitting
 - – an ACK packet
 - – an isochronous packet
 - a PHY response packet
 - a PHY packet which does not expect a PHY response packet

Isochronous arbitration

- Allow requests for the current isochronous phase and pipelining for the next
 - Mechanism very similar to asynchronous arbitration
 - – Use ISOCH_EVEN and ISOCH_ODD requests
- • To start an even isochronous cycle, the cycle master issues a CYCLE_START_EVEN token
 - – Boss will then grant ISOCH_EVEN requests
 - – Other nodes will prioritize ISOCH_EVEN requests over ISOCH_ODD requests
 - – When there are no ISOCH_EVEN requests left, then Boss will grant asynchronous requests

Combining isochronous and asynchronous requests

- Encoding scheme allows a single token to contain both an isochronous arbitration request and an asynchronous arbitration request
- A node may make a single isochronous request and a single asynchronous request
 - – A node with no isochronous requests generates ISOCH_NONE
- • If it has no requests for the current phase (either isochronous or asynchronous) then it can pipeline a request for the next phase
- • When forwarding requests, a node gives priority to requests for the current phases over requests for the next phases

When there are no requests or Grants

- If Boss has no requests, then it advances the fairness interval and issues a grant to its parent,
 - – which, if it has no requests, then passes the Grant onto its parent
- • In an idle bus, the root becomes Boss
- • Root has a timeout for bus inactivity
 - – Grant may be lost due to transmission error
 - – Root restores bus activity by generating a grant

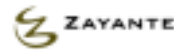
Hybrid 1394-1995/1394a/1394b buses

- A *border node* is one which has some ports and/or its link operating as described in this presentation, and some ports and/or its link operating according to 1394a signaling and arbitration rules
-
- • Border operation has to ensure that gaps are preserved on the legacy side
- – some Boss details are not the most obvious in order to allow border nodes to meet these constraints
-
- Use a LEGACY request to indicate to the Boss that a request has been received from a legacy domain which can be granted
- Separate presentation to describe Border operation in detail

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Hybrid Buses and the Border PHY A P1394a Approach



Jerry Hauck
Michael Johas Teener
Colin Whitby-Stevens

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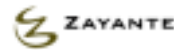


P1394a Arbitration Tutorial A Refresher



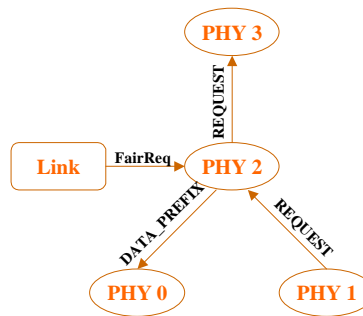
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P1394a PHY Arbitration Request Rules

- A request from a child port is automatically and immediately forwarded towards the root. Other children ports receive DATA_PREFIX.
- Requests from the link:
 - IsoReq: Immediately forwarded
 - FairReq or PriReq: forwarded at
 - Known end of subaction (ack)
 - Gap = Subaction + Arb Delay
 - Gap \geq Arb Reset + Arb Delay



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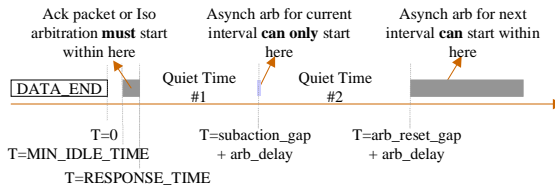
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P1394a Arbitration Quiet Windows

To ensure consistent, bus-wide detection of gaps, legacy arbitration has quiet intervals during which arbitration must not be initiated:

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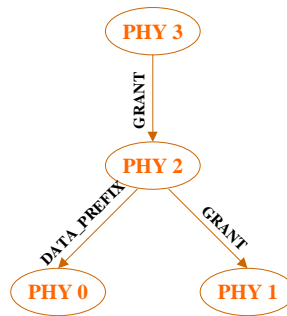


P1394a Grants

Explicit “Loud” Grant

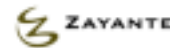
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- Grant traverses downward from root along path to requesting node.
- All branches off of “chosen” path are held inactive with leading DATA_PREFIX.

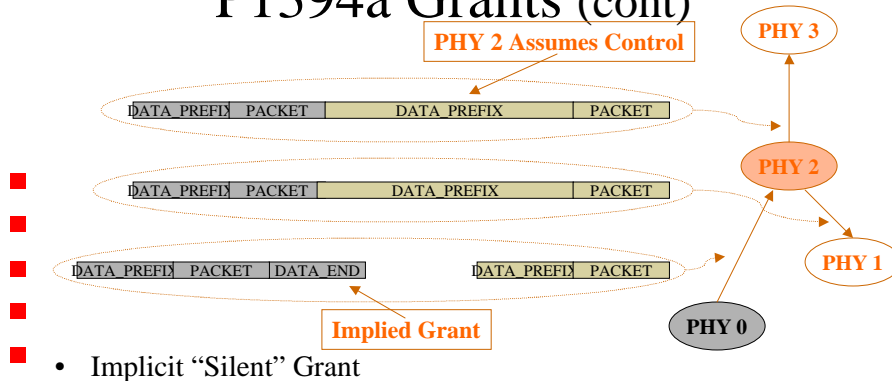


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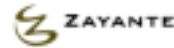
P1394a Grants (cont)



- • Implicit “Silent” Grant
 - After packet transmission, DATA_END traversing upwards along the path to the root is an implied GRANT
 - Parents noting DATA_END can perform fly-by concatenation and assume control of the bus.

6

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P1394a Bus Phases

- • Isochronous Interval
 - Begins with a Link-issued Cycle Start Packet
 - Concludes when no more isochronous arbitration occurs, causing a subaction gap to elapse on the bus
- • Fairness Interval (Asynchronous)
 - Active whenever not in the isochronous interval
 - Fairness interval boundaries marked with arbitration reset gaps which occur when no asynchronous arbitration remains.

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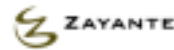
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BOSS: Reviewed and Slightly Revised

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Establishing BOSS^{ship}

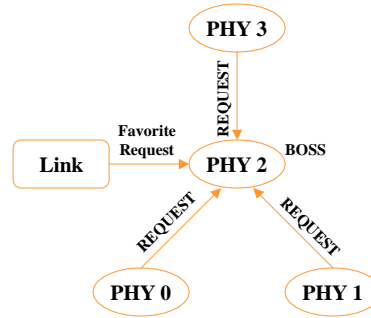
- When does a PHY become BOSS?
 - Any beta/border PHY first originating a packet into a given beta cloud is BOSS of that local cloud, immediately.
 - A PHY which receives an explicit or implicit GRANT is BOSS.
 - The “local root” of a cloud automatically assumes BOSS^{ship} after any extended period of inactivity.
- When does a PHY surrender BOSS^{ship}?
 - Whenever a packet is received from a beta-mode port, the receiving PHY ceases to be BOSS.
 - When an explicit or implicit GRANT is issued, the issuing PHY ceases to be BOSS.

9

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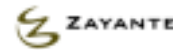
BOSS Request/Grant Rules

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- Current or pipelined requests are issued by P1394b Links
 - PHY's constantly forward favorite asynch and favorite isoch requests received from attached link and any cable ports towards the current BOSS.
 - At the established end of a subaction, the current BOSS immediately grants any in-phase request.



10

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Types of BOSS Grants

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- Explicit, Subaction Completion Confirmed
 - Explicit-Loud
 - Issued after the end of a subaction in response to an active, in-phase asynch, isoch, or legacy request
 - Granted port sees GRANT control symbol

DATA_PREFIX	PACKET	GRANT
-------------	--------	-------
 - Denied ports see DATA_PREFIX control symbols

DATA_PREFIX	PACKET	DATA_PREFIX
-------------	--------	-------------
 - Explicit-Quiet
 - Returns control to parent (and ultimately local root) at the end of a subaction when no in-phase asynch, isoch, or legacy requests remain
 - Granted port (parent) sees GRANT control symbol

DATA_PREFIX	PACKET	GRANT
-------------	--------	-------
 - Denied ports (children) see DATA_END

DATA_PREFIX	PACKET	DATA_END
-------------	--------	----------
 - Implicit, Subaction Completion Unconfirmed

DATA_PREFIX	PACKET	DATA_END
-------------	--------	----------

 - Returns control to parent (and ultimately local root) when subaction has not yet concluded. Local root has responsibility to time-out (i.e., ACK-MISSING)
 - All ports see DATA_END, parent port interprets as an implicit grant.

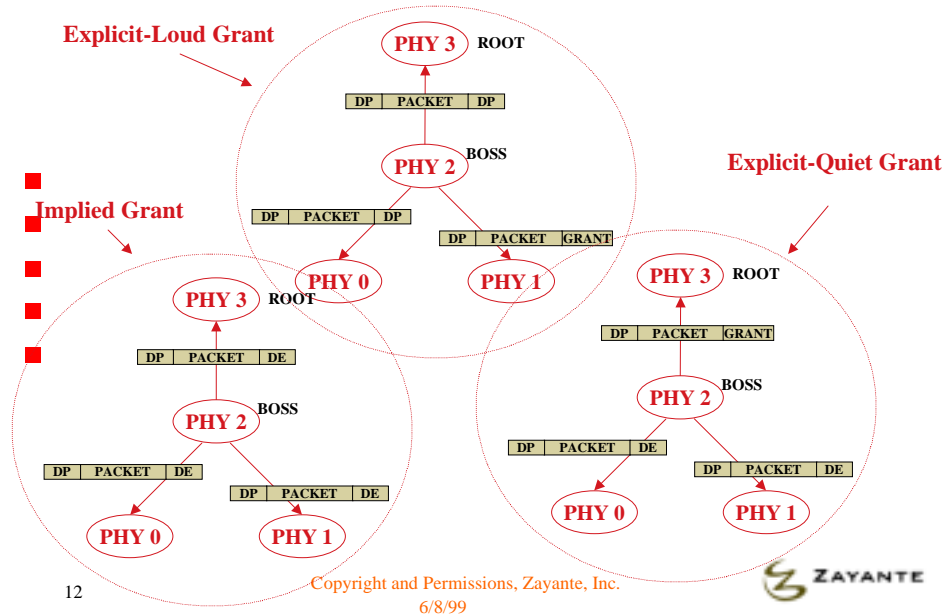
DATA_PREFIX	PACKET	DATA_END
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11

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Grants Illustrated

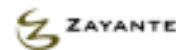


12

When BOSS is Permitted to Transmit

- Explicit Grant
 - End of subaction has been explicitly marked, it is safe for BOSS to use received GRANT for any in-phase request.
- Implicit Grant
 - End of subaction has *not* been communicated. If receiving BOSS can independently determine that the subaction is concluded (e.g., bus is in isoch phase or last packet was an ack in the asynch phase, or LEGACY request from LINK), GRANT can be used accordingly.
- Unarbitrated
 - PHY can assume BOSS*ship* immediately and begin transmitting an ACK or a PHY response packet.

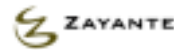
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P1394b Bus Phases

- Isochronous Interval
 - Begins with P1394b link issues a Cycle Start packet *and* a CYCLC_START_ODD/EVEN token.
 - Concludes when current BOSS has no favorite in-phase isoch request to grant.
 - BOSS marks conclusion of interval by issuing ASYNC_START token.
- Fairness Interval (Asynchronous)
 - Active whenever not in the isochronous interval
 - Fairness interval boundaries marked by current BOSS with ARBRST_EVEN/ODD token when no favorite in-phase asynchronous requests remain.

14

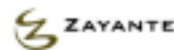
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Summary of Proposed Border

Feature	P1934a	Border	Beta-Only
Gap Timer	✓	✓	
Gap Tokens		✓	✓
QuietArb Windows	✓	✓	
Retractable Requests	✓	✓	
Pipelined Requests		✓*	✓
Explicit-Loud Grant	✓	✓	✓
Explicit-Quiet Grant		✓*	✓
Implicit Grant to Parent/Root	✓	✓	✓
Accel/Decel Timer	✓	✓*	
DATA_PREFIX Extension		✓	✓

Note: ✓ * signifies an optional feature for a simple long-haul repeater

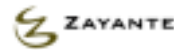
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Detailed Proposal Border PHY Theory of Operation

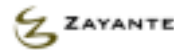
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P1394b Scope

- P1394b fundamentally offers an enhanced PHY layer specification for the family of IEEE1394-1995 based protocols.
- Changes to higher layers, services, and programming models are strongly discouraged and avoided (enhanced arbitration services between PHY and Link are exception)
- As a result, certain PHY Layer indications are expected/required for proper LINK and TRANS layer operation whether the underlying bus is composed of P1394a PHYs, P1394b PHYs, or both ...

17

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Required PHY Event & Data Indications

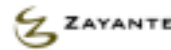
Regardless of PHY flavors present in a connected bus, certain PH_EVENT.indication's and PH_DATA.indication's are required. Of interest to the hybrid topology discussions:

- – BUS_RESET_COMPLETE, marking the end of the self-ID phase of bus configuration
- – SUBACTION_GAP marking the end of an isochronous period or indicating a missing ACK packet
- – ARBITRATION_RESET_GAP marking the boundaries of fairness intervals

For proper operation of higher layers and fulfillment of the programming model (isoch period batched before asynch), these indications must be faithfully synchronized across all nodes on a bus.

18

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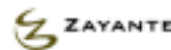
Communicating PHY Indications BOSS vs Legacy

PHY Indication	BOSS (Token)	Legacy (Gap)
End of Self-ID	ASYNC_START(?)	subaction gap
End of Isoch Interval	ASYNC_START	subaction gap
Missing ACK <small>(only needed at subaction initiator)</small>	ASYNC_START(?)	subaction gap
Boundary of Fairness Interval	ARBRST_ODD/ ARBRST_EVEN	arb reset gap

BOSS and Legacy arbitration algorithms have different ways of communicating/synchronizing PHY Indications across a bus and ultimately to attached nodes ...

19

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Hybrid Bus Problem Statement #1

Synchronizing PHY Indications

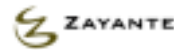
PHY Indication	BOSS (Token)	Legacy (Gap)
End of Self-ID	ASYNC_START(?)	subaction gap
End of Isoch Interval	ASYNC_START	subaction gap
Missing ACK <small>(only needed at subaction initiator)</small>	ASYNC_START(?)	subaction gap
Boundary of Fairness Interval	ARBRST_ODD/ ARBRST_EVEN	arb reset gap

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... Consequently, a hybrid bus requires both BOSS and Legacy style indications to “fire” for each occurrence of a given PHY indication.

20

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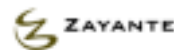
Hybrid Bus Problem Statement #2

Beta-Only Arbitration Constraints

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- Beta-only PHYs, as an assumption, do not have configurable gap timers. If any timeout period is implemented, it is assumed to be fixed and set for a maximum sized topology. As a consequence, attempting to set the gap_count on a beta-only PHY has no effect.
 - BOSS currently defines asynchronous and isochronous pipelined requests. The BOSS PHY needs to understand the bus phase (isoch or asynch, even or odd) before it can grant an incoming request.

21

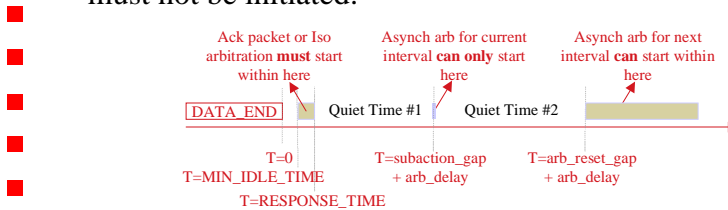
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Hybrid Bus Problem Statement #3

Legacy Arbitration Constraints

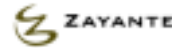
- To ensure consistent, bus-wide detection of gaps, legacy arbitration has quiet intervals during which arbitration must not be initiated:



- Null packets (consisting of DATA_PREFIX & DATA_END & IDLE) have a minimum specified duration of ~440 ns (140 + 260 + 40)

22

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Proposed Solution - Overview

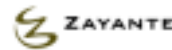
Synchronizing Legacy Gap Periods with BOSS Tokens

Summary: To synchronize Legacy gap indications with BOSS token indications:

- D/S clouds are prevented from timing gaps during Beta-only transmissions
- Beta-only PHYs are prevented from issuing gap tokens in a hybrid network (since they don't know about legacy gap timings)
- A border PHY will guarantee a gap token is generated whenever a corresponding gap period has expired within the D/S cloud and, by extension, in all D/S clouds connected to the bus

23

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Detailed Solution

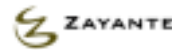
Preventing Timing of Gaps during Packet Transmission
 Particularly during beta-only traffic, we need to make sure that legacy devices don't detect any gaps.

(Example failure: during isoch transmission of beta-only packets, occurrence of a subaction gap in the D/S cloud would cause legacy nodes to fall into the asynch period too quickly and perhaps before their own isoch transmissions occurred.)

- – Legacy formatted packets in a beta cloud are repeated by a border directly into any D/S cloud as normal (with DATA_PREFIX replacing the payload if the speed is too great)
- – For beta-only packets, a border will begin generating DATA_PREFIX. Since the border must meet minimum DATA_PREFIX/DATA_END timings, and can not predict when the next legacy packet will arrive, it can not safely release DATA_PREFIX at any arbitrary point. Instead, it holds DATA_PREFIX until a legacy packet arrives. The legacy packet is then simply tacked onto the end of the DATA_PREFIX which allows the D/S cloud to return to idle.
- – To ensure that the border PHYs don't get stuck in DATA-PREFIX, BOSS PHYs are required to issue a legacy null packet anytime the end of a subaction has been reached, there are no more in-phase requests to grant, and the last packet sent was not a legacy packet.

24

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Detailed Solution

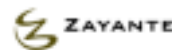
Preventing Beta-Only PHYs from Issuing Gap Tokens

Normally, a beta-only PHY will issue a gap token at the end of a subaction when no eligible in-phase requests remain to be granted. To prevent a beta-only PHY from doing so in a hybrid network,

- – Border PHY's announce their presence within a cloud by continued assertion of the BORDER_LOW arbitration request. With a priority above any out-of-phase NONE_* or NEXT_* requests, the BORDER_LOW request is guaranteed to propagate to the active BOSS before the BOSS would naturally attempt to issue a gap token.
- – If at the end of a subaction the BOSS has no more in-phase requests to grant and it detects the presence of a BORDER_LOW request, control is passed towards the local root (after transmitting any necessary null packet to "free" the border nodes stuck in DP). No gap token is issued and the bus will fall IDLE.
- – Note that a BORDER_LOW "request" is never actually granted.

25

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Detailed Solution

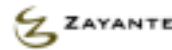
Guaranteeing Legacy Gaps are Matched with Tokens

Border PHYs are responsible for issuing gap tokens whenever a relevant gap period is detected within the attached D/S clouds

- – With the presence of one or more BORDER_LOW requests in the network, border nodes reserve the exclusive right to issue gap tokens. If the duration of IDLE at a border reaches a gap timed threshold, that border will issue the corresponding gap token. A bus with multiple borders will end-up with duplicate gap indications as each of the border PHY's reach the gap timeout. This is of no concern given that the gap tokens are required to be idempotent.
- – When the local root (which has become the BOSS by default) receives a gap token, it can grant any request that is now in-phase. For example, if the ASYNCH_START token is generated in response to the detection of a subaction gap, the local root can grant any outstanding asynchronous requests immediately upon receipt of ASYNCH_START.

26

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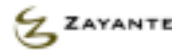
Detailed Solution

BOSS PHY's Unaware of Isochronous Interval

- The BOSS PHY normally uses the current bus phase (asynch/isoch) to determine which of the arbitration requests it is receiving are in phase and are eligible to be granted.
- When a given beta cloud has no P1394b links, it is possible that some/all of the beta PHY's will be unable to detect the start of an isochronous interval. Without P1394b links, no CYCLE_START_ODD/EVEN tokens are introduced into the beta cloud. Even a border node with a P1394a style link may not be able to infer the start of the isochronous interval if the link has no isochronous data to send.
- • Even though the beta PHY's are unable to track the bus phase, there may still be some isochronous packets to send which are being originated from a D/S cloud. To make sure that requests from the D/S cloud can be granted properly absent any bus phase information, a new LEGACY type request is created.
- • The LEGACY request has priority over any normal asynchronous or isochronous request. The LEGACY request in itself is neither asynch nor isoch. It communicates to the BOSS PHY that the originator of the LEGACY request has enough information to determine that it would be appropriate and valid to immediately grant the request.
- • The BOSS must either grant the LEGACY request or grant a higher priority request within ARB_RESPONSE_DELAY of receiving the LEGACY request to prevent gaps from occurring.
- • Unlike other BOSS request types, the LEGACY request operates like it does in P1394a and is expected to be withdrawn if denied.

27

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Detailed Solution

Guaranteeing P1394a “Quiet Times”

A semi-formal proof that P1394a quiet times are respected:

- Quiet Time #1 (Making sure a subaction gap is consistently heard)
 - Quiet time #1 only has to be respected when detecting ACK_Missing, the end of the isoch period, or the end of self-ID. The quiet period is at risk if ack packets arrive late, if isochronous arbitration is granted late, or primary asynchronous packet arbitration starts too quickly.
 - All nodes (including Beta-only) are required to meet RESPONSE_TIME and ARB_RESPONSE_DELAY, meaning data prefix or arbitration must be initiated by a responding PHY and repeated by intermediate PHYs within P1394a defined limits. The P1394a gap count analysis then applies and guarantees that ack packets and isochronous arbitration will be seen by all PHYs before the beginning of Quiet Time #1.
 - Specifically, after transmitting a packet that marks the end of a subaction, the current BOSS must grant the next PHY immediately. If there are no valid requests to grant, control is passed towards the local root. When the local root becomes BOSS, it must grant a request within RESPONSE_TIME or refrain from generating any subsequent grant until an ASYNCH_START token is received/generated by a border or until a LEGACY request is received. This is identical to the role a P1394a arbitration state machine plays in determining when it is okay to initiate arbitration.
 - Border PHYs forward D/S style requests as high priority LEGACY requests. Given that all D/S PHYs respect Quiet Time #1 when generating a LEGACY request, and given the beta-PHYs repeat legacy requests within ARB_RESPONSE_DELAY, LEGACY requests can only be present outside of the quiet period.

28

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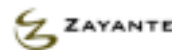
Detailed Solution

Guaranteeing P1394a “Quiet Times” (cont)

- Quiet Time #2 (Making sure an arbitration reset gap is consistently heard)
 - Quiet time #2 is at risk if a late arriving asynchronous request is granted, or if arbitration for the next fairness interval is granted too soon.
 - If the current BOSS (which should be the local root) has no requests to grant at the time a subaction_gap token (ASYNCH-START) arrives, it enters the second quiet period and will wait until a border signals the ARBRST_* event or until a LEGACY request is received.
 - Border PHYs forward D/S style requests as high priority LEGACY requests. Given that all D/S PHYs respect Quiet Time #2 when generating a LEGACY request, and given that beta-PHYs repeat legacy requests within ARB_RESPONSE_DELAY, LEGACY requests will only be present outside of the quiet period.

29

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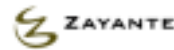


Border Request Mapping

- D/S to BOSS
 - RX_REQUEST from D/S (only heard between active packet transfers) is mapped to new BOSS LEGACY request immediately. Note that the border PHY may not know the phase of the bus (isoch or asynch), so it can not generally try to map RX_REQUEST to a BOSS asynch or isoch request.
- • BOSS to D/S
 - – The border PHY always respects the P1394a quiet times when forwarding eligible BOSS requests into the D/S cloud.
 - – The border PHY determines which requests are eligible based on the phase of the bus, asynch or isoch, even or odd. If the border PHY is unaware of the start of the isochronous interval, then it can't possibly be receiving any isochronous requests. (The presence of isochronous requests implies the presence of P1394b links which are required to send CYCLE_START_EVEN/ODD tokens.) If the border PHY thinks the bus is in the asynch phase when it isn't, the border will still refrain from forwarding asynch requests too soon since it is observing the quiet times and knows it can't arbitrate until after a subaction gap elapses.
 - – LEGACY BOSS requests are always eligible.

30

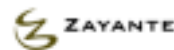
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Detailed Revisions to BOSS Operation in Support of Borders

31

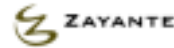
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BOSS Request Types and Priorities Asynchronous

Request Name	Priority Level	Comment
CYCLE_START_REQ	7	Used for a P1394b link-issued cycle start request, or to force control back to senior border when cycle start expected from parent D/S cloud
NEXT_ODD/EVEN	6	
CURRENT	5	
BORDER_LOW	4	Never granted, simply establishes presence of border PHYs
NONE_EVEN/ODD	3	
NEXT_EVEN/ODD	2	
NONE_ODD/EVEN	1	

32

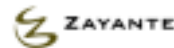
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BOSS Request Types and Priorities Isochronous & Legacy

Request Name	Priority Level	Comment
ISOCH_ODD/EVEN	4	
BORDER_LOW	3	Never granted, simply establishes presence of border PHYs
ISOCH_NONE	2	
ISOCH_EVEN	1	

- • Legacy Request
 - Has priority over all asynchronous and isochronous requests, regardless of current bus phase
 - Maybe coded as reserved configuration request or as reserved isoch request

33

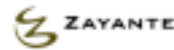
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Border-Imposed BOSS Requirements

- Beta-only PHYs must meet RESPONSE_TIME when generating ACK's or queuing in-phase isoch arbitration.
- Beta-only PHYs must repeat arbitration within ARB_RESPONSE_DELAY, particularly propagation of GRANT and DATA_PREFIX.
- • When explicitly granting a particular requesting port, other ports must start sending DATA_PREFIX to stop the timing of legacy gaps.
- • New LEGACY request type which is granted with a higher priority than asynch or isoch requests. It is granted or denied immediately without regard to bus phase. Furthermore, when it is denied, it will be withdrawn/cancelled as in P1394a. Due to the longer cables of P1394b and shorter packet sizes, some filtering of LEGACY requests may be required.
- • When no borders are present, current BOSS is expected to issue gap tokens immediately. Control of the bus is retained by ending previous packet with DP, generating token, and then ending with DE/GRANT as appropriate.
- • Packet ending symbols can now include DP, DE, or GRANT. All need +/- disparity versions. As a byproduct, concatenated packets are now defined for beta-only.

36

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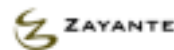


Observations/Axioms

- For a Beta-Only device, Link, if present, is Beta-style link and able to mark each and every end of subaction. If link is not beta-style, than PHY is border PHY by definition.
- • Explicit grant can only be issued after isoch if P1394b link is present. However, it can be issued after asynch by Beta phy (phy response packet) or by border node after ack even when a P1394b link is not present.
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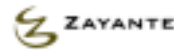
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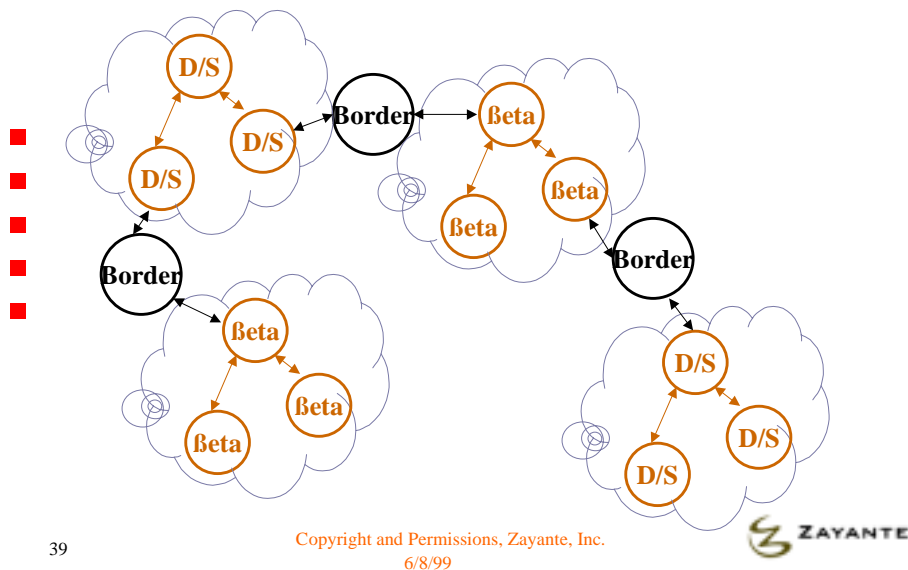
Issues for Later Discussion

- Loss of Synch
- Timeout of Beta-only root must be $>$ then
 - worst case subaction gap detection time and
 - token delivery time.
 -
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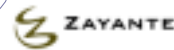
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Interactive Examples



39

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LOOP Healing - David Wooten

Progress is being made. This will not be in the critical path - soon. David said he will (in all likelihood) be something posted on the ftp site late next week for folks to begin to consider.

Colin pointed out that, during his report to the DVB group, their chairman pointed out that it would be a mistake to drop loop healing but it was more important to complete border node functionality first.

SPEC Completion Schedule

David stated his desire to go to first ballot review in October - therefore the specification must be complete by September.

Steve Bard moved that no technical material shall be added or removed from scope in the draft standard from this point forward without a two week review period by the plenary membership followed by a 2/3 super majority vote of those present in a plenary meeting to adopt or remove the technical material in question. Seconded by Jerry Hauck.

Points of clarification: Colin Whitby-Stevens inquired as to whether the intent of the 2/3 vote was to consider abstentions as NO vote. Both Steve Bard and Jerry Hauck concurred.

As a further point of clarification, the technical content currently not in the draft (but which has been exposed to the plenary and is work in progress for inclusion in the draft standard) are:

- 1) Beta/Bilingual connector
- 2) Loop healing
- 3) PIL/FOP and side band signals (PHY/Link interface stuff)

Work on these three topics will continue and completeness of that work will find its way into the draft prior to the draft standard revision released at the September meeting.

Vote Taken: 11 affirmative; 0 against; 1 abstain;

ACTION ITEM LIST:

AI#1: John Fuller, Jerry Hauck, David Wooten will investigate a resolution to the 1394b per port maximum speed registers - specifically: How does the value become loaded and how is the value preserved (as when the PHY power cycles, etc.). Report via e-mail on the reflector or at the next plenary.

AI#2: John Fuller - in regards to the AI#1, John will bring the subject of PHY register value preservation across power cycle events to a point of discussion at the next OHCI 1.1 meeting.

AI#3: Colin Whitby-Stevens to socialize on the "B-Reflector" the issue of whether to require all beta compliant PHY's shall report their self-ID speed bits as 11b. To be completed prior to the next plenary.

AI#4: David Wooten will form the ballot review committee.

AI#5: Colin Whitby-Stevens to ask Allistair why we need positive negative disparity of data_prefix and data_end. Report via e-mail or at the next plenary.

Meeting adjourned: 5:50 PM

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