

# Gbit Serial Bus

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The following is a group of foils presented by Keith Heilmann at the 1394B meeting held in Fort Collins CO. on 3/3/97. This represents IBM's proposal for a backward compatible IEEE-1394 gigabit extensions.

Any questions can be directed to Keith Heilmann or Michael Sorna.

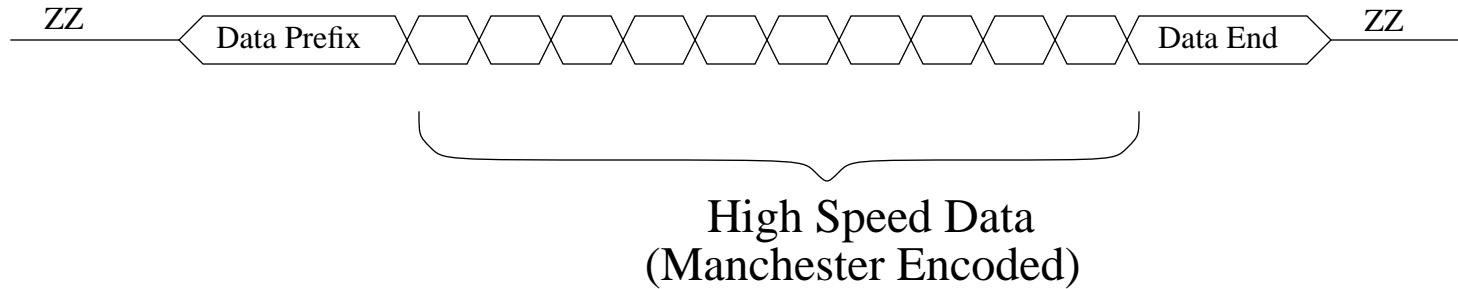
Mike can be reached at (914) 892-3425 or [sorna@vnet.ibm.com](mailto:sorna@vnet.ibm.com)

Keith can be reached at (914) 892-2413 or [heilmann@vnet.ibm.com](mailto:heilmann@vnet.ibm.com)

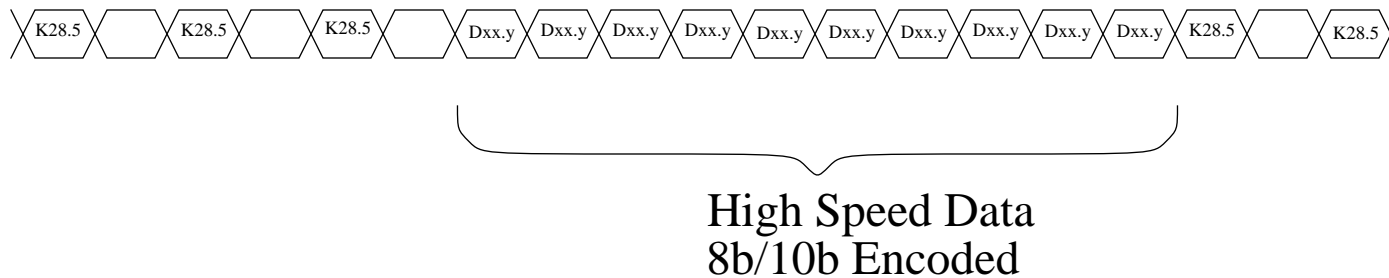
# Serial Bus Packet Format



1394-1995 (as root):



1394B Continuous 8b/10b code:



- 8K max packet at 800Mb/s
- No insertion or deletion of characters within a packet
- 20nS Arbitration character facilitates backward compatibility with 1394-1995

# 1394B Transmission Speed



**Table 1: Transmission Speed vs. Data Rate**

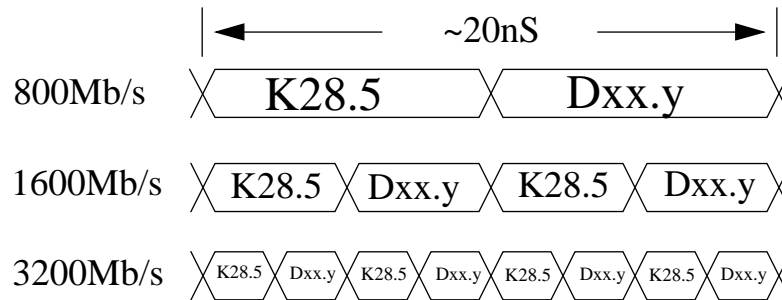
Generic Speed	Data Rate (Mb/s)	Transmission Bit Rate (Mb/s)	Transmission Bit Time (ns)
100	98.304	98.304	10.17
200	196.608	196.608	5.086
400	393.216	393.216	2.543
800	786.432	983.040	1.017
1600	1572.864	1966.080	0.5086
3200	3146.728	3932.160	0.2543

Concern: 800 & 400 Mb/s transmission bit rates are not integer multiples.

# 1394B Arbitration Format



## 2 Byte ordered sets for Arbitration signals



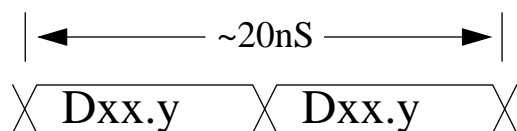
First Byte: Special K character (Recommend K28.5)

- Signifies the start of an arbitration ordered set
- Allows word synchronization

Second Byte: Arbitration code (decoded)



<u>Field</u>	<u>Significance</u>
A0	Arb_A_0 Arbitration signal
A1	Arb_A_1 Arbitration signal
B0	Arb_B_0 Arbitration signal
B1	Arb_B_1 Arbitration signal
SPD	Speed Code (Same as 1394a link request)
R	0 = 1394-1995 arbitration, 1 = extended use

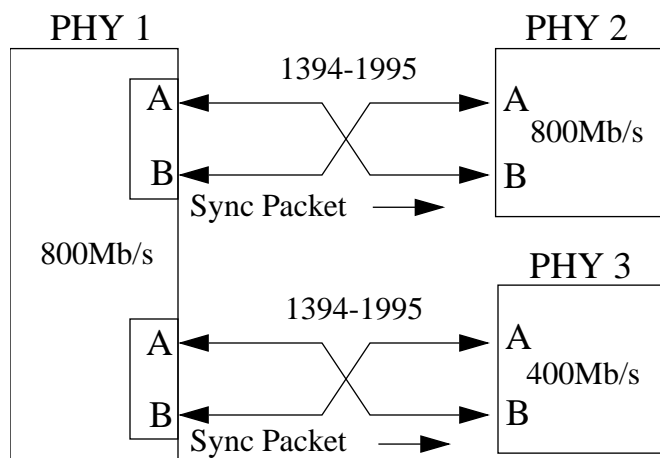
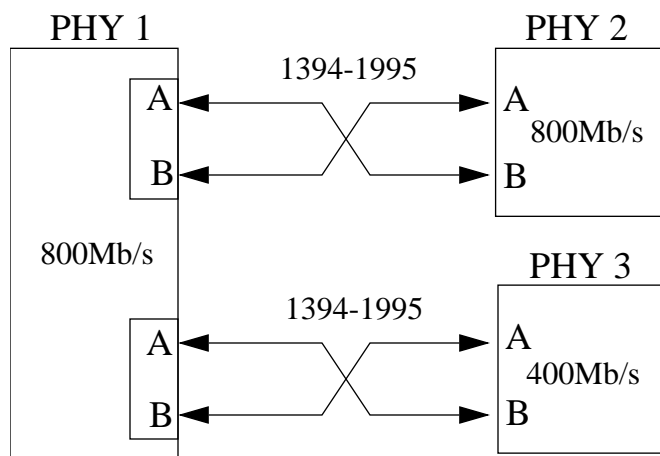


**Table 1: 2 Byte Data Format vs. Speed**

Speed (Mb/s)	Data Format
100	DD00 0000 0000 0000 <sup>a</sup>
200	DDDD 0000 0000 0000
400	DDDD DDDD 0000 0000
800	DDDD DDDD DDDD DDDD

<sup>a</sup> The “D” signifies a valid data bit for the given speed.

1600 Mb/s & 3200 Mb/s will transmit 4 bytes and 8 bytes respectively, within 20 ns similar to the arbitration format.

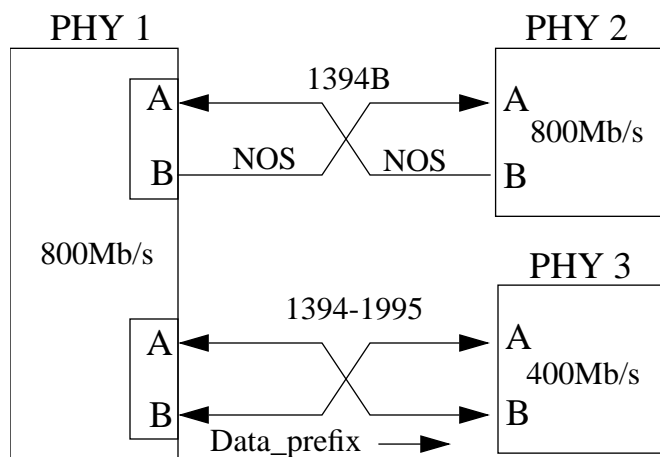


## Initializing the Bus:

- Normal 1394-1995 tree-id and self-id using 400Mb/s analog speed signalling. Actual PHY capability is reported in its SID packet.
- Record the peer speed for each port from the SID packet using the last SID packet received from your child when the PHY receives ident\_done. An algorithm created for digital speed signalling is required to identify parents SID packet.
- All PHYs enter A0 (idle) communicating with 400Mb/s 1394-1995 analog signalling.

## Sending PLL Rcv Sync Packet:

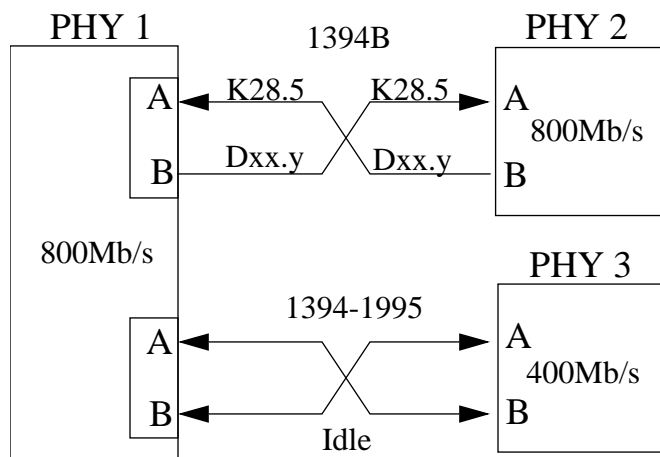
- All PHYs with a peer capable of 1394B communication issue a priority request to send a “Receiver PLL sync packet” at 100 Mb/s.
- Reception of the receiver PLL sync packet indicates to the PHY to begin locking sequence.
- All Phys repeat the packet and concatenate Data\_prefix for 2.6 us to hold the bus while 1394B communication is established on appropriate ports.



### Ports convert to 1394 communication:

- After transmitting the receiver PLL sync packet, the PHY begins transmitting a continuous flow of 8b/10b code on its “B” port.
- The receive PLL on the “A” port begins locking on it’s neighbors transmission.
- The PHY can use a sequence similar to Fibre Channel to synchronize their receive PLLs (NOS, OLS, LR, LRR).
- After 2.6us, the PHY must begin transmitting idle on all its ports. In the event that the receivers were unable to lock, the port returns to 400 Mb/s 1394-1995 communication.

### Established 1394 communication



## Serial Bus:

- Cable attenuation and connector electrical performance.
- Should the 1394B connection remain over a bus reset? This would require tree-id and self-id over the Gbit interface.
- 2 and 4 Gbit/s receive PLLs must be able to handle slower 1394B data rates.

## Link/Phy interface:

- Should the interface remain at 50Mhz to support isolation (pin count grows to 64 at 3200Mb/s)?
- Support older links?
- Can the link request the PHY to send a Receiver PLL synch packet?

# Summary

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- Compatible with 1394-1995.
- Digital speed signalling for speeds over 400Mb/s.
- Continuous stream of 8b/10b code.
- Minimizes changes to existing state machines.

IBM is currently evaluating cable transceiver specifications:

- DC vs AC coupling.
- Signal amplitude boost (~600mV).
- Analog current & voltage specs.