

P1394b

# *P1394b Start-up*

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# Introduction

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- ▢ Scope: start-up procedure for Beta-capable links
- ▢ Arbitration state machine operation (bus reset, tree-ID, self-ID and normal operation) will follow AFTER this start-up procedure
- ▢ Recent developments
  - concept of a sub-PHY, to take care of long haul
  - common coding scheme for all long-haul speeds and S800+ copper
- ▢ Questions on interoperability (see next foils)
  - many different sorts of port can be imagined
  - what can talk to what?

## *Port properties - 1*

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### a P1394b port

- a. may be capable of operating at any speed range from S100 upwards
- b. may be capable of operating at any speed range from S800 upwards
- c. shall be capable of operating in Beta mode
- d. when capable of operating at S100, shall be capable of DS at S100-S400, may be capable of Beta mode at S100-S400
- e. may be brought out to a 1394-1995 connector ONLY when capable of operating in DS mode
- f. NB improved connector electrical properties are required for S800
- g. open issue - connector for S1600 and S3200
- h. may be connected directly to a suitable transceiver for long haul connection (thus also providing DC isolation)
- i. may use DC (e.g. capacitive or galvanic) isolation when operating in Beta mode

 this is also the "short-haul" port on a P1394b sub-PHY

## *Port properties - 2*

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- ▣ The "long-haul" port on a P1394b sub-PHY
  - a. may be capable of operating at any single speed (S100 - S3200)
  - b. may be capable of operating at any speed range from S100 upwards (i.e. S1, or S1+S2, or S1+S2+S4, etc)
  - c. may be capable of operating at any speed range from S800 upwards
  - d. operates in Beta mode only
  - e. is not required to interoperate with a 1394-1995 or P1394a port
  - f. shall not be bought out to an interface using a 1394-1995 connector
  - g. connects through a suitable transceiver (this may be integrated), galvanic isolation and a RJ45 connector for S100 UTP
  - h. connects through a suitable transceiver and, optionally, a suitable optical connector for optical fibre transmission
  - i. "understands" the speed limitations of the connected long-haul transceiver by an implementation dependent mechanism

## *Sub-PHY long-haul port*

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 A subPHY long haul port is essentially a stripped down 1394b port.

It's a 1394b port:

- without DS
- 1394 connector forbidden
- may operate at only one speed (S100 through S3200), or a range of speeds
  - ✓ provided the range includes either S100 or s800 or both (for start up)
- speed(s) dictated by attached transceiver.

## *Port types and properties*

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### 1. S100+ DS

- a port as defined in 1394-1995/1394a  
(S100+ means S100, or S100+S200, or S100+S200+S400)

### 2. S100+ DS/Beta

- as 1) but also capable of Beta mode (not necessarily all Beta speeds)

### 3. S100+ Beta

- Beta mode only at S100+ i.e. a long haul only port for slower speeds
- cannot be brought out to a 1394 connector

### 4. S100+ DS; S800+ Beta

- as 1) but also capable of operation in Beta mode only at higher speeds ( $\geq$  S800)

### 5. S100+ DS/Beta; S800+ Beta

- as 4) but also capable of beta mode at S100+
- this is the bells and whistles port

### 6. S800+ Beta

- only operates at speeds of S800 upwards, and does not support the 1394-1995 signalling interface (i.e. long haul for higher speeds)
- cannot be brought out to a 1394 connector

★ The above does not fully comprehend single-speed Beta ports

## Interoperability table

	S100+ DS	S100+ DS/Beta	S100+ Beta	S100+ DS; S800+ Beta	S100+ DS/Beta; S800+ Beta	S800+ Beta
S100+ DS	yes DS	yes DS	no	yes DS	yes DS	no
S100+ DS/Beta		yes DS (?)	yes Beta	yes DS	yes DS (?)	no
S100+ Beta			yes Beta	no	yes Beta	no
S100+ DS; S800+ Beta				yes Beta	yes Beta	yes Beta
S100+ DS/Beta; S800+ Beta					yes Beta	yes Beta
S800+ Beta						yes Beta

## General goals

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### Start-up in Beta mode if

- both ends are Beta capable at S800+, or
- at least one end is not DS capable, or
- there's no DC connection

### Corollary: start-up in DS mode if

- both ends are DS capable, and
- there's a DC connection, and
- at least one end is not Beta capable at S800+
  - ✓ lower power consumption

 The above is not agreed, as we may wish to start up in Beta mode to take advantage of arbitration interleaving!

## Power-on state

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- ▢ Ports power on assuming they are disconnected and in suspend mode - every port is in Disconnected state
- ▢ Suspend/resume low power connection detect mechanism transits the port state machine to Resume state
  - mechanism relies on a DC connection
    - ✓ need another mechanism for use in AC connections
  - resume state actions rely on TpBias
    - ✓ need another handshake mechanism for AC connections
- ▢ Other port state transitions rely on TpBias and LpCon
  - ✓ above mechanisms need to substitute for these functions
- ▢ Connection\_status monitor relies on low power connection detect mechanism and on TpBias output control flip-flop
  - need to avoid a port looking as if it is connected during Beta mode start-up

# Start-up phases

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- ▢ determination of connection
  - Steve Bard presentation on suspend/resume
- ▢ determination of beta or DS mode
  - ditto
- ▢ determination of what speed to start beta mode (S800 or S100)
  - see later
- ▢ bit synchronisation
  - need AC coupling settling times, PLL lock times
- ▢ codeword sync
  - Alistair's proposal
- ▢ scrambler sync
  - ditto
- ▢ speed negotiation
  - possibly resulting in going back to bit sync at a higher speed
- ▢ root contention reconciliation
  - (if HP proposal is adopted it happens here)

## *Speed determination - 1*

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- ▮ This is largely still open, and requires further study
  - requires review in the light of the coding decisions
  
- ▮ Four symbol sequences are defined - S1, S2, S3, and S4
  - For ease of understanding, consider each sequence as four 10-bit symbols.
  - Each sequence should have the property that the PHY can perform symbol alignment by examination of the bit-patterns within the symbols.
  
- ▮ The ability to transmit and receive at a lowest common denominator speed is established first.

## Speed determination - 2

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- ▢ Proceed through bit-sync, codeword sync and scrambler sync
- ▢ The sequence S1 is transmitted repeatedly at the lowest rate that the PHY is capable of (122.88 MBaud for S100)
- ▢ Simultaneously, the sequence is listened for.
  - The receiver performs symbol alignment until it can receive the sequence successfully.
  - The exchange of S1 continues for long enough to provide a sufficient level of confidence in the link signalling integrity
    - ✓ NB this is NOT a BER test
  - NB the "other" end may be trying at S800 when we're trying at S100, or vice versa
- ▢ The PHY then transmits S2 repeatedly to confirm "good" reception, and awaits reception of the S2 sequence.

## Speed determination - 3

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- ▮ If the PHY is capable of a higher speed, it then transmits S3 repeatedly, otherwise it transmits S4 repeatedly.
  - If it is capable of a higher speed, and it receives the S3 sequence, then it starts to transmit the S1 sequence at the S200 equivalent rate.
  - Upon successful reception for a defined period of time, the PHY confirms reception by changing the transmitted pattern to S2. The process repeats to the next highest speed.
- ▮ The result of this procedure is full-duplex transmission at the maximum rate acceptable to the PHYs. Bit alignment and symbol alignment is achieved.
- ▮ Upon completion of the procedure (transmission or reception of S4), the PHY commences to transmit IDLEs.
- ▮ The PHY also sets the Bias bit (simulating TpBias for the PHY-LINK interface), with the consequent implications for the Con bit.
  - needs review for suspend/resume

## *Await connection*

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- ▮ The Beta capable PHY has received neither TpBias nor a tone.
- ▮ It transmits a tone for a period of  $n$  microseconds (we propose  $n=5$ ).
  - This is repeated at intervals of  $60n$  (say) microsecond until either a tone is heard or TpBias is detected on TPB.
  - If a tone is heard, then the speed determination procedure is entered (see above).
  - If TpBias is detected, then TpBias is generated on TPA and start-up is as per 1394-1995 for DS-Links.
- ▮ This scheme avoids excessive energy being transmitted into an unterminated cable.
  - This would be necessary for a UTP 1394 link, but could also be a sensible move for any 1394b copper link.
- ▮ Also consider use of “sleep” modes, and the need to be able to detect a wake-up signal without requiring the PHY to be powered all the time.
  - This may be achievable either by having a low level active circuit which can respond to the reception of the tone and wake up the rest of the PHY.

## Low Power connect detect

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- use a periodic burst of signals during suspend
  - send for B microseconds, followed by S microsecs of silence ( $S \gg B$ ).
  - receiver's 'Connected' is true if any transitions are detected within B+S usecs.
    - ✓ signal does not have to be recovered - just the presence of transitions detected (ie no PLL, decoding at this point in time).
  
- To resume, the resume initiator starts sending all the time
  - receiver detects resume by sensing no period without transitions in time B+S
  - $B > 100\text{usecs}$  (??) long enough to wake up an optical receiver
  - S could be of the order of a millisecond.
  
- does it conserve enough power?
  - Transmitter needs to generate burst of signals with transitions (does not even need to be valid control/data - but probably should not be a tone due to EMC).
  - Receiver needs to detect transitions. Both tx and rx need to have (share) a crude timer.
  
- how long can S be before there is the possibility of a disconnect/reconnect occurring during the interval S?
  - quite long for human controlled disconnects,
  - but what about if someone builds an electronic switch

## *Loss of synchronisation*

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- ▮ This is a topic for further study
  - needs review following coding decisions
  
- ▮ However, a good starting point is the Fibre Channel state machine
  - provides hysteresis on the detection of an error (e.g. an invalid symbol, or excessive running disparity),
    - ✓ synchronisation is maintained unless a rapid sequence of errors is detected.
  - The PHY transmits an indication of loss of synchronisation
    - ✓ this could be the S1 sequence
  - The PHY enters the speed determination state on loss of synchronisation and on receipt of the loss of synchronisation indication.
  - need to consider the reset behaviour on loss of synchronisation