IEEE p1394b
Standards Closure Action Team (SCAT)
Meeting
June 7 & 9 1999

07 June 1999

CHAIR: *David Wooten*
SECRETARY: *Steve Bard*
EDITOR: *Eric Hannah*

Action Items from this Meeting:

#1: Alistair has some work to accomplish prior to the next SCAT meeting (see SCAT Issues #37 & #42).

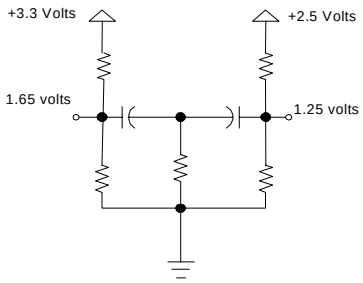
#2: Colin will begin investigating the issue of symbols which may be deleted. The goal is to insure FIFOs do not become empty when the are supposed to be repeating packets. The FIFO may become empty due to clock frequency differences and related quantization effects.

After a fair amount of "meeting logistic fibrillation", the meeting began at 9:30 AM. Those present at today's meeting are so indicated in the attendance roster appended to the end of these meeting minutes.

Terms for the unaware reader:

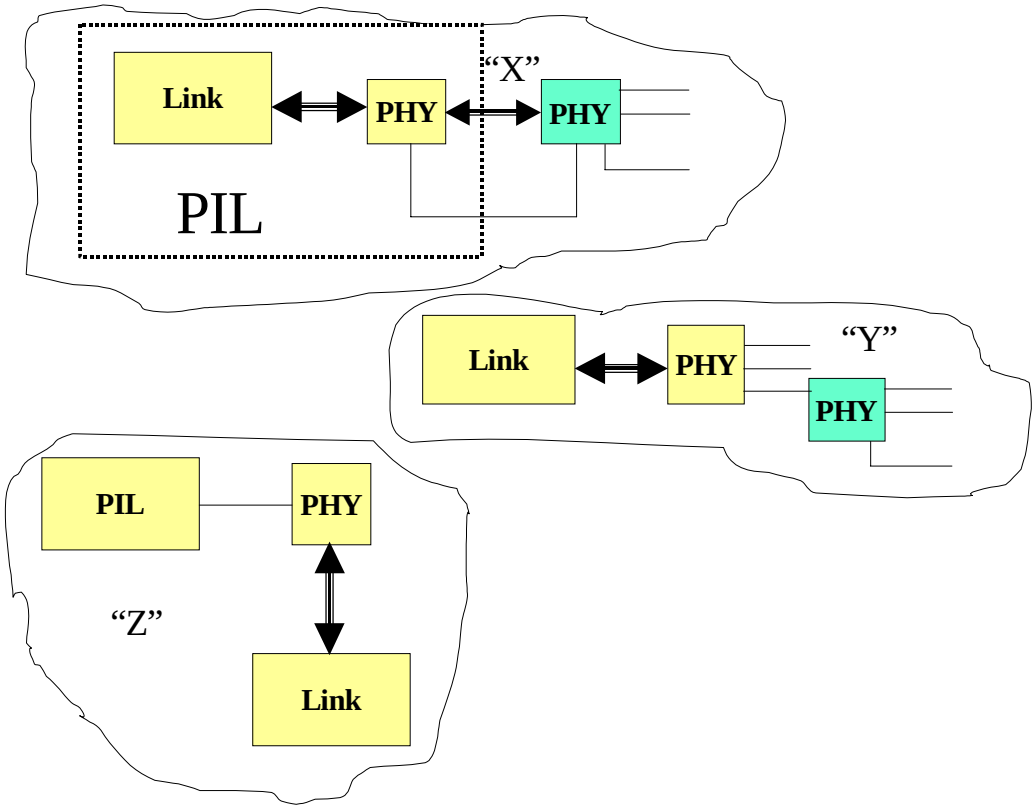
PIL	Integrated PHY/Link silicon device
FOP	Fan Out PHY

Some discussion ensued regarding isolation issues when using PIL/FOP, just a PIL (connected to transceivers and to a panel connector), power planes, etc. The drawing (below) was used in these discussions.



Tony Foster suggested that SCAT impose a requirement in the 1394b draft specification that the signaling at both ends of the PHY/Link parallel interface shall be 3.3 volts. There was consensus among SCAT members present. Tony will deliver the message to the Plenary tomorrow. It was suggested that any plenary member which votes "NO" would require the no vote owner to submit a better solution.

Much discussion took place around what software might and might not be able to do with the PIL-FOP model specific to the three models shown below:



The PIL shall have a set of side-band signals (PINT'ish and LREQ'ish). The 1394b draft standard shall define these side-band signals and the behavior between the PIL and a FOP when these side-band signals are used. These side-band signals are depicted in model "X" (above) as the single connection (no arrows) between the PIL PHY and the PHY outside the PIL.

The "holy grail" of this discussion is to make certain that model "X" and model "Y" are software "(read: OS) transparent. From a power management standpoint, Steve Bard has penned a few thoughts. You may read them, if you like, for they have been conveniently appended to the end of these minutes (right after the attendance table).

Model "Z" is a typical use model which shows an implementation of a PIL providing complete capability of true PHY.

Nothing precludes the PIL from having one or more complete beta-only PHY ports (each which behaves exactly like the PHY ports on a discrete beta-only PHY).

The FOP shall not contain the traditional parallel PHY/Link interface.

A FOP shall include the standardized side-band signals.

A FOP may have a strap option which causes all ports to power-up disabled. In this instance, one port would not power-up disabled. It would be this port which would be connected to the PIL port.

When implemented together, the PIL and FOP behave as a traditional Link and single PHY (e.g. the PHY in the PIL and the FOP behave as if they were a single PHY).

Colin take a moment and presented the following little matrix (less the "blue" entries):

PHY (MAX)

LINK (MAX)	BETA			
	S800	S400	S200	S100
S800 β	100 MHz β/8	100 MHz β/8	100 MHz β/8	100 MHz β/8
S400 β	100 MHz β/8	100 MHz β/8	100 MHz β/8	100 MHz β/8
S200 β	100 MHz β/8	100 MHz β/8	100 MHz β/8	100 MHz β/8
S100 β	100 MHz β/8	100 MHz β/8	100 MHz β/8	100 MHz β/8
S400 α	50 MHz α/8	50 MHz α/8	50 MHz α/4	50 MHz α/2
S200 α	50 MHz α/4	50 MHz α/4	50 MHz α/4	50 MHz α/2
S100 α	50 MHz α/2	50 MHz α/2	50 MHz α/2	50 MHz α/2

After which, he pointed out that the only need for 100 MHz clock is S800 - S800, therefore, Colin suggested we simply drop the parallel PHY/Link interface all together for 1394b!

David Wooten stated that this is not a rational chart and is irrelevant. After some discussion, it was determined and agreed that (when the table is completed with the "blue" data) what we have is precisely what the draft specification has documented (revision 0.60).

In consideration of the desire to move the world to Beta mode devices sooner than later, the [complete] table will stand - 100 MHz β/8 is required for all implementations.

A discussion of when to complete took place. Steve suggested that it would be very good to submit the draft for first ballot in October (1999). This calls for a vote by the Plenary in September to submit the draft to ballot. Steve also suggested that the draft should have all technical content submissions closed by the July meeting.

The following technical subjects are all that are left to complete the draft standard: 1) border node, 2) PHY/Link (FOP/PIL implementation and standardization), 3) Loop healing, 4) Beta/bilingual connector. It would be good to have an informative section which sort of ties things all together (like clause three of 1394a).

Colin stated that the state of border node is such that Jerry has a presentation for simplified border node functionality. If the plenary agrees in principle (at tomorrow's meeting) then all which remains is pounding out the details. The details (implementation) is being worked on already, however.

Sean stated PHY/Link shall be completed either: 1) well before the September meeting, or 2) well, before the September meeting.

Jerry and David stated that loop healing algorithms are completed and have been submitted to Colin for incorporation into the draft standard. As soon as Colin has sorted out some other things (sorted out tree-ID and self-ID) then he will be ready to take the algorithms and incorporate them into the draft standard. Colin sees no show stoppers in being able to do this.

David expects that it may be very difficult for the connector group to complete all which needs completion by the September meeting. Something about a "snow ball" was mentioned.

Dismissed 7 June at 4:20 PM (after which Jerry and David delved into a lengthy discussion of BOSS, border nodes, arbitration, Jerry's issues with 1394a, deleteable symbols, and other somewhat interesting subjects).

Wednesday, 09 June 1999

Updated SCAT issues table was distributed and discussed. Actions taken have been documented within the SCAT issues table. The Issues table will be submitted for upload to the ftp repository and will be made available to general IEEE 1394b working group membership for further comment.

In view of the decision in yesterday's plenary session (e.g. submit for first ballot review in October) the chair took an action item to post an e-mail to the "B" reflector in which he will strongly encourage folks to review the SCAT and compare it against the draft specification and make comment as one feels necessary.

Jerry inquired as to whether "B "links required to have adjustable cycle timers? There is no compelling reason to force a "B" node become root. A bridge could force a node which has an adjustable timer to become root (which means the bridge could force itself to be root). The point being made, however, is there is a desire to make certain that there is no requirement that a bridge SHALL ALWAYS be root.

It may need to be that the subject of an adjustable cycle timer be brought forth for discussion in another forum (such as OHCI 1.1).

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Power management thoughts from Steve Bard:

Terms for the unaware reader:
1394PE a beta-mode only implementation of IEEE p1394b

In this scenario, an integrated PHY/Link (with a single exposed 1394PE port) connects to a Fan-Out PHY (FOP). What about Power Management?

Possible Power Modes of the PIL:

PIL4: Hard OFF – zero power being consumed;
PIL3: Soft OFF – still some amount of power being consumed;
PIL2: Suspend – as defined in 1394a and 1394b;
PIL1:Standby – as defined in 1394b
PIL0: ON

Possible behaviors for each of the PIL Power Modes;

PIL0: Full and normal communications between the PIL Port and it connection
PIL1: As specified in 1394b, the FOP serves as PIL proxy; PIL participates in standby/restore protocols
PIL2: As specified in 1394a and 1394b Suspend
PIL3: Link portion of PIL not in the lowest power state it can while PHY portion of PIL is in suspend (standby?)
PIL4: Link and PHY portions of PIL are consuming zero power.

The FOP may consist of the following configurations:

a) a pure FOP – knows and is dedicated as a new piece of silicon serving only as a FOP; may be either beta only or bilingual; contains no PHY/Link interface; has three or more ports - one port always connects to PIL while two or more ports are exposed as external or internal interconnect; may be Beta only or bilingual.
b) a Tri-FOP – knows about how to behave as a FOP; may be either beta only or bilingual; has three or more ports - one port always connects to the PIL while two or more ports are exposed as external or internal interconnect; provides a PHY link interface, however, in implementation, a separate link chip shall not be attached when one port is attached to the PIL.

What is the relationship between the PIL and FOP for the various PIL power modes? The FOP itself has its own various power modes. What is the functional model when overlaying FOP power modes on top of the ILP and its various power modes?