Scrambler is Bypassed

Encoder is Bypassed

New function added: Data Type ID

Serializer is Bypassed

Interface to Ethernet PHY is 10 bits parallel data

1394b PHY beta mode functions
Modifications for 1000BASE-T PHY

Data Type Identification (2 bits added)
Data Type Identification
2 bits appended to identify class of data field

1394b data byte (8 bits)

Data Type Identification Bits:
00 = 1394b data byte

10 bit word: S800BASE-T Data Unit (SDU)
**Data Type Identification**

2 bits appended to identify class of data field

1394b request symbol (8 bits)

Data Type Identification Bits:
01 = 1394b request symbol

10 bit word: S800BASE-T Data Unit (SDU)
Data Type Identification
2 bits appended to identify class of data field

- Null Data (0’s)
- 1394b control symbol (8 bits)

Data Type Identification Bits:
10 = 1394b control symbol

10 bit word: S800BASE-T Data Unit (SDU)
Mux SDUs into single stream

1394b data byte (8 bits)
Data Type Identification Bits:
00 = 1394b data byte

1394b request symbol (8 bits)
Data Type Identification Bits:
01 = 1394b request symbol

Null Data (0’s)

1394b control symbol (8 bits)
Data Type Identification Bits:
10 = 1394b control symbol
S800BASE-T Block Diagram

Reconciliation Sub-layer

Transmit Path:
Mux Data, Request, Control
8 bit word input at ~786Mbps

Add 2 bits to make 10 bit word input (SDU)
~983Mbps

8 bit word output, at 1000Mbps, matches GMII format

 Receive Path:
8 bit word input, at 1000Mbps, GMII format
10 bit word output ~983Mbps (SDU)

Use first 2 bits to de-mux into
Data, Request, Control, 8 bits words

FIFOs accommodate rate
Mismatches in both directions

TX_EN and RX_DV control filling,
Emptying of FIFOs
Reconciliation Sublayer: Transmitter

Encoded S800 data stream:
10 bit word SDU (S800BASE-T Data Unit)

Shift 10 bit word at 98.3MHz into FIFO

120 bit deep FIFO

Pointer

Transmit Enable

When pointer indicates FIFO reach FULL state, TX_EN goes HIGH

When pointer indicates FIFO reached EMPTY state, TX_EN goes LOW

TX_EN

8 bit bytes go directly to 1000BASE-T GMII
Reconciliation Sublayer: Transmitter

Transmit Sequence:

1. 1394b PHY begins transmitting to FIFO at 983Mbps
2. FIFO takes 80-88ns to reach FULL state
3. TX_EN goes HIGH, 1000BASE-T PHY begins transmitting data
4. FIFO empties while 1000BASE-T PHY transmits at 1000Mbps (faster than the incoming data)
5. When FIFO reaches EMPTY state, TX_EN goes LOW
6. 1000BASE-T PHY sends IDLE while FIFO is re-filling
7. After 80-88ns, FIFO is FULL, TX_EN goes HIGH, data transmission resumes

1394b PHY sends data + control symbols continuously at 983Mbps

1000BASE-T PHY alternates between bursts of data and IDLE symbols
Reconciliation Sublayer: Receiver

8 bit bytes come directly to 1000BASE-T GMII

120 bit deep FIFO

Receive Data Valid
- When RX_DV is LOW (IDLE) no data is loaded into FIFO
- When RX_DV is HIGH, valid data is loaded into FIFO

Encoded S800 data stream:
10 bit word SDU (S800BASE-T Data Unit)

Shift 10 bit word at 98.3MHz out of FIFO
Reconciliation Sublayer: Receiver

Receive Sequence:

1. 1000BASE-T receives IDLE, no data is loaded into FIFO
2. When 1000BASE-T receives data, RX_DV goes high
3. FIFO fills with data from 1000BASE-T at 1000Mbps
4. FIFO empties data to 1394b PHY at 983Mbps
5. Periodic IDLE patterns allow FIFO to empty, in order to prevent overflowing

1000BASE-T PHY alternates between bursts of data and no data (no input to FIFO)

1394b PHY receives data + control symbols continuously at 983Mbps
Link Equivalence

1394b Link → 1394b PHY → R.S. Sub-layer → 802.3 PHY → 802.3 PHY → R.S. Sub-layer → 1394b PHY → 1394b Link

100m Cat 5 Cable

1394b Link → 1394b PHY → FIFO With 1us delay → 1394b PHY → 1394b Link

S800 983Mbps 983Mbps S800

802.3 PHY
No recovered clock sent to 1394b receive PHY 2
Data rate does NOT match exactly
1394b receive PHY 2 handles rate difference delta, after each 1394 packet