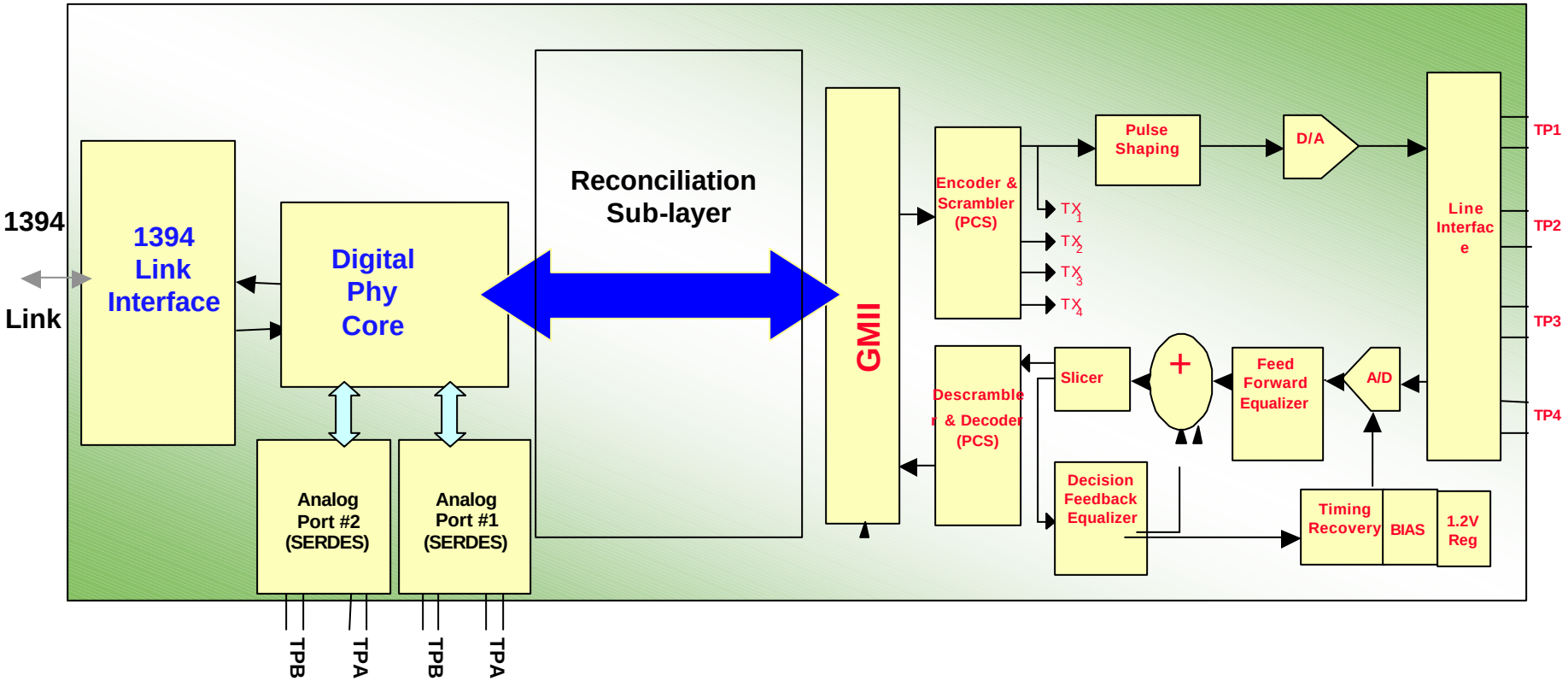
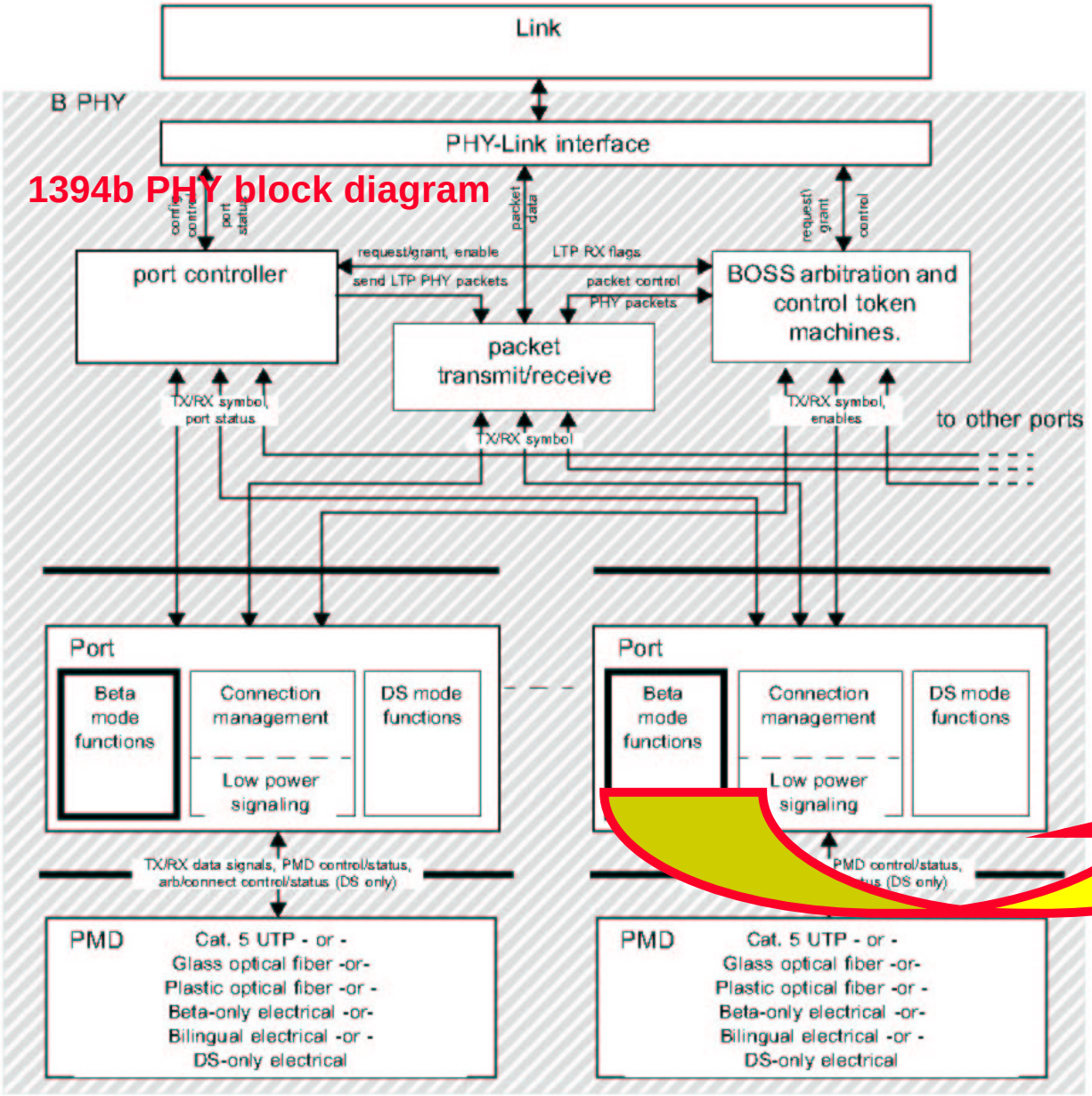
S800BASE-T Block Diagram

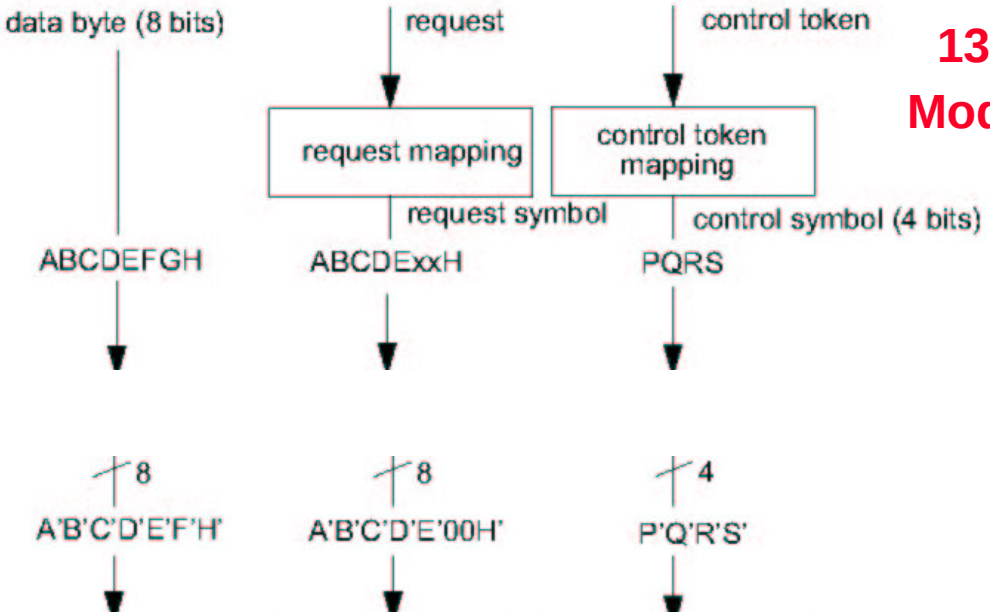


1394b PHY block diagram



Interface to 100BASE-T PHY

Figure 10-1—PHY master architecture (Data routing, arbitration and control interfaces in context)



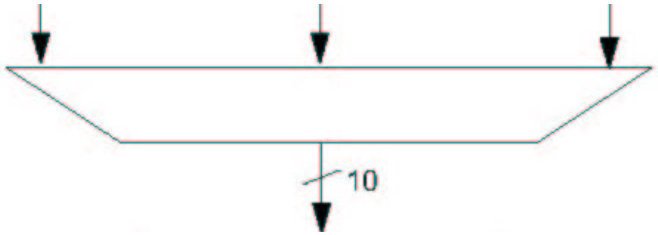
1394b PHY beta mode functions
Modifications for 1000BASE-T PHY

Scrambler is Bypassed

Encoder is Bypassed

Data Type Identification (2 bits added)

New function added:
Data Type ID

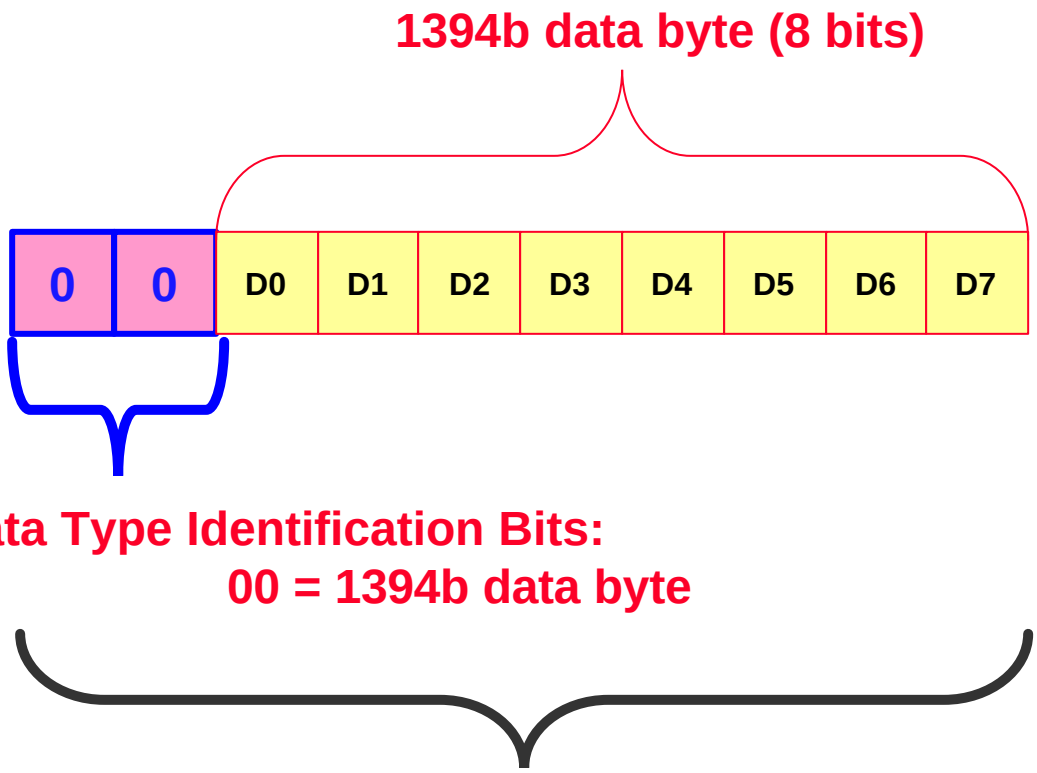


Serializer is Bypassed

Interface to Ethernet PHY is
10 bits parallel data

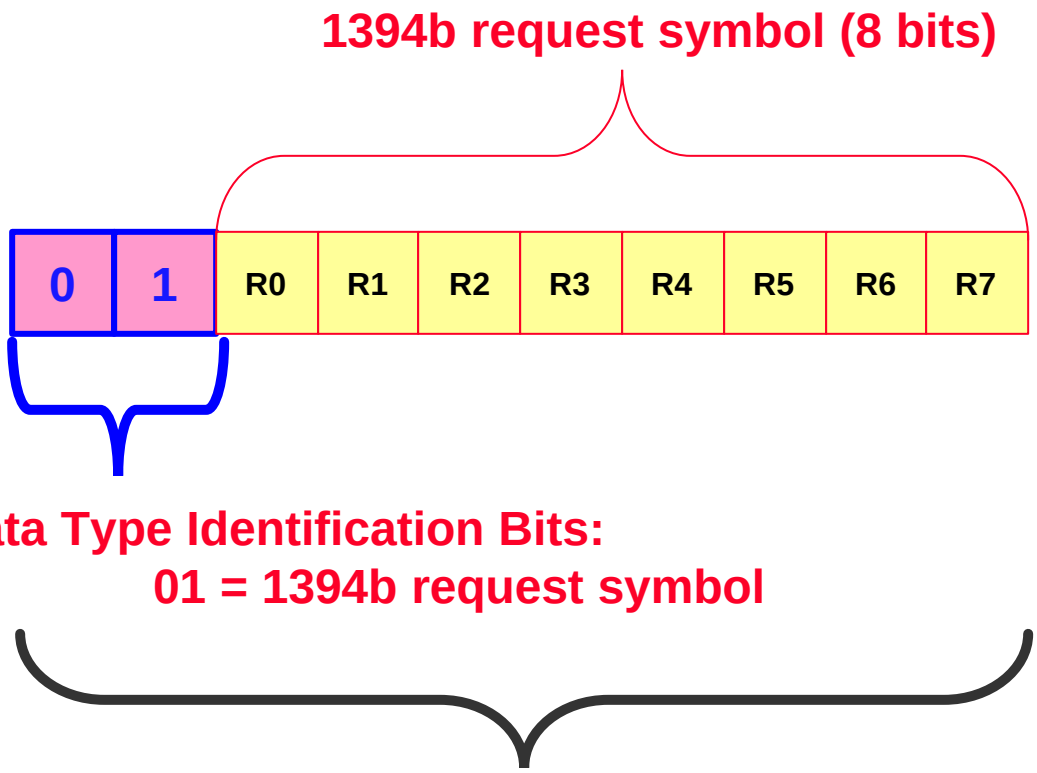
Data Type Identification

2 bits appended to identify class of data field



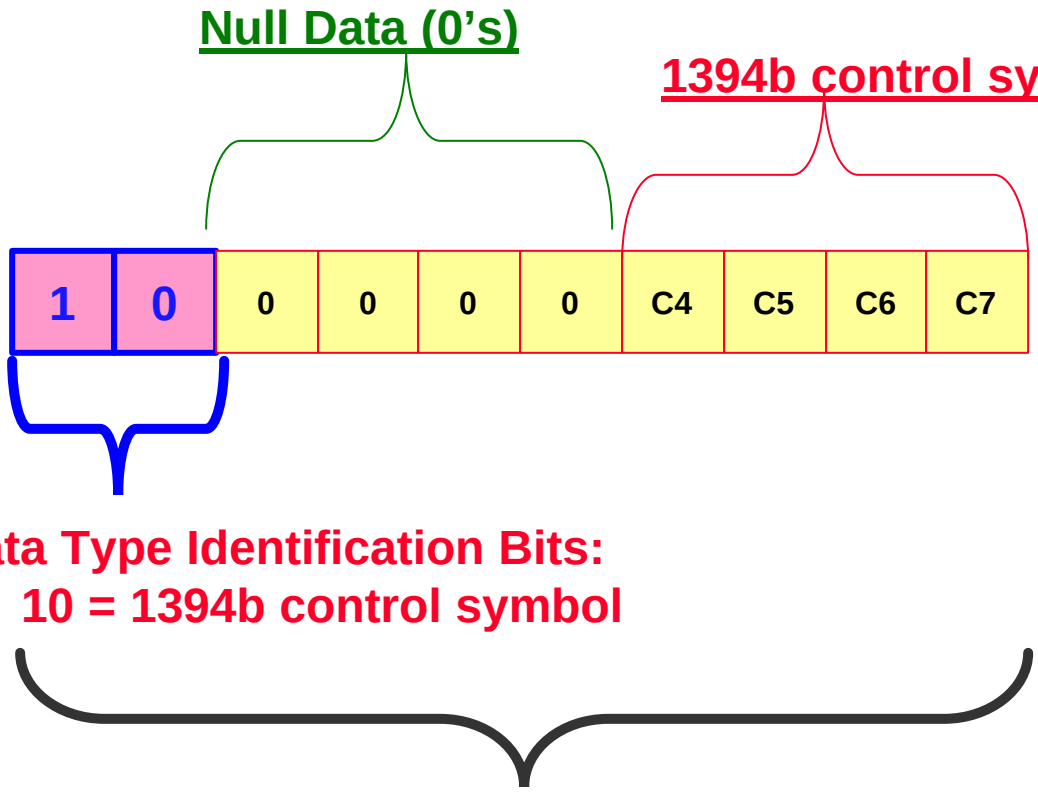
Data Type Identification

2 bits appended to identify class of data field



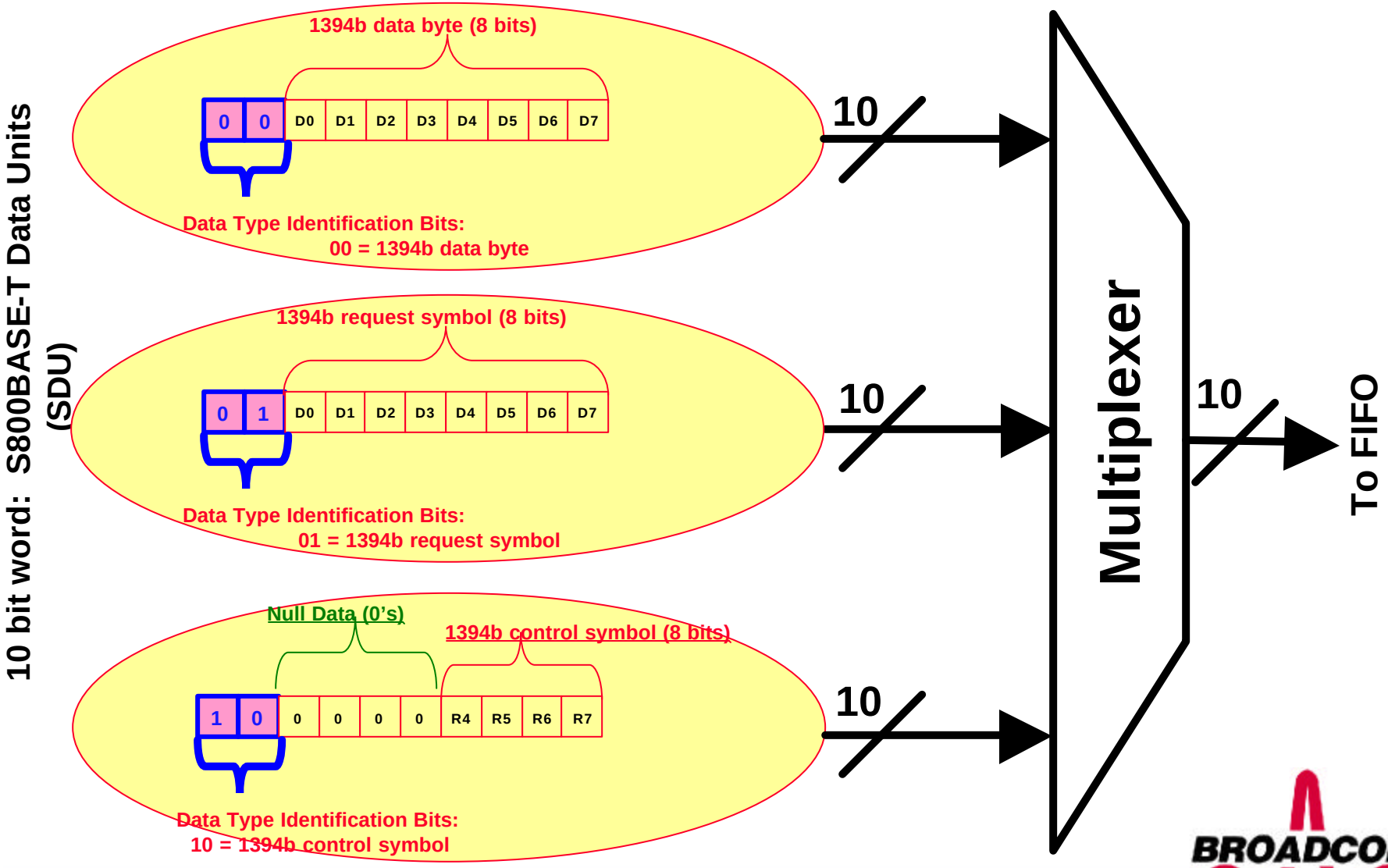
Data Type Identification

2 bits appended to identify class of data field

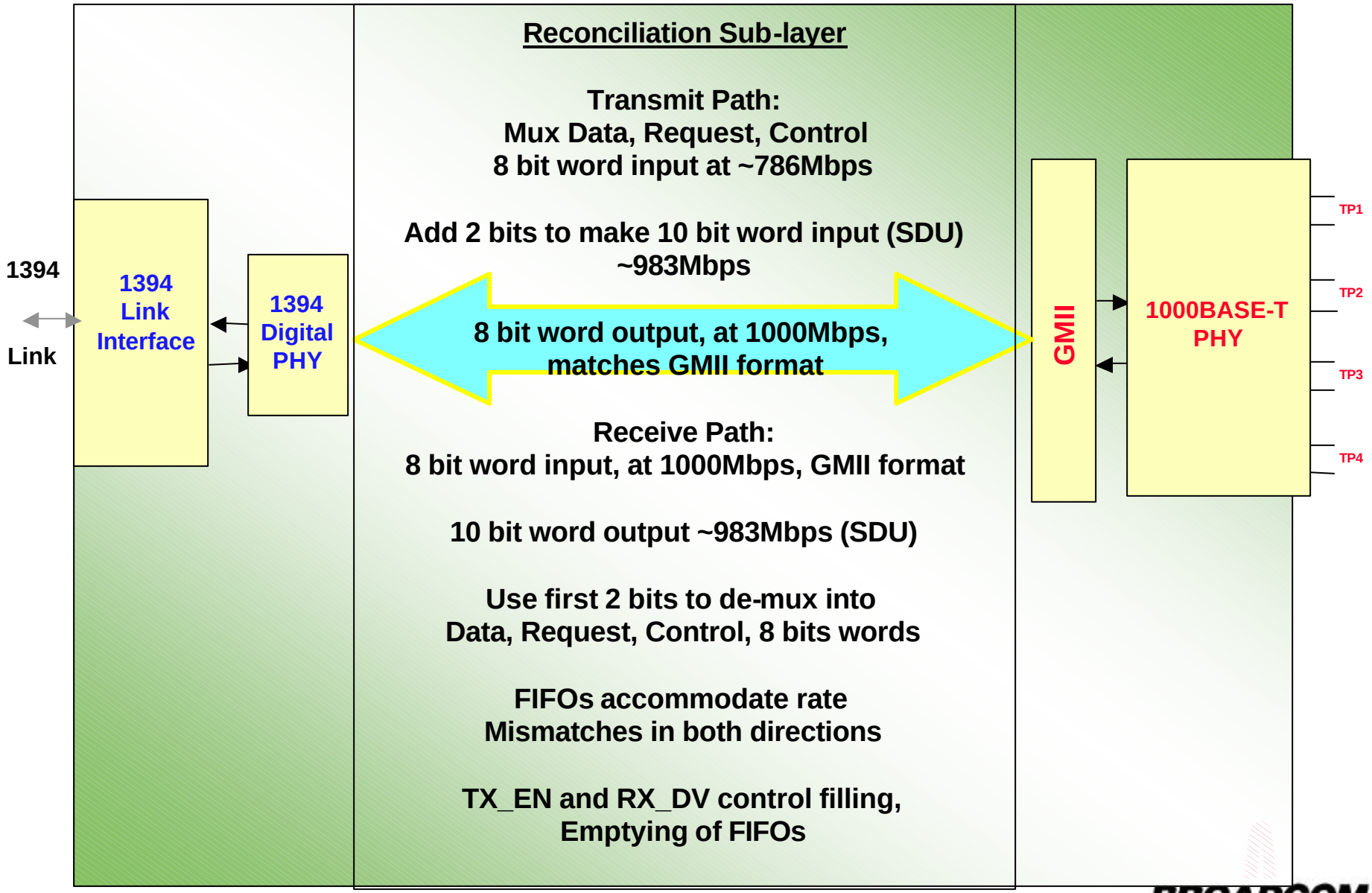


10 bit word: S800BASE-T Data Unit (SDU)

Mux SDUs into single stream



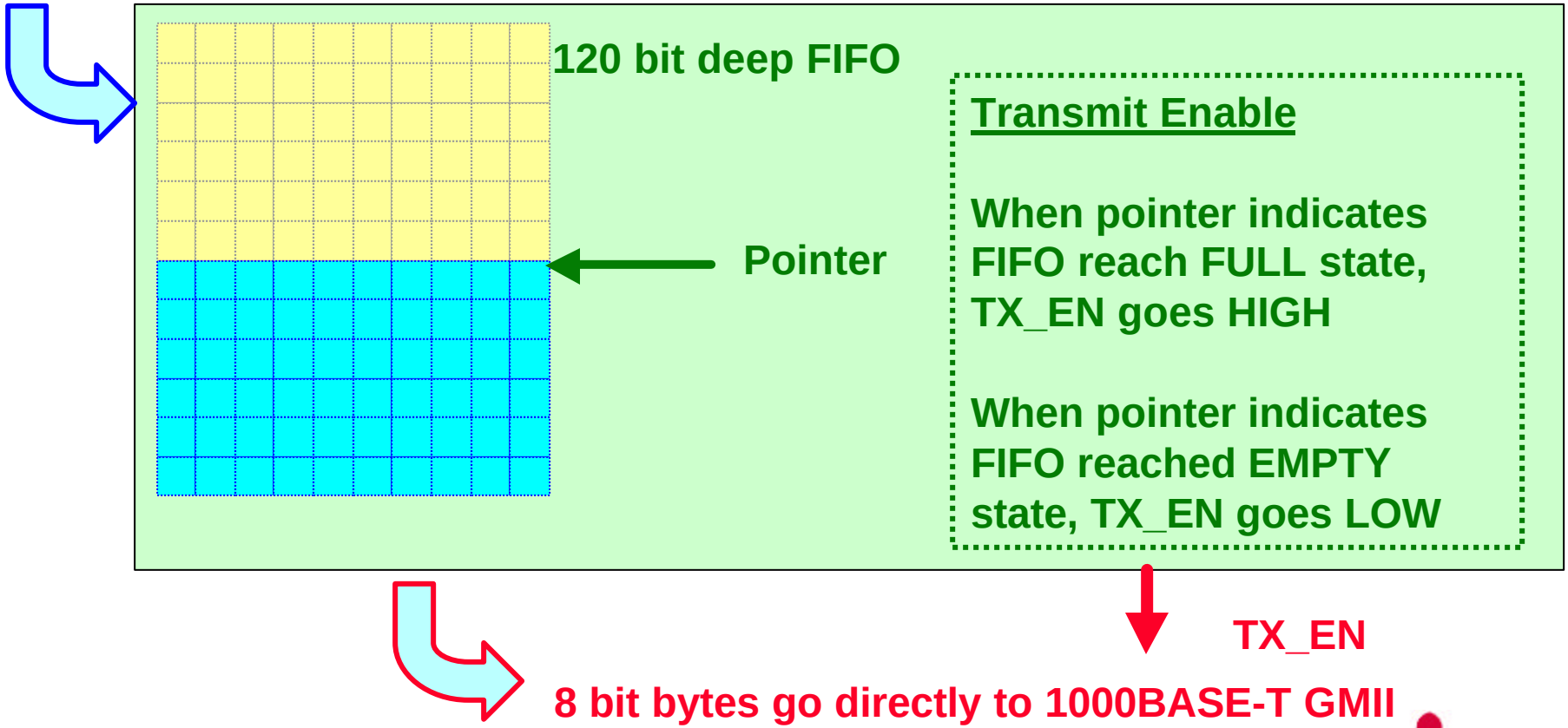
S800BASE-T Block Diagram



Reconciliation Sublayer: Transmitter

Encoded S800 data stream:
10 bit word SDU (S800BASE-T Data Unit)

Shift 10 bit word at 98.3MHz into FIFO



Reconciliation Sublayer: Transmitter

Transmit Sequence:

1. 1394b PHY begins transmitting to FIFO at 983Mbps
2. FIFO takes 80-88ns to reach FULL state
3. TX_EN goes HIGH, 1000BASE-T PHY begins transmitting data
4. FIFO empties while 1000BASE-T PHY transmits at 1000Mbps (faster than the incoming data)
5. When FIFO reaches EMPTY state, TX_EN goes LOW
6. 1000BASE-T PHY sends IDLE while FIFO is re-filling
7. After 80-88ns, FIFO is FULL, TX_EN goes HIGH, data transmission resumes

1394b PHY sends data + control symbols continuously at 983Mbps

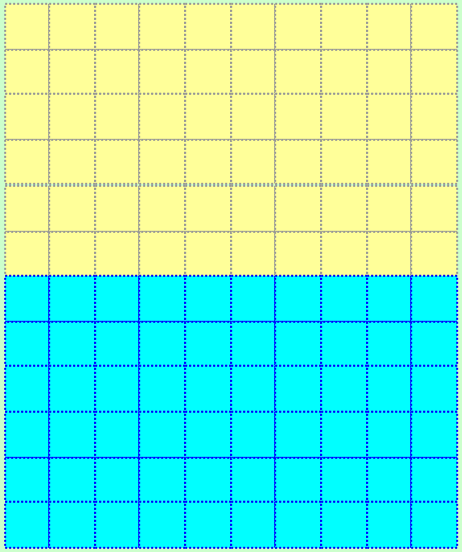
1000BASE-T PHY alternates between bursts of data and IDLE symbols

Reconciliation Sublayer: Receiver

8 bit bytes come directly to 1000BASE-T GMII

RX_DV

120 bit deep FIFO



Receive Data Valid

When RX_DV is LOW (IDLE) no data is loaded into FIFO

When RX_DV is HIGH, valid data is loaded into FIFO

Encoded S800 data stream:
10 bit word SDU (S800BASE-T Data Unit)

Shift 10 bit word at 98.3MHz out of FIFO

Reconciliation Sublayer: Receiver

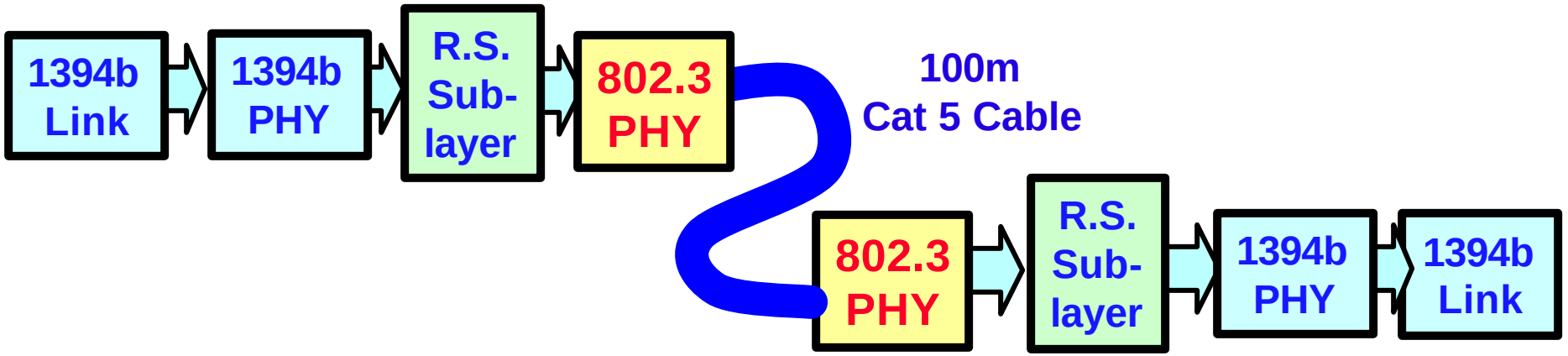
Receive Sequence:

1. 1000BASE-T receives IDLE, no data is loaded into FIFO
2. When 1000BASE-T receives data, RX_DV goes high
3. FIFO fills with data from 1000BASE-T at 1000Mbps
4. FIFO empties data to 1394b PHY at 983Mbps
5. Periodic IDLE patterns allow FIFO to empty, in order to prevent overflowing

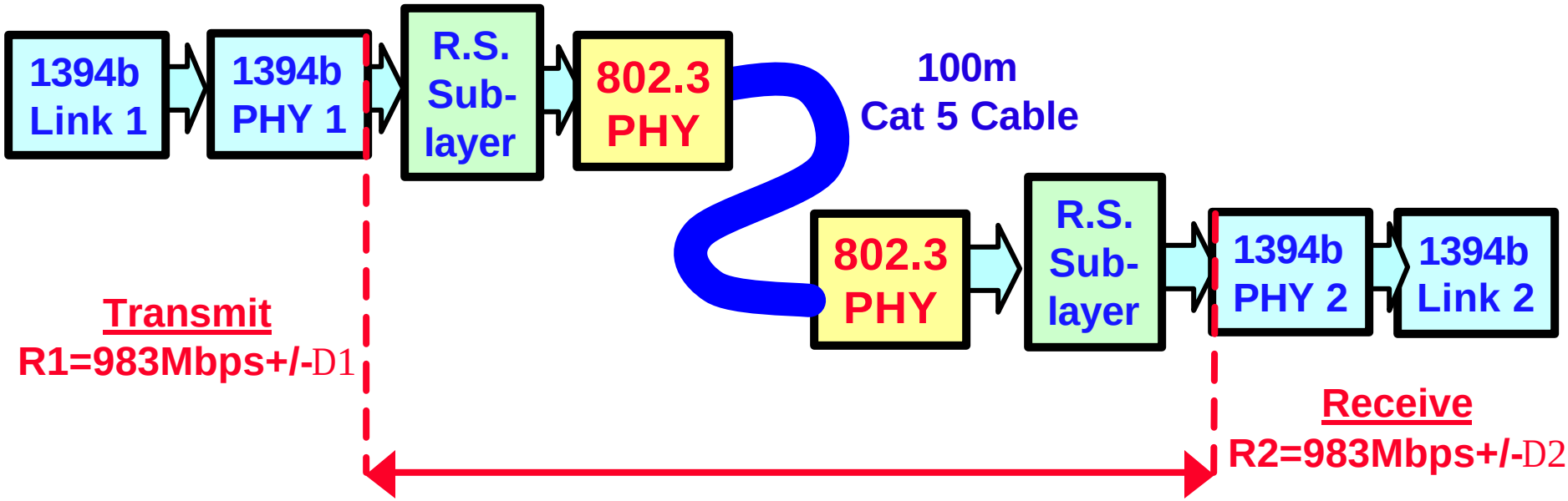
1000BASE-T PHY alternates between bursts of data and no data (no input to FIFO)

1394b PHY receives data + control symbols continuously at 983Mbps

Link Equivalence



Link Equivalence



No recovered clock sent to 1394b receive PHY 2
Data rate does NOT match exactly
1394b receive PHY 2 handles rate difference delta, after each 1394 packet