High-speed PHY interface proposal

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Overview

- Define “xGMII” interfaces for S1600 and S3200 Reconciliation Sub-Layers

- Diagram showing the connections between 1394b Link, 1394b PHY (modified), S800 Reconciliation Sub-layer, GMII, PHY, S1600 Reconciliation Sub-layer, 2xGMII, PHY, S3200 Reconciliation Sub-layer, 4xGMII, PHY.

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Alternatives

- Increase GMII bus width
- Increase GMII clock speed
- Define a new interface
  - SerDes
  - TBI
- Use XGMII (IEEE 802.3ae-2002, Clause 46)
  - Higher speed (10 Gb/s)
  - Full-duplex only
  - Can be extended via XAUI
Figure 46–1 — XGMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

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XGMII

- 32 bits wide, organized into 8-bit “lanes”, each with its own control signal.
- TxCLK rate is 156.25 MHz, sampled on both edges.
- RxCLK can be derived from data stream or synced to TxCLK
- Uses HSTL electrical specs (EIA/JESD8-6), 1.5v output supply
XGMII timing diagram

Figure 46–5—Normal frame transmission
Characteristics of XGMII

**ADVANTAGES**
- Stable, well-defined specification exists
- Numerous implementations in silicon
- Probably compatible with future 802.3 PHY specs
- XAUI interface provides for off-board extensions

**DRAWBACKS**
- 32-bits wide (real estate, power, cost)
- Runs faster than necessary
Slowing down the XGMII

- Need to throttle down from 10 Gb/s to a rate appropriate for S1600 and S3200
- Alternatives include:
  - Use of Pause frames (IEEE 802.3-2002, Annex 31B)
  - Slowing the XGMII clock
  - Using fewer lanes
    - Lane 0 for S1600 (2.5 Gb/s)
    - Lanes 0-1 for S3200 (5 Gb/s)

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- **TxD <31:0>**
- **TxC <3:0>**
- **TxCLK**
- **RxCLK**
- **RxD <31:0>**
- **RxC <3:0>**

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**Reconciliation Sub-layer**

**XGMII**

**PHY**

**Sxx00BASE-T**
### Recommended PHY Interfaces

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<th>1394 Speed</th>
<th>Ethernet PHY speed</th>
<th>Link-PHY Interface</th>
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<td>S800</td>
<td>1 Gb/s</td>
<td>GMII</td>
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<tr>
<td>S1600</td>
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<td>XGMII, Lane 0</td>
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<td>S6400</td>
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