High-speed PHY interface proposal

S800BASE-T Study Group

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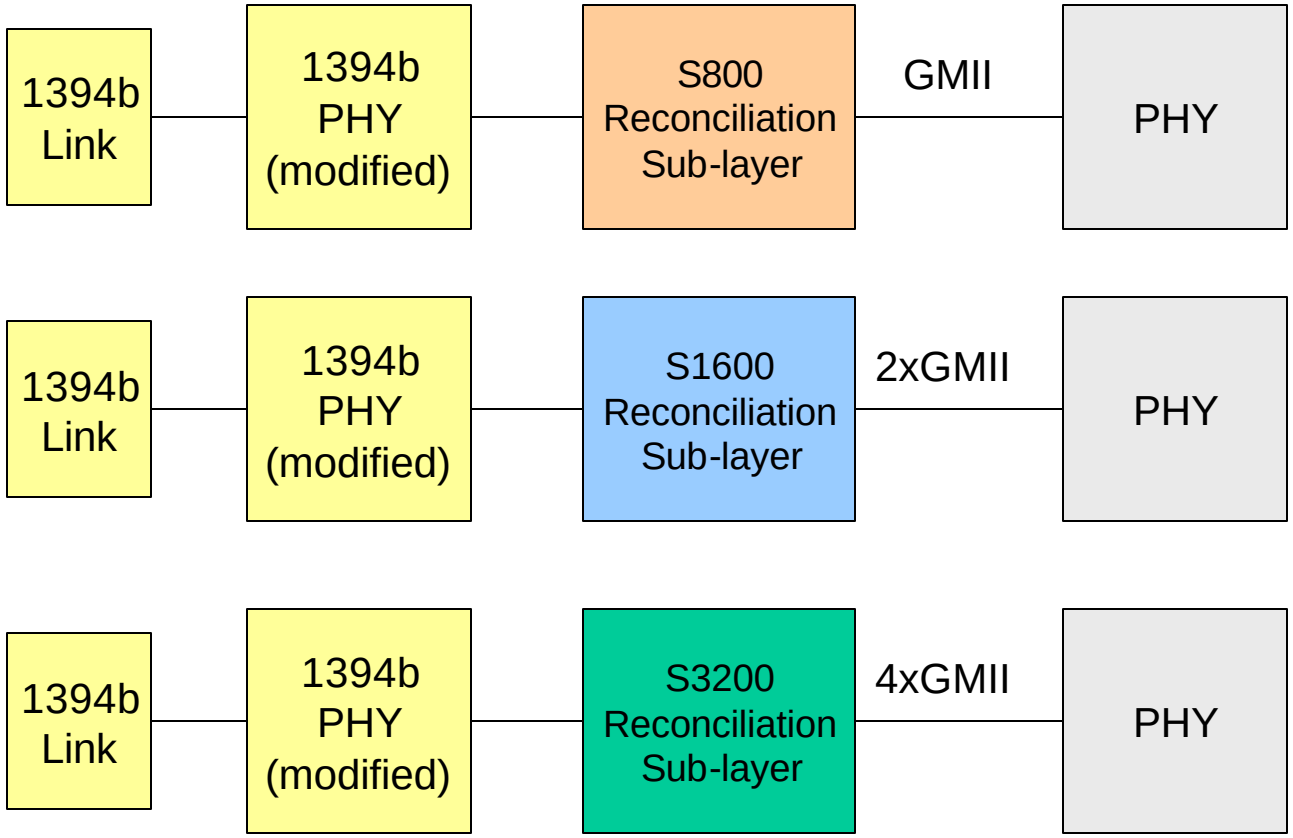
Overview

- Define “xGMII” interfaces for S1600 and S3200 Reconciliation Sub-Layers



Alternatives

- Increase GMII bus width
- Increase GMII clock speed
- Define a new interface
  - ⇨ SerDes
  - ⇨ TBI
- Use XGMII (IEEE 802.3ae-2002, Clause 46)
  - ⇨ Higher speed (10 Gb/s)
  - ⇨ Full-duplex only
  - ⇨ Can be extended via XAUI

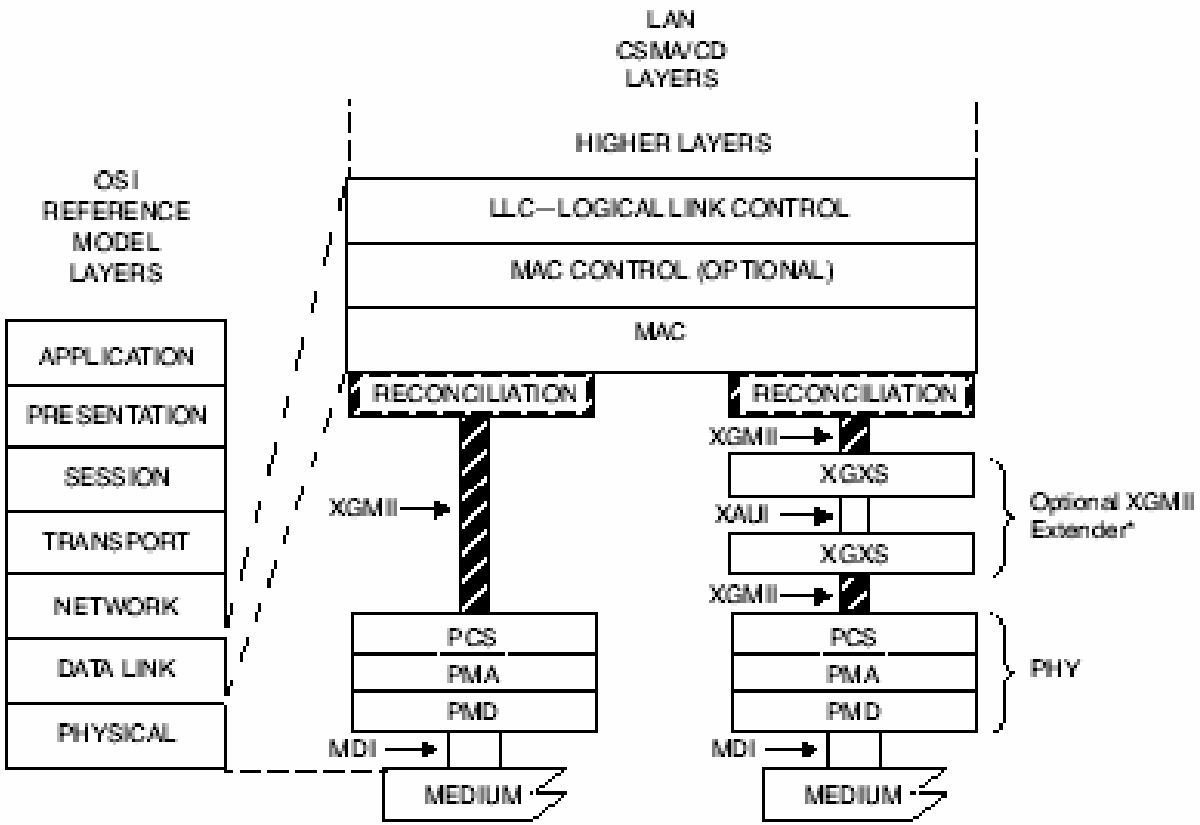
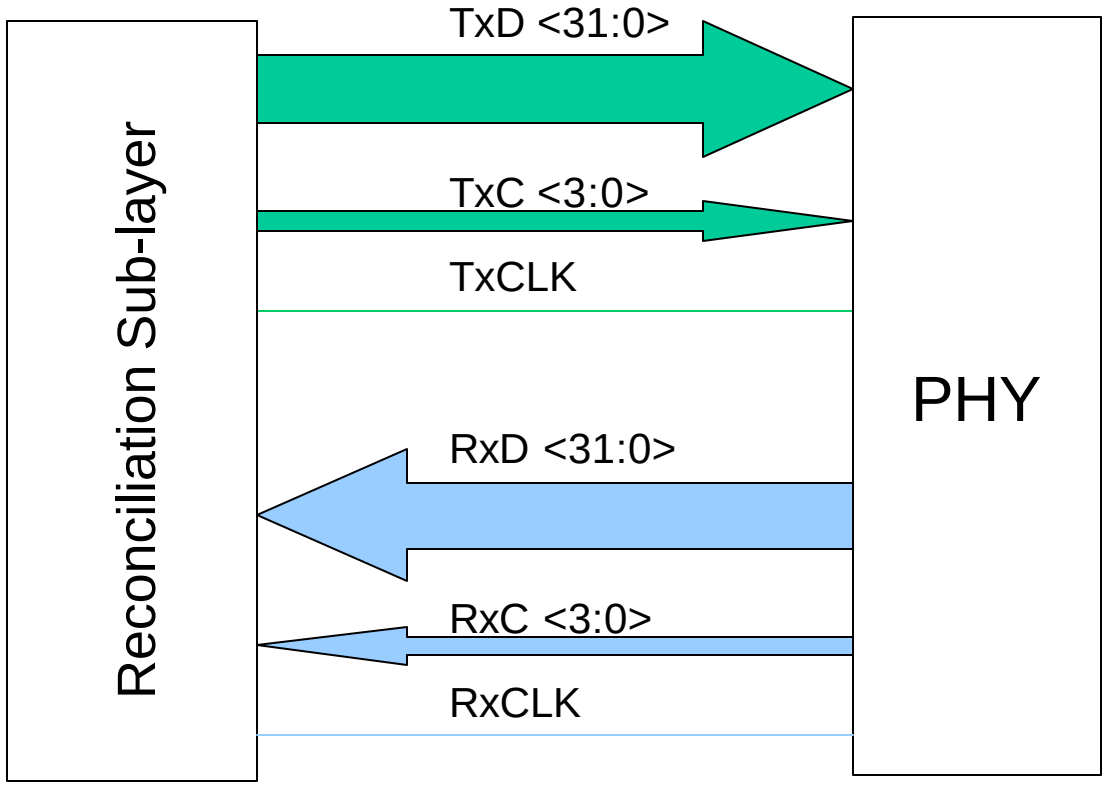


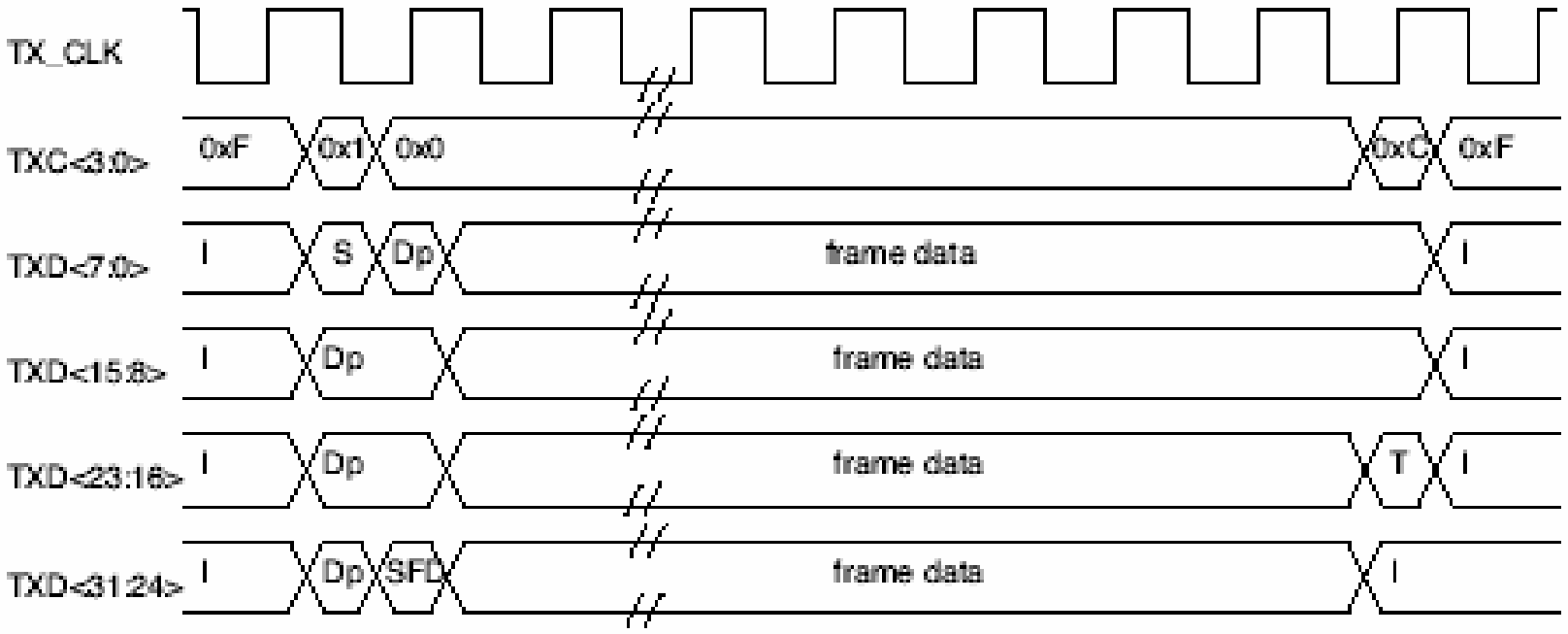
Figure 46–1—XGMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

XGMII

- 32 bits wide, organized into 8-bit “lanes”, each with its own control signal.
- TxCLK rate is 156.25 MHz, sampled on both edges.
- RxCLK can be derived from data stream or synced to TxCLK
- Uses HSTL electrical specs (EIA/JESD8-6), 1.5v output supply



XGMII timing diagram



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

Figure 46–5—Normal frame transmission

Characteristics of XGMII

ADVANTAGES

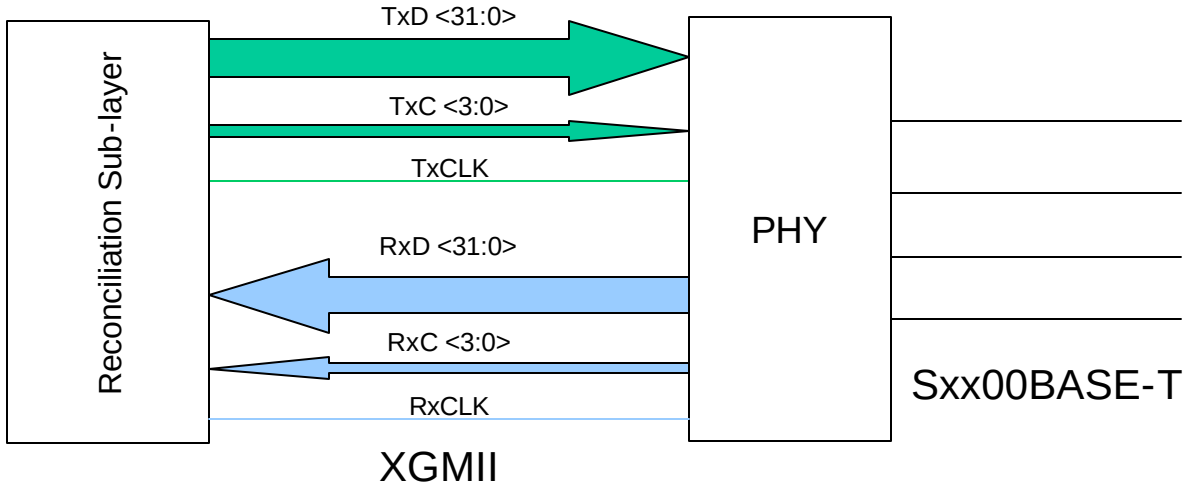
- Stable, well-defined specification exists
- Numerous implementations in silicon
- Probably compatible with future 802.3 PHY specs
- XAUI interface provides for off-board extensions

DRAWBACKS

- 32-bits wide (real estate, power, cost)
- Runs faster than necessary

Slowing down the XGMII

- Need to throttle down from 10 Gb/s to a rate appropriate for S1600 and S3200
- Alternatives include:
  - ⇨ Use of Pause frames (IEEE 802.3-2002, Annex 31B)
  - ⇨ Slowing the XGMII clock
  - ⇨ Using fewer lanes
    - ➢ Lane 0 for S1600 (2.5 Gb/s)
    - ➢ Lanes 0-1 for S3200 (5 Gb/s)



Recommended PHY Interfaces

1394 Speed	Ethernet PHY speed	Link-PHY Interface
S800	1 Gb/s	GMII
S1600	2.5 Gb/s	XGMII, Lane 0
S3200	5 Gb/s	XGMII, Lanes 0-1
S6400	10 Gb/s	XGMII