

# **STIL AMS Web Meeting**

**11 July 2005**

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**Meeting is recorded for Asia Working Group**

# Outline

- Meeting held at VTS 2005
- Question about PAR
- WG members
- How to work all together (Asia/USA/EU)
- Activities during the last months
- Work methodology

# VTS Meeting Target

- Brainstorming on AMS extension for STIL
  - What we should do ?
  - Who should participate ?
  - How should we work ?
  - ...

## What we should do ?

- AMS STIL
  - Extension of IEEE STD 1450.0-1999 ?
  - Extension to STDs and extensions ?
    - IEEE STD 1450.2-2002
    - All other extensions
      - Especially CTL (dot6)
- PAR
  - Purpose
  - Scope

# What we should do : Purpose Draft

VTS Slides

- This effort will define structures in STIL to specify the Analog and Mixed-Signal (AMS) stimuli and acquisition with synchronization that are required for the test of complex systems including AMS design parts like for example System On Chip (SOC). This will complement the IEEE Std 1450-1999 definition of structures for specification on timing and format information on Digital tester as well as the published extension (dot2) for DC Level Specification.

## What we should do : Scope Draft

- Define structures in STIL to specify the Analog and Mixed-Signal stimuli and their synchronization (with both AMS and Digital stimuli) to be applied on the Device Under Test (DUT) by the tester.
  - Stimuli are either in analog or digital format with DC conditions.
  - Stimuli quality description will be defined in the structures
- Define structures in STIL to specify the acquisition of the DUT Analog and Mixed-Signal responses and their synchronization (with both AMS and Digital stimuli) by the tester.
  - Response are either in analog or digital format with DC conditions.
  - Required acquisition quality description will be defined in the structures.
- Define signal treatment of the DUT responses to be done by the tester itself.
- Analog stimuli and responses are in the range from DC to a few GHz and Power could reach a few watts.

# Who should participate

- ATE Vendors
  - Credence
  - Roos Instruments
  - Advantest
  - *Agilent*      **Came from 1st meeting**
  - *LTX*
- EDA Providers
  - Synopsys ?
  - Mentor ?
  - EDActive Computing
- Users
  - Infineon
  - Frecale
  - Philips
  - Toshiba
  - Panasonic
- ?
  - LOA Technology
  - GE Consumer & Industrial
  - Segin
  - Syswave

# Who should participate

- USA

- Dave Barton, EDaptive Computing
- David Oka, LOA Technology
- Jose Santiago, Philips
- Lionel Gilet, Credence
- Vimal Puthiyadath, GE Consumer & Industrial
- Gary Bowers, Segin
- David Whetstone, Segin
- Oscar Rodriguez, Roos Instruments
- Paul Roddy, Freescale
- Daniel Fan, Credence

- USA Cntd

- Frank Anderson
- Rohit Kapur, Synopsys
- Tom Micek

- ASIA

- Yasuo Furukawa  
Advantest
- Bob. K Maeda Advantest
- Sato-  
masayuki@toko.gti.co.jp
- shuichi4.ito@toshiba.co.jp
- hirase.junichi@jp.panasonic.com
- maekawa.michio@jp.panasonic.com
- arai@syswave.jp
- yhayashi@syswave.jp

## Who should participate

- EU
  - Herbert Eichinger, Infineon
  - Heibler Bernhard, Credence
  - Philippe Planelle, ST
  - Martine Dufils, ST
  - Maurice Lousberg, Philips
  - Davide Appello, ST

# How should we work

- 3 Sub-working groups
  - ASIA, USA, EU
    - Proposal to fix time difference and distance issues for phone and /or regular meeting
    - Split work in independant subjects
      - Each WG works towards a specific proposal
      - Proposal to be approved by all 3 WGs
    - Do the same task in each area
      - Duplicate work
      - probably re-work all together

# How should we work

- Regular discussions and status through e-mails
  - Variable sub-working groups for specific subjects
    - Specific conf-calls / net meeting on request
      - Only a few people to synchronize
  - Regular meeting during test conferences
  - Regular (monthly) phone conf-call scheduled in turn for:
    - ASIA-USA time management
    - USA-EU time management
    - ASIA-EU time management

# VTS Meeting Conclusions

- What we should do ?
  - AMS extension should cover all existing extensions (CTL included)
  - Write in the PAR only that we will do and we will finish
- Who should participate ?
  - Some companies were missing
- How should we work
  - No final conclusion (target of this meeting)

# What we should do ?

- AMS STIL
  - Extension to .0, .1, .2, .3
    - Par to be adapted
  - Extension to .4 and .6
    - Need to identify working group in these Area
      - .4 WG could be found in AP WG
      - .6 WG to be defined
    - Then finalize the PAR accordingly
  - PAR modified as Following

# What we should do : Purpose Draft

- This effort will define structures in STIL to specify the Analog and Mixed-Signal (AMS) stimuli and acquisition with synchronization that are required for the test of complex systems including AMS design parts like for example System On Chip (SOC). This will complement the IEEE Std 1450-1999 definition of structures for specification on timing and format information on Digital tester as well as the published extensions of the standard.

# What we should do : Scope Draft

- Define structures in STIL to specify the Analog and Mixed-Signal stimuli and their synchronization (with both AMS and Digital stimuli) to be applied on the Device Under Test (DUT) by the tester.
  - Stimuli are either in analog or digital format with DC conditions.
  - Stimuli quality description will be defined in the structures
- Define structures in STIL to specify the acquisition of the DUT Analog and Mixed-Signal responses and their synchronization (with both AMS and Digital stimuli) by the tester.
  - Response are either in analog or digital format with DC conditions.
  - Required acquisition quality description will be defined in the structures.
- Identify locations in the test program where signal treatment of the DUT responses should be done by the tester itself.
- Analog stimuli and responses are in the range from DC to a few GHz and Power could reach a few watts.

# Who should participate

- ATE Vendors
  - Credence
  - Roos Instruments
  - Advantest
  - Agilent
  - LTX
  - Teradyne
- EDA Providers
  - Synopsys ?
  - Mentor ?
  - EDActive Computing
- Users
  - Infineon
  - Frecale
  - Philips
  - Toshiba
  - Panasonic
  - TI
  - ST
- Other ?
  - LOA Technology
  - GE Consumer & Industrial
  - Segin
  - Syswave
  - Simutest
  - + Contact wtith (File translator)
    - Testinsight

# How should we work

- Regular discussions and status through e-mails
  - Already discussed with AP WP
- Regular meeting during test conferences
  - To be organized for ITC05
- Local chair by Area:
  - To organize local activities (conf call, meeting,...)
    - AP : Yasuo FURUKAWA, Advantest
    - USA : To be defined
    - EU : Jean-Louis CARBONERO, ST
- Web/audio conf-call when needed

# Activities during the last months

- Individual meeting at conferences
  - VTS, Palm Spring, USA
    - IEEE Standardization committee,
  - IMSTW / WTW, Cannes, France
    - ASIA STIL-AMS WG chair
- Local contacts and discussion with ATE suppliers
  - Credence, Teradyne, Agilent, LTX
- Studies of some part of STIL-AMS definitions inside ST
  - Proposal to be done for discussion

# Work methodology

- Document to be used as reference
  - STIL-0 : STD 1450-1999
  - STIL-1 : Draft P1450.1 D24
  - STIL-2 : STD 1450.2-2002
  - STIL-3 : Draft P1450.3 D09
  - STIL-4 : to be defined
  - STIL-6 : Draft P1450.6 D1.6

# Work methodology

- Each work based on existing/draft standard/extensions.
- Document organization
  - Follow first the one of STIL-0 (P1450-1999)
  - Add at the right place the modifications coming from other extensions (STIL-1, STIL-2...)
  - When all sections are written: rework on the document organization

# Work methodology

- Start with STIL-0
  - What we have to add for AMS ICs in clauses 1 to n ?
    - Nothing
    - Some adds, new sub-clauses or new full clauses
    - Not ready to define and write the adds (we will come back later)
    - Make, review, and adopt the proposals
- Then : what make sens ?:
  - What we have to add for AMS IC in clauses 1 to n of STIL-1
  - What we have to add for AMS IC in clauses n+1 to n+x of STIL-0
  - Split the work in several sub-working groups
- Schedule:
  - 1 week for proposals
  - 1 week for reviewing (new proposal writing can start)
  - 1 week for voting (new reviewing and proposal writing can start)
  - Adoption if every one agree
    - If not: the point has to be reworked to find an agreement
    - If no agreement at the end, the point will remain not adopted and will not be reported in the standard.

# Work methodology

- For this summer:
  - Define adds, sub-clauses and clauses to
    - STIL-0 Clauses 1 to 4
    - STIL-1 Clauses 1 to 4
    - STIL-2 Clauses 1 to 4
    - STIL-3 Clauses 1 to 4
    - STIL-6 Clauses 1 to 3
  - Proposal to be done by September 2nd
    - [jean-louis.carbonero@st.com](mailto:jean-louis.carbonero@st.com)
  - Review on W36
  - Proposal validation W37

## 14.1 Signals block syntax

**Signals** {

( SIG\_NAME < **In** | **Out** | **InOut** | **Supply** | **Pseudo** > ; )\*

( SIG\_NAME < **In** | **Out** | **InOut** | **Supply** | **Pseudo** > {

( **Termination** < **TerminateHigh** | **TerminateLow** | **TerminateOff** | **TerminateUnknown** > ; )

( **DefaultState** < **U** | **D** | **Z** | **ForceUp** | **ForceDown** | **ForceOff** > ; )

( **Base** < **Hex** | **Dec** > WAVEFORM\_CHARACTER\_LIST ; )

( **Alignment** < **MSB** | **LSB** > ; )

( **ScanIn** (DECIMAL\_INTEGER) ; )

( **ScanOut** (DECIMAL\_INTEGER) ; )

( **DataBitCount** DECIMAL\_INTEGER ; )

})\*

}

## Signal Block (Add to STIL-0, Clause 14.1)

Two new signals attributes are necessary

### Signal Block Syntax (Add to STIL-0, Clause 14.1):

```
Signals {  
  ( SIG_NAME <In | Out | Inout | Supply | Pseudo> ; ) *  
  ( SIG_NAME <In | Out | Inout | Supply | Pseudo> {  
    (Termination ...;)  
    (DefaultState ...;)  
    (Base ...;)  
    (Alignment ...;)  
    (ScanIn ...;)  
    (ScanOut ...;)  
    (DataBitCount ...;)  
    (Analog;)  
    (DigitizedAnalog;)  
  } ) *  
}
```

**Analog:** this attribute allows to distinguish analog signals from digital one. It can be associated with In, Out, Inout or Pseudo

**DigitizedAnalog:** this attribute is used to designate digital signals connected to an analog block ( e.g. DAC input, ADC output, ...). These signals are programmed as digital.

## TesterChannelMap (Add to STIL-3.D09, Clause 10)

This block allows to specify the mapping of a STIL\_AMS test sequence to a set of tester channels on tester. It follows the syntax proposed in P1450.3 (Tester Target Specification) for digital signals. The MAP\_STRING item of analog connections is defined more precisely in the following .

### TesterChannelMap – Syntax (Add to STIL-3.D09, Clause 10.1):

```
Environment (ENV_NAME)
{
  (
    NameMaps (MAP_NAME)
    {
      ( Signals { (SIG_NAME "MAP_STRING"; ) * } ) *
    }
  ) *
}
```

ENV\_NAME : user's defined simple identifier allowing to refer the test equipment

MAP\_NAME : simple identifier allowing to specify the mapping set.

SIG\_NAME: any primary or internal signal (Analog and/or Digital) already defined in Signal Block.

MAP\_STRING: {connection\_assignment} RESOURCE\_TYPE

RESOURCE\_TYPE: depends on the tester.

### **IntegraFlex application**

RESOURCE\_TYPE could be

FLX\_DC30\_VI  
FLX\_DC30\_DVM  
FLX\_DC75\_VI  
FLX\_DC75\_DVM  
FLX\_DC90\_VI  
FLX\_DC90\_DVM

### **A580 application**

RESOURCE\_TYPE could be

A58\_Matrix\_VI  
A58\_Matrix\_DVM

### **Catalyst application**

RESOURCE\_TYPE could be

Cat\_Matrix\_VI  
Cat\_Matrix\_DVM

## New Clause: AMS Block (Add to STIL-0., )

This is a new block that must appear just after Timing Block.

It defines the different AMS\_Set that will be activated during the sequence.

Each AMS\_Set defines for each impacted analog signal:

- the type of requested analog resource(s)
- the analog resource configuration
- the associated programming values.

Note: the present document describes DC resource programming only. AC and other resources will be specified in a further release

### Syntax:

#### AMS\_SetList

```
{
  ( AMS_Set (AMS_SET_NAME)
  {
    ActiveConnectionSet (CONNECTION_SET_NAME);
    ( Signal SIG-NAME
      {
        ( Resource < DC | AC | ... > (RSC_NAME)
        {
          ( Force_V = (voltage_expr); )
          ( Force_I = (current_expr); )
          ( Measure = < Strobe_V | Strobe_I | Trigger_V | Trigger_I >; )
          ( Clamp_I = (current_expr); )
          ( Clamp_V = (voltage_expr); )
          ( SlewRate = (slew_rate_expr); )
          ( Guards = < On | Off >; )
          ( Modulation = < On | Off | local >; )
          ( Delta = < On | Off | local >; )
          ( Range_V = (voltage_expr); )
          ( Range_I = (current_expr); )
          ( Filter = (frequency_expr); )
          ( Averaging = Off | { (number_of_samples); (sampling_duration) }

          } // end of current resource programming
        ) * // possibility to describe several analog resources for a given signal
      } // end of current signal
    ) * // possibility to describe several signals in a single AMS_Set block
  } // end of current AMS_Set
) * // possibility to describe several AMS_Set blocks in a STIL-AMS sequence
} // end of AMS_SetList Block
```

**AMS\_SET\_NAME:** user's defined named following requirements of a simple\_identifier

**CONNECTION\_SET\_NAME:** name of the ConnectionSet to be activated. The ConnectionSet must be previously defined in the Connection block. The ActiveConnectionSet statement is mandatory.

**SIG\_NAME:** any primary or internal Analog signal already defined in Signal Block.

**DC:** Voltage/Current source instrument

At least one of the following 2 items is mandatory. It allows to specify whether the resource is working in voltage or current source.

**Force\_V:** Voltage value to be sourced

**Force\_I:** Current value to be sourced

**Measure:** indicates type of measurement. Measure is assigned to one of the following possible values:

**Strobe\_V :** Measure one voltage value

**Strobe\_I:** Measure one current value

**Trigger\_V :** Measure a series of voltage values

**Trigger\_I:** Measure a series of current values

### ***Source programming parameters***

At least one of the two following items is mandatory

**Clamp\_I:** clamp current ( meaningful only with Force\_V)

**Clamp\_V:** clamp voltage (meaningful only with Force\_I)

**SlewRate:** optional parameter. Define signal slope or cut off frequency

**Guards:** protection against current leakage

**Modulation:** To Be Defined with AC source

**Delta:** addition inside the option of an external signal

### ***Measure programming parameters***

At least one of the two following items is mandatory

**Range\_V:** measure voltage range (meaningful with Strobe\_V and Trigger\_V)

**Range\_I:** measure current range (meaningful with Strobe\_I and Trigger\_I)

**Filter:** cut off frequency

**Averaging:** Defines if averaging is used or not. If yes , defines the number of samples and the measure duration

### ***Voltage expression and units (voltage\_expr)***

Voltage expression could be a constant or a variable (simple\_identifier)

Constant Voltage expression is enclosed in single quotes. It consists of an integer or real number followed by one of the following units

V, mV, uV, nV, pV

### ***Current expression and units (current\_expr)***

Current expression could be a constant or a variable (simple\_identifier)  
Constant current expression is enclosed in single quotes. It consists of an integer or real number followed by one of the following units  
A, mA, uA, nA, pA

### ***Frequency expression and units (freq\_expr)***

Frequency expression is enclosed in single quotes. It consists of an integer or real number followed by one of the following units  
Hz, kHz, MHz, GHz

### ***Slew Rate expression and units (slew\_rate\_expr)***

Slew rate expression is enclosed in single quotes. It could be

- an integer or real number followed by a couple of units separated by a "r". First is a voltage or current unit; second is a time unit.
- a frequency expression

**Example1:** simple configuration, where Force and Sense are performed on the same signal

```
AMS_SetList
{
  AMS_Set    Regulator_test1
  {
    ActiveConnection toto ;
    Signal    VPLUS
    {
      Resource DC
      {
        Force_V = '10V';  Clamp_I = '200mA';
        Measure = Strobe_I;  Range_I = '20mA';
        Guards = ON;        SlewRate = '400.0e03V/s';
      }
    }
  }
}
```

**Example2:** the purpose of this example is to illustrate possible more complex configurations. Here AMS\_Set XX allows to source PinA and to measure PinA as well as PinB. It is assumed that PinA and PinB are declared as primary analog signals

```
AMS_SetList
{
  AMS_Set      XX
  {
    ActiveConnection C_XX;
    Signal      PinA
    {
      Resource DC
      {
        Force_V = '10V';  Clamp_I = '200mA';
        Measure = Strobe_I;   Range_I = '20mA';
        Guards = ON;          SlewRate = '400.0e03V/s';
      }
    }
    Signal      PinB
    {
      Resource DC
      {
        Measure = Trigger_I;   Range_I = '20mA';
      }
    }
  }
}
```

**Example3:** the purpose of this example is to illustrate an AMS\_Set where a differential voltmeter is used. The measurement given by the voltmeter is performed on VM\_1 pseudo signal.

It is assumed that

- VPLUS and VLOAD are declared as primary analog signals
- VM\_1 is declared as internal analog signal. It is connected to Voltmeter in AMS\_Connection "C\_YY"

```
AMS_SetList
```

```
{
  AMS_Set    YY
  {
    ActiveConnection C_YY;
    Signal    VPLUS
    {
      Resource DC
      {
        Force_V = '10V';           Clamp_I = '200mA';
        Measure = Strobe_I;       Range_I = '20mA';
        Guards = ON;              SlewRate = '400.0e03V/s';
      }
    }
    Signal    VLOAD
    {
      Resource DC
      {
        Force_I = '100mA';        Clamp_V = '10V';
        Measure = Strobe_V;       Range_V = '10V';
        Guards = ON;              SlewRate = '400.0e03V/s';
      }
    }
    Signal    VM_1
    {
      Resource DC
      {
        Measure = Strobe_V;       Range_V = '10V';
      }
    }
  }
}
```

## New Sub-clauses in Pattern Block (Add to STIL-0, Clause 23)

### AMS\_Set selection and activation (Add to STIL-0, Clause 23)

#### AMS\_Apply statement

AMS\_Apply statement allows to select and activate the relevant AMS\_Set in "Source" mode. AMS\_Set selection is performed in the same way as WaveformTable selection except the used keyword which is **AMS\_Apply**. Once an AMS\_Set is selected, it will be activated at the beginning of the first Vector that follows.

#### Syntax:

(LABEL :) **AMSApply** (AMS\_SET\_NAME) ;

#### Example:

```
AMSApply test1;
```

## AMS\_Measure statement (Add to STIL-0, Clause 23)

AMS\_Measure statement allows to select and activate the relevant AMS\_Set in "Measure" mode. It allows to specify on which pin(s) the measurement will be performed. It also allows to specify the expected measured value(s).

AMS\_Set selection is performed in the same way as WaveformTable selection except the used keyword which is **AMSMeasure**. Once an AMS\_Set is selected, it will be activated at the beginning of the first Vector that follows.

### Syntax:

```
(LABEL :) AMSMeasure (AMS_SET_NAME)
    {
        ( (SIG_NAME) { ((voltage_expr);)* | ((current_expr);)* } ) *
    }
```

### Example:

```
AMSMeasure test1 { VPLUS {'149.85mA';} }
```

## AMSCalculationPoint location (Add to STIL-0, Clause 23)

The AMS\_CalculationPoint statement indicates the location where a calculation procedure could be launched. Name of calculation procedure is a character string that is not to be defined anywhere in the STIL-AMS sequence

### Syntax:

(LABEL :) **AMSCalculationPoint** (PROCEDURE\_NAME) { free\_comment }

### Example:

```
AMSCalculationPoint MyProcedure {"calculate pullup resistor  
from forced voltage and measured current"}
```