Wrapper Interface Port (WIP), Wrapper Instruction Register (WIR) and Wrapper Bypass

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Presentation Outline

- **Introduction & Overview**
  - Tiger Team Members, Mission & Scope
  - WIP, WIR and Bypass in the P1500 Architecture

- **Design** *Descriptions and Specifications*
  - Rules, Permissions & Recommendations
  - Wrapper Interface Port
  - Wrapper Register Architecture
  - WIR Interface to Bypass, WBR & Core
  - WIR Design and Operation
    - WIR Subordination (TBD)
  - Bypass Design and Operation
  - WIR and Bypass SIL System Chip Configuration

- **Example Implementations**
  - WIR and Bypass Implementations
  - Examples of P1500 for SoC
Team Members

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Team Mission & Scope

Specify and describe the design & operation of the Wrapper Instruction Register (WIR) and the Wrapper Bypass (WBY) in terms of an IEEE Standard: Rules, Permissions, and Recommendations.

- WIR & Bypass within the P1500 Wrapper Register Architecture
- Wrapper Interface Port (WIP) for WIR & Bypass
- WIR design and operation (Capture, Shift, Update, Reset, etc.)
- WIR interface to Bypass, WBR and Core
- Wrapper Bypass design and operation
- WIR & Bypass in SIL System Chip configuration
- Examples of WIR & Bypass implementations and SoC configurations
WIR Tiger Team Terminology

**WIP**: Wrapper Interface Port. Terminals on P1500 Wrapper for scan, controls & clocks.

**WSI & WSO**: Wrapper Scan In and Wrapper Scan Out

**WIR**: Wrapper Instruction Register. Used to shift in and update instructions to wrapper.

**WBR**: Wrapper Boundary Register.

**WDRs & CDRs**: Wrapper Data Registers and Core Data Registers. Either can be a user defined scan register. WBR and Bypass are WDRs, internal core scan chains are CDRs.

**WR**: Wrapper Register. Registers in the “wrapper” as opposed to the “core”. WIR, WBR, Bypass and user WDRs are included in WRs.
SIL & TAM: Serial Interface Layer and Test Access Mechanism. The SIL is the standard P1500 WSI-WSO with associated registers and circuitry. The TAM provides parallel test access and is user defined.

Wrapper Instruction: Currently active wrapper instruction, as was previously updated in the WIR.

Operation: A protocol sequence applied to the WIP terminals that causes a particular behavior to occur in the P1500 Architecture components.

Selected Register: The currently selected WR(s), or CDR(s). All register selections are determined by the WIP signals and the Wrapper Instruction. Subsequent WIP operations are then performed on the selected register(s).
Overview of P1500 Architecture Components
WIP, WIR & Bypass in the P1500 Architecture

- **WIP**: Includes WSI, WSO and Controls/Clocks for SIL & TAM
- **WIR**: Instruction control of Wrapper Components & Core Modes
- **Bypass**: Scan bypass through WSI-WSO
Wrapper Interface Port (WIP)

Description

- The WIP is currently defined to control & clock the WIR and Bypass
  - It could also control and clock other WDRs, CDRs (e.g., the WBR, internal scan, etc,) and TAMs.

- WIP Wrapper Terminals:
  - WRCK is one or more clocks used to operate registers
  - WRSTN is a dedicated asynchronous Wrapper Reset
  - SelectWIR selects whether or not the WIR is connected between WSI-WSO
  - UpdateWR, ShiftWR and CaptureWR are enables for register operations
    - May be used for gating WRCK clock rather than data enables
Wrapper Register Architecture

Description: WIR and Bypass

- The SelectWIR terminal causes the WIR to be the selected WR.
  - SelectWIR must be de-asserted (logic 0) to select WDRs or CDRs.
- When SelectWIR is logic 0, the updated WIR contents then determines:
  - Which WDRs or CDRs are selected
  - The current P1500 Wrapper Modes and (optionally) the Core Modes
  - If a user defined TAM connection & register configuration are enabled
- The selected register can the be operated through the SIL, or a TAM
WIR Interface to Bypass, WBR & Core

Description

- WIR Circuitry includes: WIR shift stage, decode logic and WIR update
- The WIR interface to the Bypass, WBR and Core:
  - Controls selection of which WDR or CDR to connect to the WSO output
  - Controls operations for the Bypass, WBR and optionally other WDRs or CDRs
  - May output Core Modes & controls for other WDRs/CDRs
  - WIP signals may also interface directly to WDRs, CDRs, and the Core
The WIR circuitry is controlled & clocked by the WIP and provides:

- Serial shift of the WIR contents from WSI to WSO
- Wrapper Instruction decode and update circuitry
  - Generates Wrapper and Cores Modes based on Wrapper Instruction
  - Ensures that Modes remain stable during WIR shift operations
- Optional parallel capture of test control information into the WIR
  - Can also be utilized for testing of WIR logic & WIR scan path
The Wrapper Bypass Register (WBY) provides a single bit scan bypass of the Wrapper’s SIL, from WSI to WSO.

The WBY is controlled & clocked by the WIP (e.g., WRCK, WSI) and WIR Circuitry (e.g., WBY_Cntrl signals).

- The WBY Control signals from the WIR Circuitry are generated based on the current Wrapper Instruction and the WIP.
- WBY can only be selected when the WIP SelectWIR signal is logic 0.
P1500 Example Implementations

Wrapper Instruction Register (WIR)

WIR Opcodes
- WBYPASSOpcode = 3'b001
- WPRELOAD_Opcode = 3'b010
- WEXTEST_Opcode = 3'b011
- SAFESTATE_Opcode = 3'b100
- WCLAMP_Opcode = 3'b101
- COREBIST_Opcode = 3'b110

UpdateStage
- WBYPASS = [5]
- WPRELOAD = [4]
- WEXTEST = [3]
- SAFESTATE = [2]
- WCLAMP = [1]
- COREBIST = [0]
P1500 Example Implementations

Wrapper Bypass Register (WBY)