

Unapproved IEEE P1500 Working Document



***Overview the Proposed IEEE
P1500 Scaleable Architecture for
Testing Embedded Cores***

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Presentation Outline

□ Introduction

- **CTAG Task Force Mission and Scope**

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- **A System Chip with P1500 Cores**

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□ P1500 Wrapped Core Examples

- **Core with internal scan connected to TAM**

P1500 Architecture Task Force

Summary of Task Force Mission and Scope

Goals of IEEE P1500

Standardize a Core Test Architecture which:

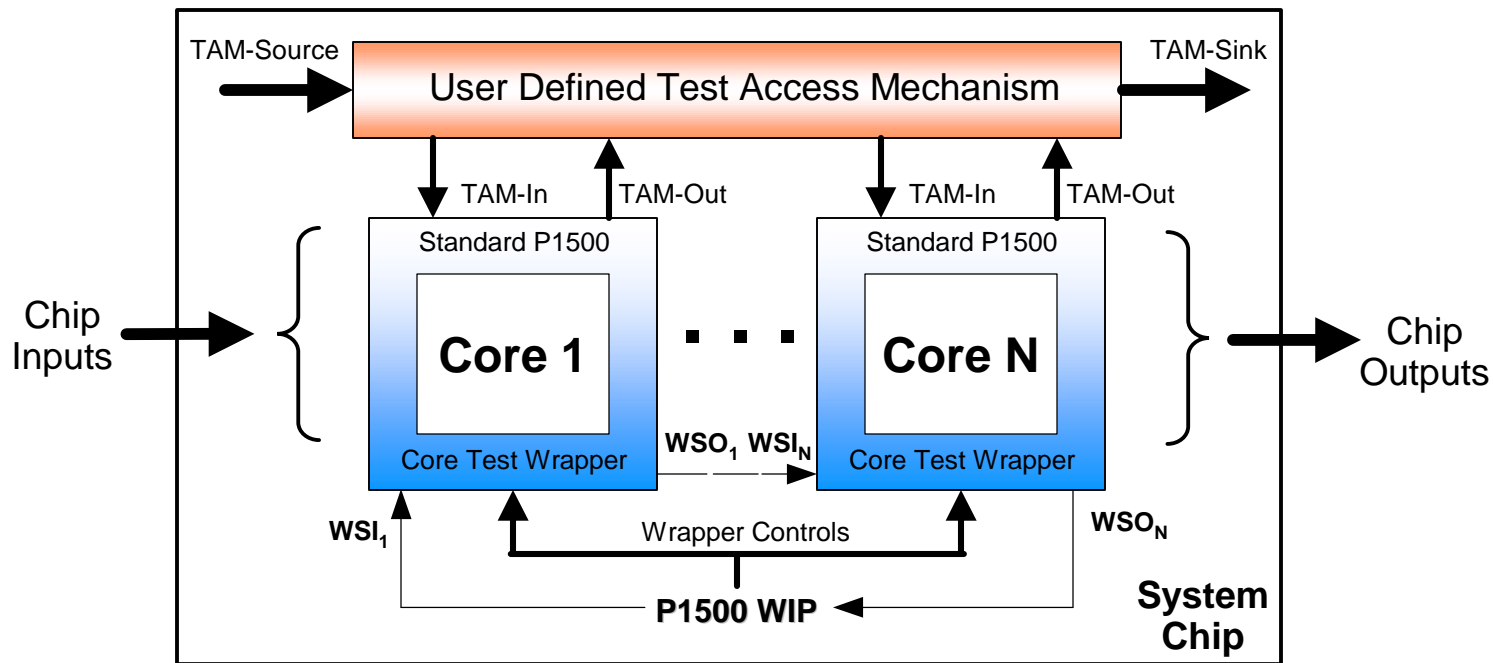
1. Defines a core test interface between an embedded core and the system chip.
2. Facilitate test reuse for embedded cores through core access and isolation mechanisms, and provide testability for system chip interconnect and logic.
3. Facilitates core test interoperability, with plug-and-play protocols, in order to improve the efficiency of test between core providers and core users.

Scope of IEEE P1500

- ✓ Standardize *core* test mechanisms, for core access and isolation, including protocols and test mode control.
- ✗ *System Chip* test access mechanism is defined by the system chip integrator.
- ✗ The *core test method* is defined by the core provider – P1500 supports, and enables, various different methods (e.g., scan, BIST, I_{ddq} , etc.).

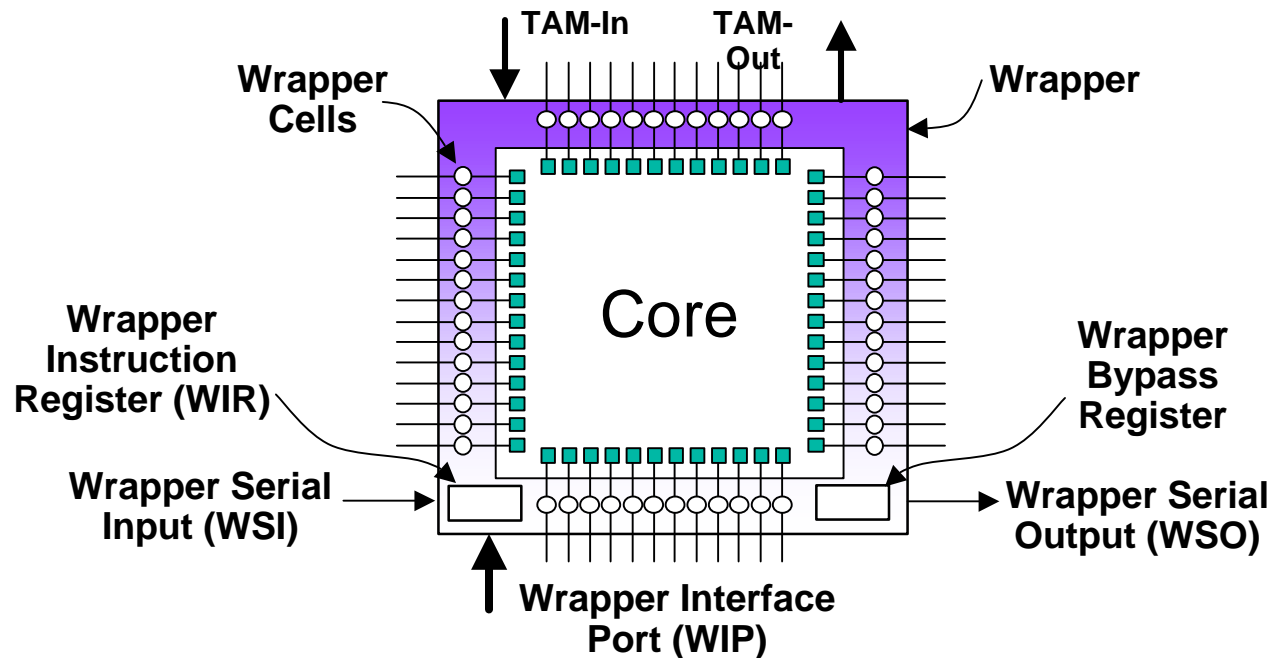
Overview of P1500 Architecture

System Chip with P1500 Cores



- **TAM Source/Sink**
 - ✓ From chip I/O, test bus/rail, BIST, etc...
- **TAM In/Out**
 - ✓ 0 to n lines for parallel and/or serial test data, or test control
- **P1500 Wrapper Interface Port (WIP)**
 - ✓ From chip-level TAP Controller, chip I/O, etc...

P1500 Architecture Components



□ A P1500 Wrapper has the following:

- A WIR for providing wrapper mode control
- Wrapper Cells to provide test functions at the core terminals
- A Bypass register for scan bypass through the wrapper
- The WIP for standard serial control (WIR, Bypass & WBR) and optionally TAM control

P1500 Wrapper Instructions

Proposed Standard Instructions

WBYPASS

- Wrapper allows normal core inputs/outputs to pass through the wrapper for normal system operation, selects the Bypass.

CORETEST 1–N

- Wrapper is configured to disable the core's normal mode and enables core internal test.
- Core test methods, registers, and access mechanisms (i.e., a parallel TAM source/sink or the standard wrapper serial input/output) are user defined.

WEXTEST

- Wrapper is configured to disable the core's normal mode and the WBR is selected between WSI-WSO for test between cores (e.g., UDL).

P1500 Wrapper Instructions

Proposed Standard Instructions continued

SAFESTATE

- Wrapper configured to disable the core's normal mode and the state of wrapper terminals are controlled to predefined safe states, selects the Bypass.

WCLAMP

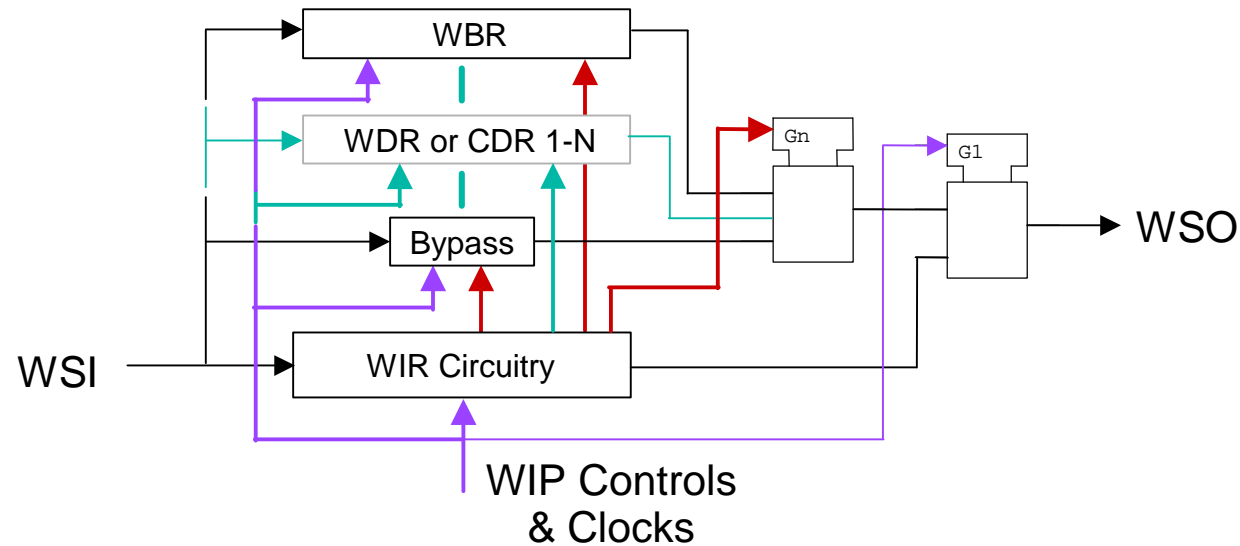
- Wrapper configured to disable the core's normal mode and the state of wrapper terminals are controlled by the WBR, selects the Bypass.

WPRELOAD

- Wrapper allows normal core inputs/outputs to pass through the wrapper for normal system operation, selects the WBR.

P1500 Wrapper Registers

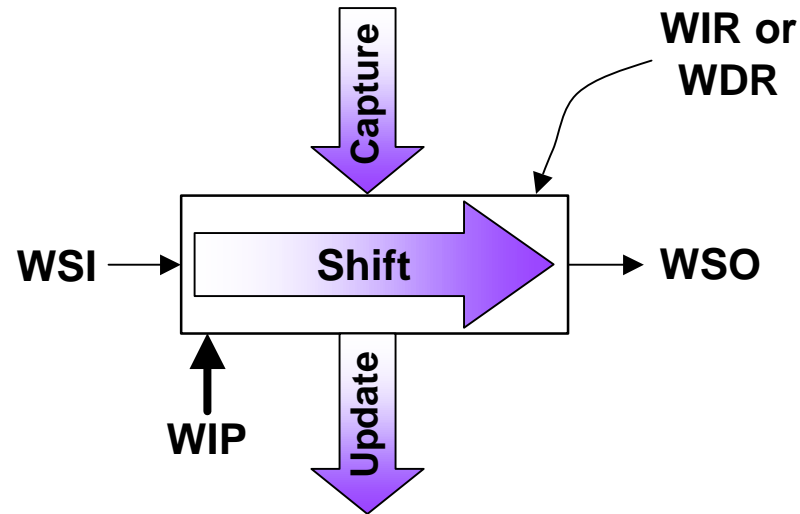
Wrapper Register Architecture



- ❑ **WIP selects if WIR or other register is connected to WSI-WSO**
 - SelectWIR is de-asserted to select other registers, i.e. Bypass, WBR, WDRs, or CDRs
- ❑ **Updated WIR contents determines:**
 - Which WDR or CDR gets connected between WSI-WSO
 - The current P1500 Wrapper Mode and (optionally) the Core Mode
 - If a user defined TAM connection & register configuration is enabled
- ❑ **The Wrapper Bypass Register provides a scan bypass of WSI-WSO**

P1500 Wrapper Registers

WIR and WDR Behavior

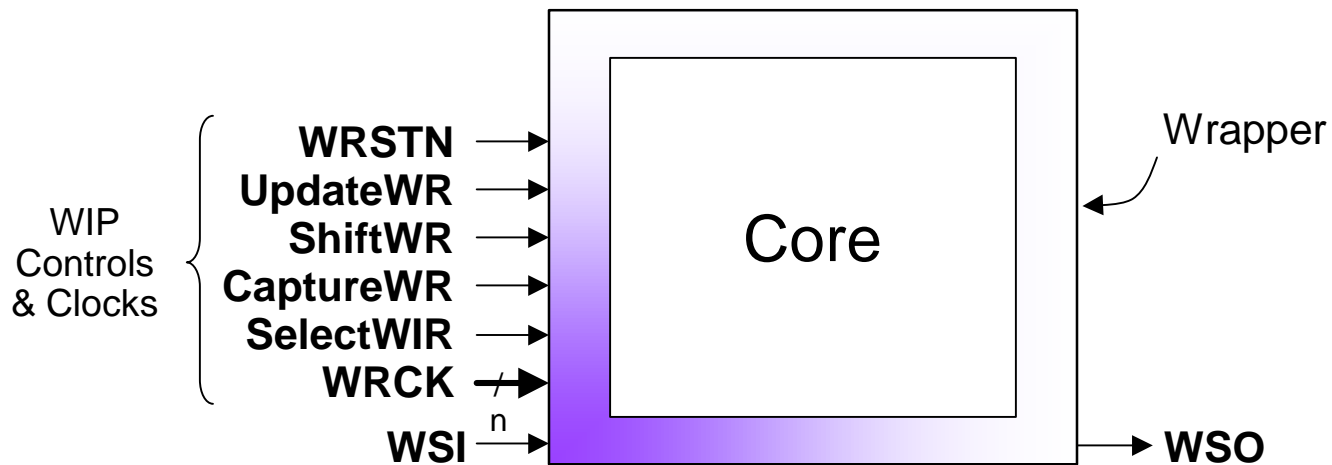


□ Standard P1500 Wrapper Registers provide:

- **Serial *Shift*** of the WR contents from WSI to WSO
- **Optional parallel *Update***
 - ✓ Holds updated shift data stable
 - ✓ Required for WIR to prevent Wrapper & Core Modes from toggling during WIR shift
- **Optional parallel *Capture***
 - ✓ Required for WBR to provide interconnect and UDL test capability
 - ✓ Optional for WIR to provide capture of test control information, or for testing of WIR circuitry & WSI-WSO scan paths

Wrapper Interface Port (WIP)

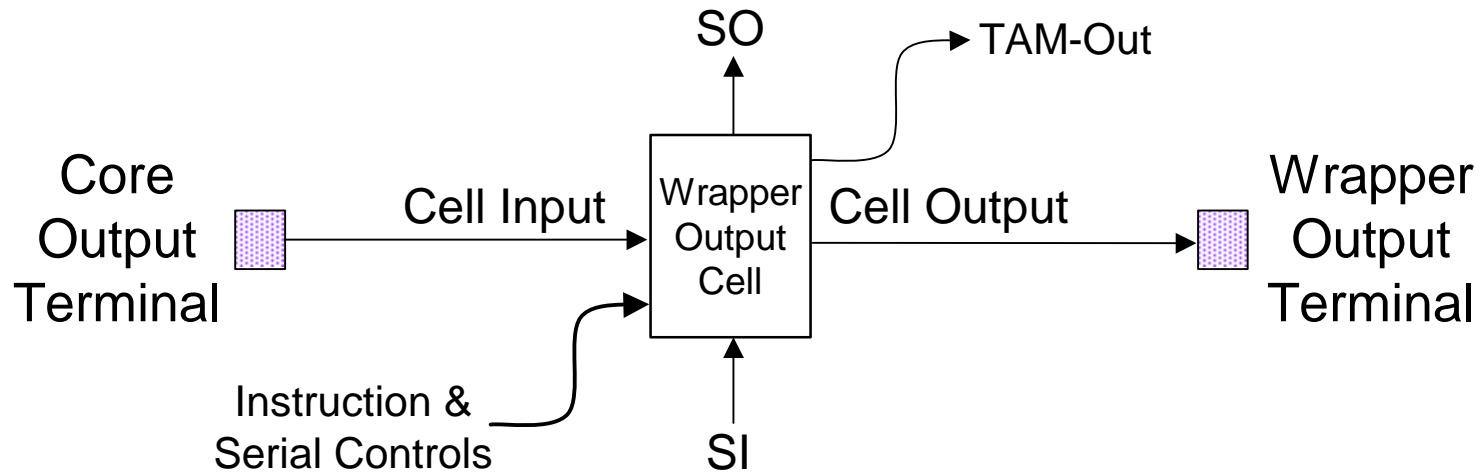
WIP for WIR and Bypass



- ❑ The WIP is currently defined to support the WIR and Bypass
 - Could also support other WDRs & CDRs (e.g., WBR, internal scan)
- ❑ WIP Terminals:
 - WRCK is one or more clocks used to operate registers
 - WRSTN is a dedicated asynchronous Wrapper Reset
 - SelectWIR selects whether or not the WIR is connected between WSI-WSO
 - UpdateWR, ShiftWR and CaptureWR are enables for register operations
 - ✓ May be used for clock generation/clock gating

P1500 Wrapper Cell Example

Dedicated Output Cell with Update Stage & TAM-Out



❑ Cell behavior in response to Wrapper Instructions

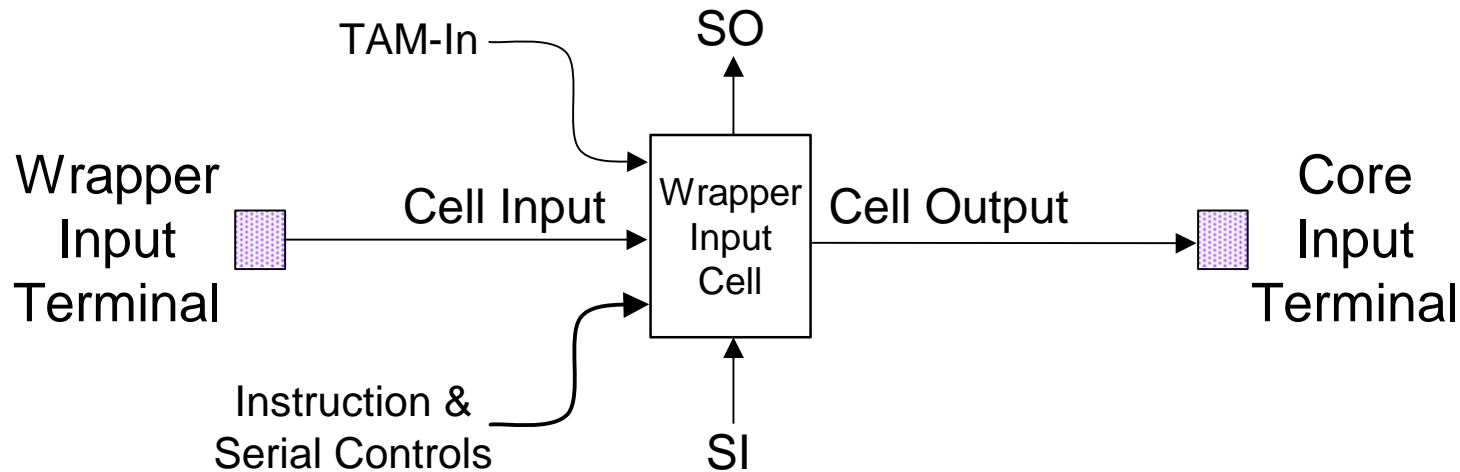
- ✓ Normal: Cell output connects to Cell input
- ✓ Serial External Test: Cell output is sourced from cell's update stage
- ✓ Isolation: Cell output is appropriately disabled or constrained
- ✓ Core Test 1: TAM-Out is sink & provides output observation for core test

❑ Cell behavior for Wrapper Scan Protocol

- 1) Captures data at cell input
- 2) Shifts data from scan input (SI) to scan output (SO)
- 3) Updates shift stage data to update stage

P1500 Wrapper Cell Example

Dedicated Input Cell with Update Stage & TAM-In



❑ Cell behavior in response to Wrapper Instructions

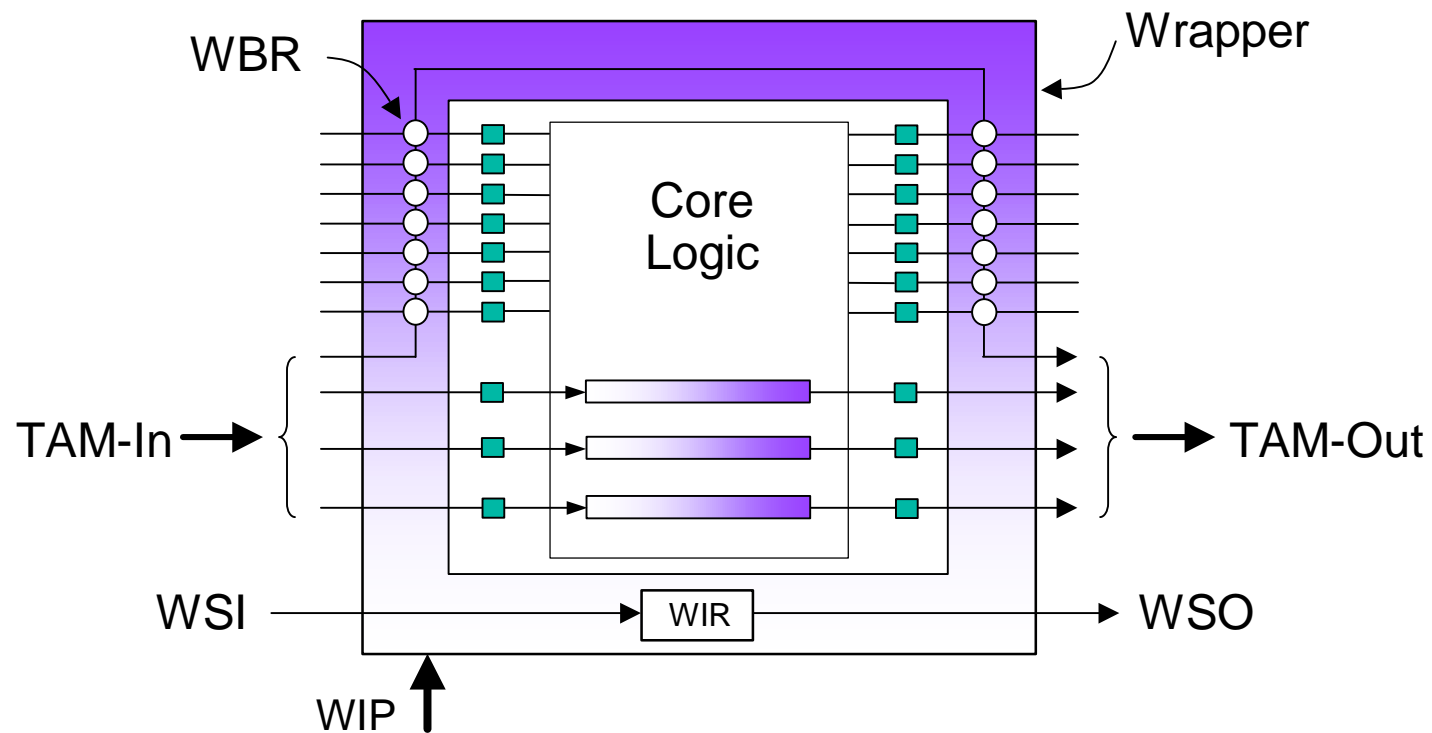
- ✓ **Normal:** Cell output connects to Cell input
- ✓ **Serial External Test:** Cell input is captured into cell's shift stage
- ✓ **Isolation:** Cell output is appropriately constrained
- ✓ **Core Test 1:** TAM-In is source & provides input control for core test

❑ Cell behavior for Wrapper Scan Protocol

- 1) Captures data at cell input
- 2) Shifts data from scan input (SI) to scan output (SO)
- 3) Updates shift stage data to update stage

P1500 TAM Connection Example

Core with Parallel Internal Scan



- ❑ Core internal scan paths & WBR are connected in parallel to TAM by a Core Test instruction
- ❑ Many other TAM connections and configurations are possible !