

# The need for Functional Testing in True System-On-Chip

Ian Phillips FIEE  
Strategic Technologist  
ARM Ltd. Cambridge, UK.

*[ian.phillips@arm.com](mailto:ian.phillips@arm.com)*

## See ... ARM7TDMI 'System-Chip'

A Commercial GSM Base-Band Processor Chip ...

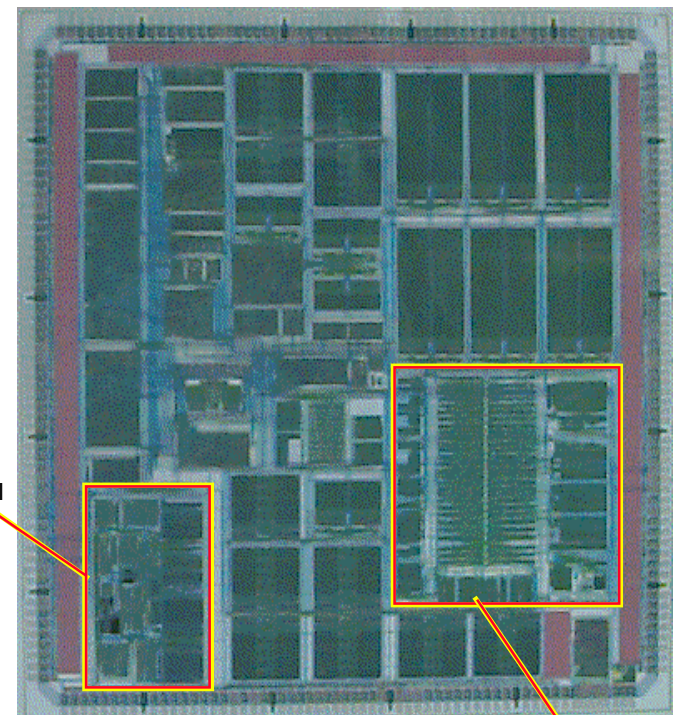
### System-Level Integration (Dataquest '95)

- A Compute engine
- 100k used gates
- Significant on-chip memory

### GSM Base-band Processor (circa '96)

- Two Compute Engines (ARM & OAK)
- ~ 400k gates
- ~100 kB on-chip memory

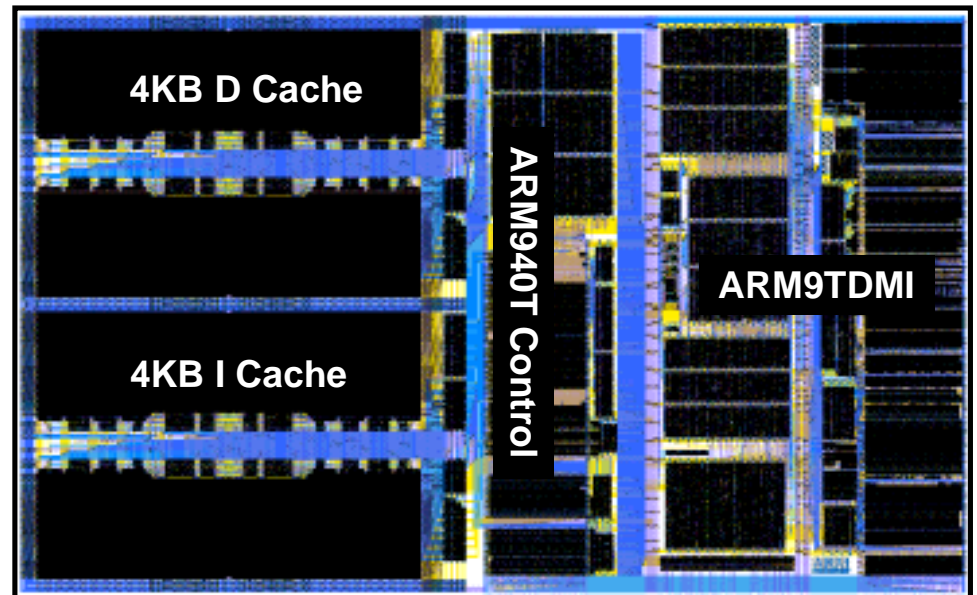
*... A 'full-chip' on 0.5u (~9x9 mm)*



OAK DSP

## See ... ARM940T Macrocell

- ARM9TDMI Harvard Architecture, CPU Core
- 2x4KB Harvard Cache with lock-down
- AMBA on-chip-bus interface
- ~240MIP at 200MHz
- Memory protection unit
- ARM/Thumb instruction set
- EmbeddedICE debug support

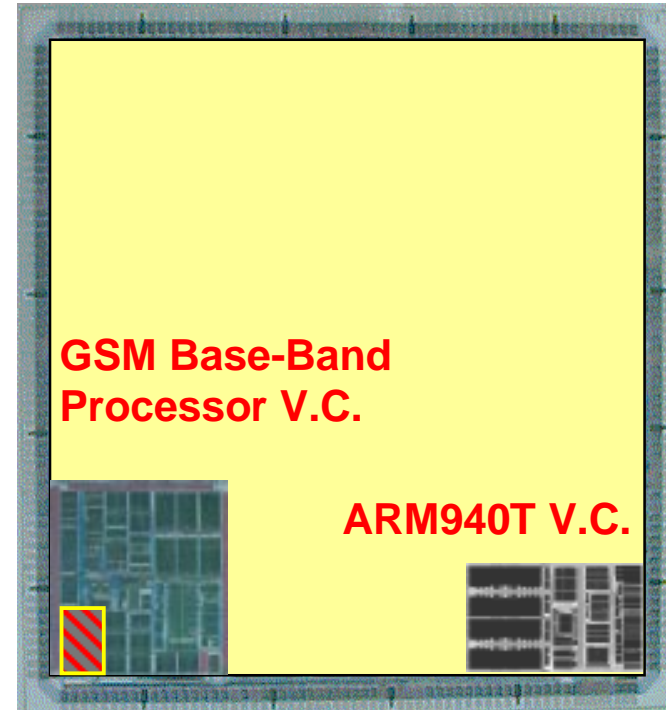


*~ 8 mm<sup>2</sup> on 0.25u ...*

## *Believe ... The Whole System on Silicon!*

0.12u ... 100M transistors ...  
... capacity for *incredible* functionality ...

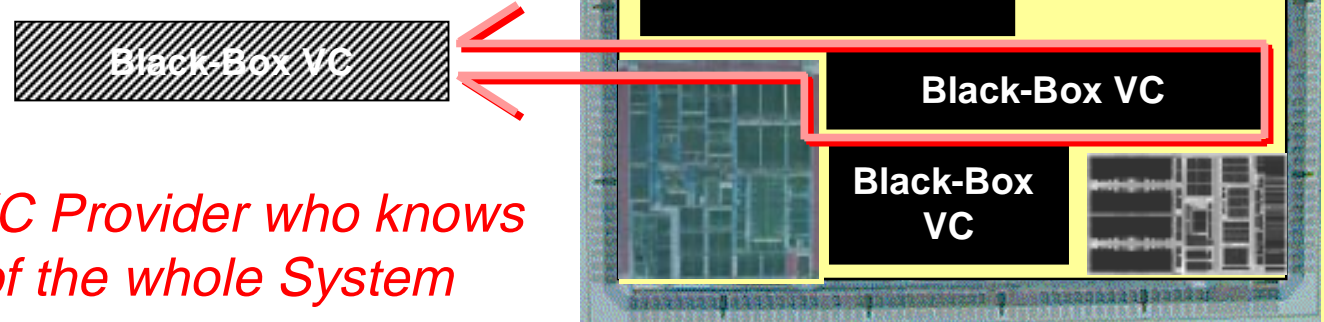
- ~ x 8 Logical capacity of 0.5u ...  
~ x 2 Frequency ...  
... x 16 Functional Capacity !  
*... This is x2/year !*
- Will be implemented out of Components and Sub-Systems.
- Not the sole domain of hardware, but a Functional alloys of HW & SW.
- Will be an incredible design challenge for today's methods and tools



*... Lead players are facing System-Level design today!*

# Virtual Extraction

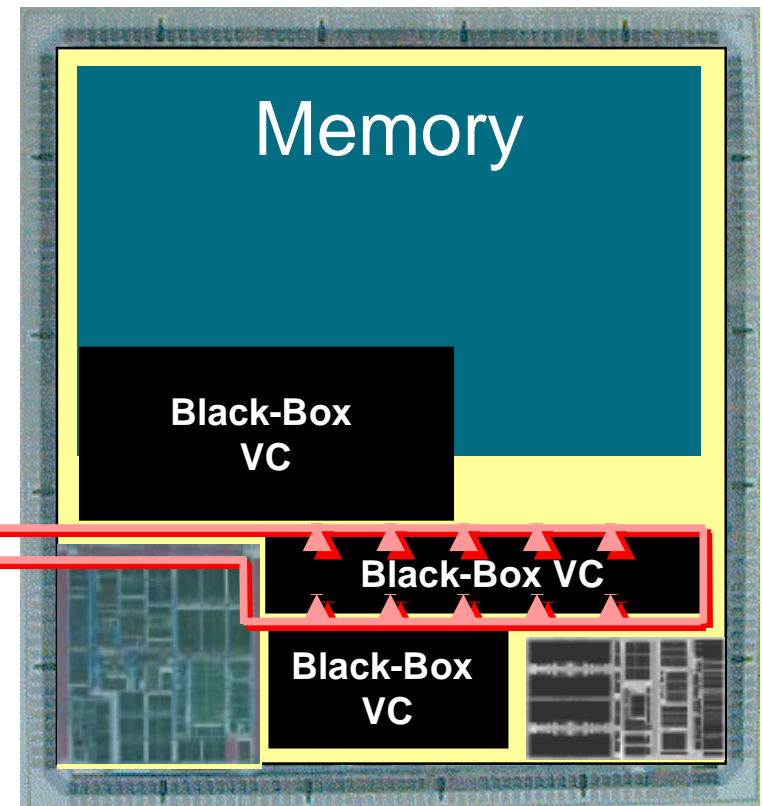
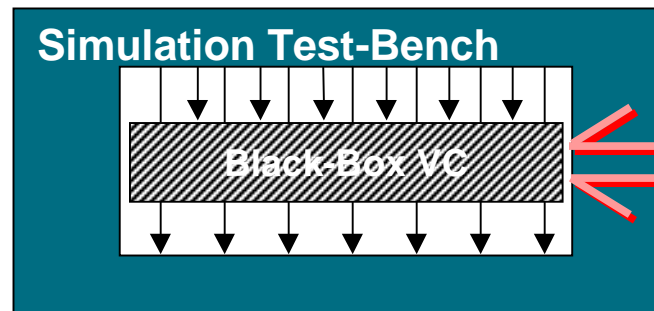
- The need for isolated access to hw & sw VCs ...
  - To analyse its environment
  - To investigate details of its operation
  - To act as a simulation accelerator
  - To validate its functionality



*... By the VC Provider who knows nothing of the whole System*

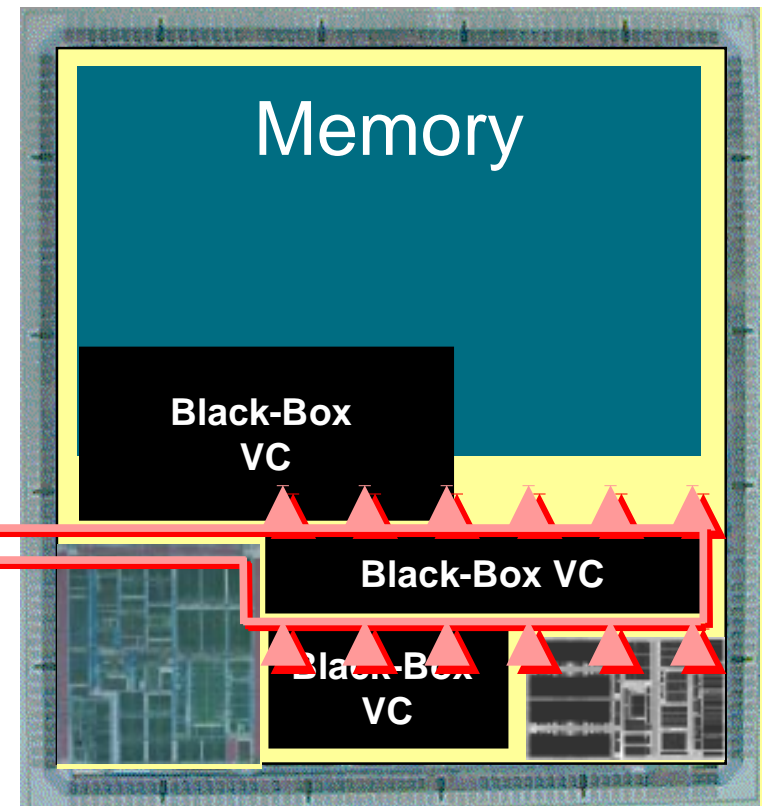
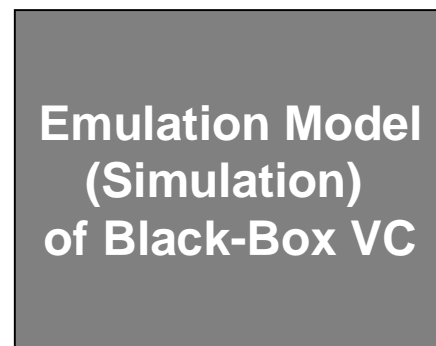
# Functional Analysis

- Exercise the VC from simulation environment ...
    - To gain better understanding of the VC operation.
    - To enable the simulation of larger data-sets (acceleration).
    - To assist with architecture debug or development.
- ... Also, Physical Validation*



# Environment Analysis

- To investigate the real interface effects ...
  - Emulation modelling of the VC on a simulation engine...
  - ... Drive *real* outputs
  - ... Respond to *real* inputs
- ... *Not real time, but much nearer than pure simulation can achieve*



## Functional Test

- To establish that the Target VC, works as Simulated, and as Required, within the context of the assembled physical System.
- Requires ...
  - The ability to access the Target VC at its pins ...
    - Without 'Breaking' the Target VC Functionality
    - Without 'Breaking' its Environment Functionality
  - Supports At-Speed and IO-Timing verification.
  - For Hardware, Software and Mixed VCs

# Implementation

- Access ... (Ah-La P1500)
  - Standard Physical Interface Port
  - Supplementary non-functional / multiplexed pins
- Features ...
  - VC Peripheral Scan-Chain
    - Sampling behind Input Registers
    - BIST-able for at-speed and random functional test
  - CPU accessible 'Parallel-Port'
    - Offers equivalent access to Software and Mixed VC

## Conclusion

- P1500 supports the Structural test needs of the most complex SoC Manufacturing.
- But ... Component Based SoC Product Introduction needs Functional Test support to get through the hierarchical Physical Validation and Qualification stages.
- As the needs are so similar, that P1500 should be revised to make sure they are included.

*... TTM is the main issue. Testability is a prerequisite, but not the only one ... It must also work !*

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[lan.phillips@arm.com](mailto:lan.phillips@arm.com)

