

Unapproved IEEE P1500 Working Document



***Overview of Proposed IEEE P1500
Scaleable Architecture for Testing
Embedded Cores***

Presented on behalf of the CTAG Team by

Mike Ricchetti

June 20, at DAC 2001

Presentation Outline

□ Introduction

- **CTAG Task Force Mission and Scope**
- **CTAG Members, Organization & Development Phases**

□ P1500 Architecture

- **System Chip with P1500 Wrapped Cores**
- **P1500 Wrapper Architecture**
- **Wrapper Serial Interface Layer (SIL) Architecture**
- **Wrapper Interface Port (WIP)**
- **Wrapper Boundary Register (WBR) Cells**
- **Wrapper Example with a Parallel TAM Interface**
- **System Chip SIL Connections**

□ P1500 Wrapper Instructions

□ Status update since VTS 2001

P1500 Architecture Task Force

Summary of Task Force Mission and Scope

Goals of IEEE P1500

Standardize a Core Test Architecture which:

1. Defines a core test interface between an embedded core and the system chip.
2. Facilitate test reuse for embedded cores through core access and isolation mechanisms, and provide testability for system chip interconnect and logic.
3. Facilitates core test interoperability, with plug-and-play protocols, in order to improve the efficiency of test between core providers and core users.

Scope of IEEE P1500

- ✓ Standardize *core* test mechanisms, for core access and isolation, including protocols and test mode control.
- ✗ *System Chip* test access mechanism is defined by the system chip integrator.
- ✗ The *core test method* is defined by the core provider – P1500 supports, and enables, various different methods (e.g., scan, BIST, I_{ddq} , etc.).

P1500 Architecture Task Force

Current Task Force Members

Lee Whetsel (Task Force Chair) - Texas Instruments

Saman Adham - LogicVision

Louis Basto - Analog Devices

Dwayne Burek - LogicVision

★ Francisco da Silva - Synopsys

Bulent Dervisoglu - Cadence

Jason Doege - Inovys

Grady Giles - AMD

Alan Hales - Texas Instruments

Andy Halliday - TriMedia Technologies

Douglas Kay - Cisco Systems

Erik Jan Marinissen - Philips

★ Teresa McLaurin - ARM

Fidel Muradali - Agilent Technologies

Rochit Rajsuman - Advantest

★ Mike Ricchetti - Intellitech

Paul Soong - Nortel

Wu Tung - Mentor Graphics

Jon Udell - Palmchip

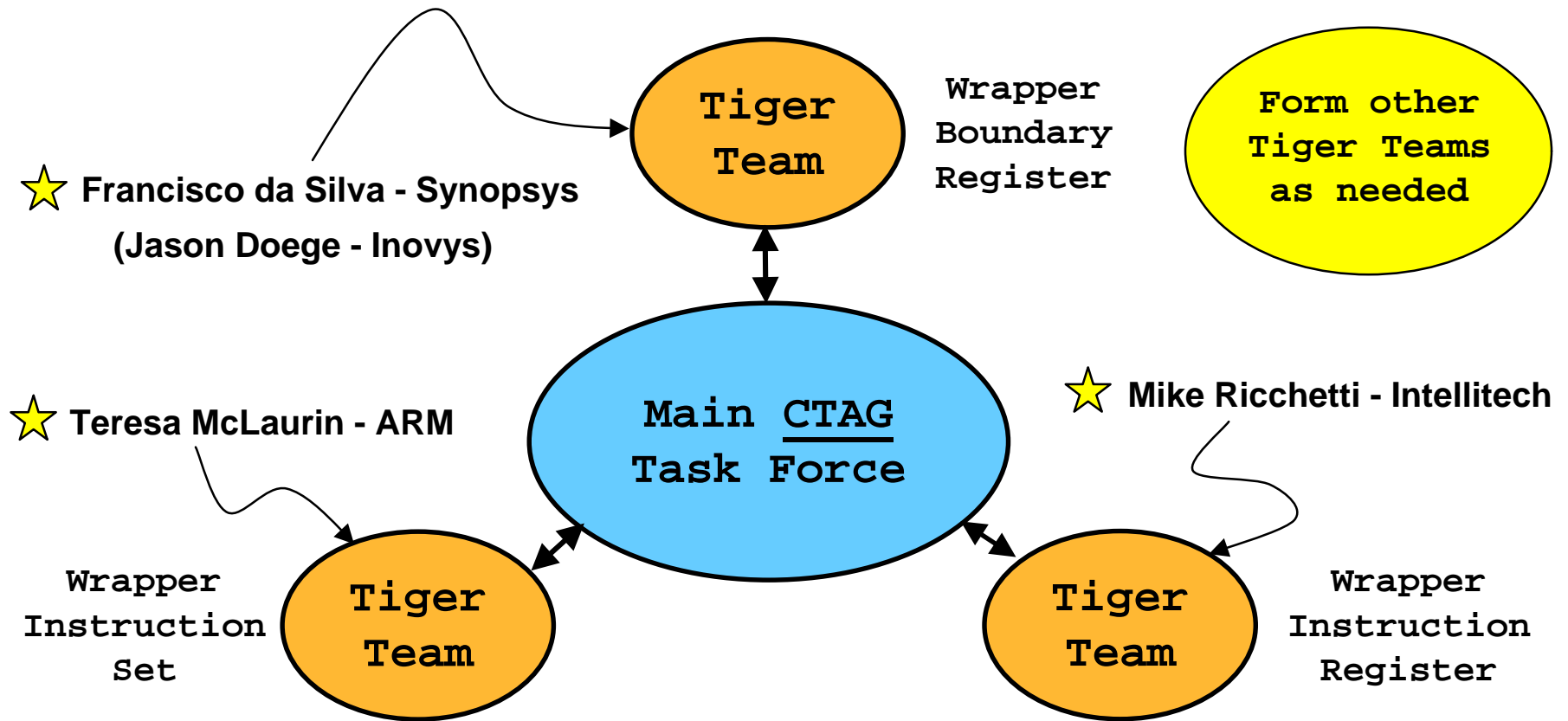
Ron Walther - IBM

Yervant Zorian - LogicVision

★ - Tiger Team Champions

P1500 Architecture Task Force

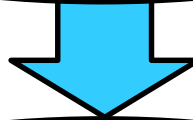
Organization of Task Force



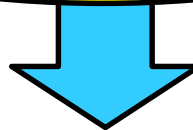
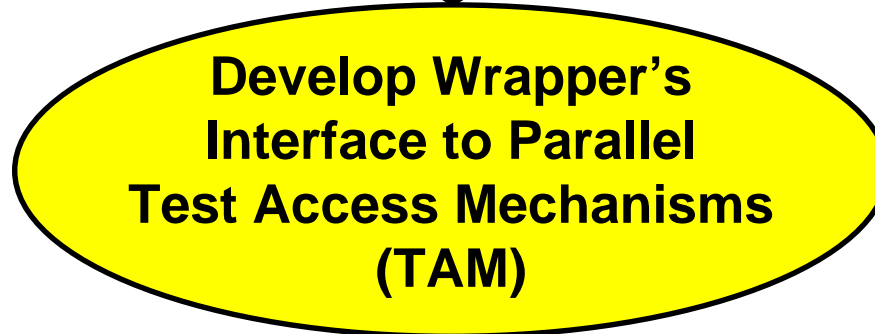
P1500 Architecture Task Force

Task Force Wrapper Development Phases

Phase 1



Phase 2

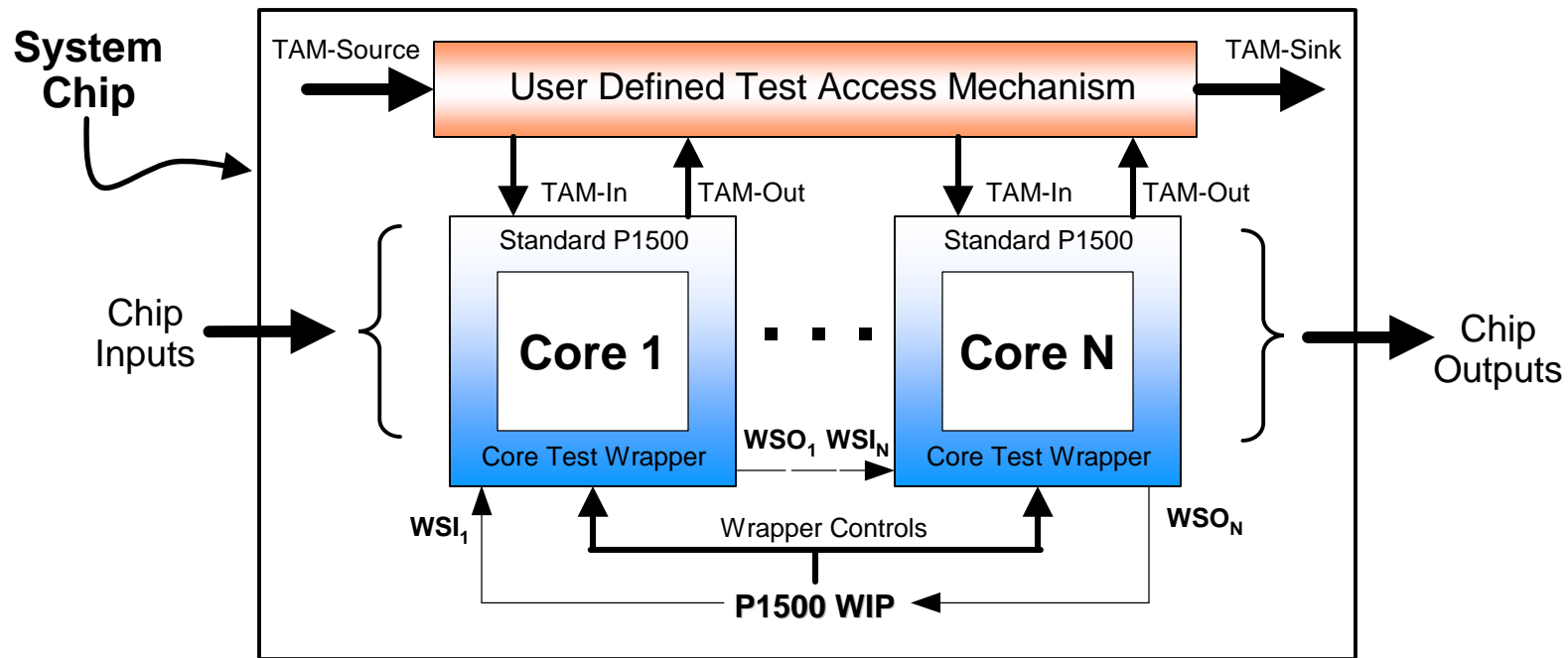


P1500 Standard

P1500 Architecture

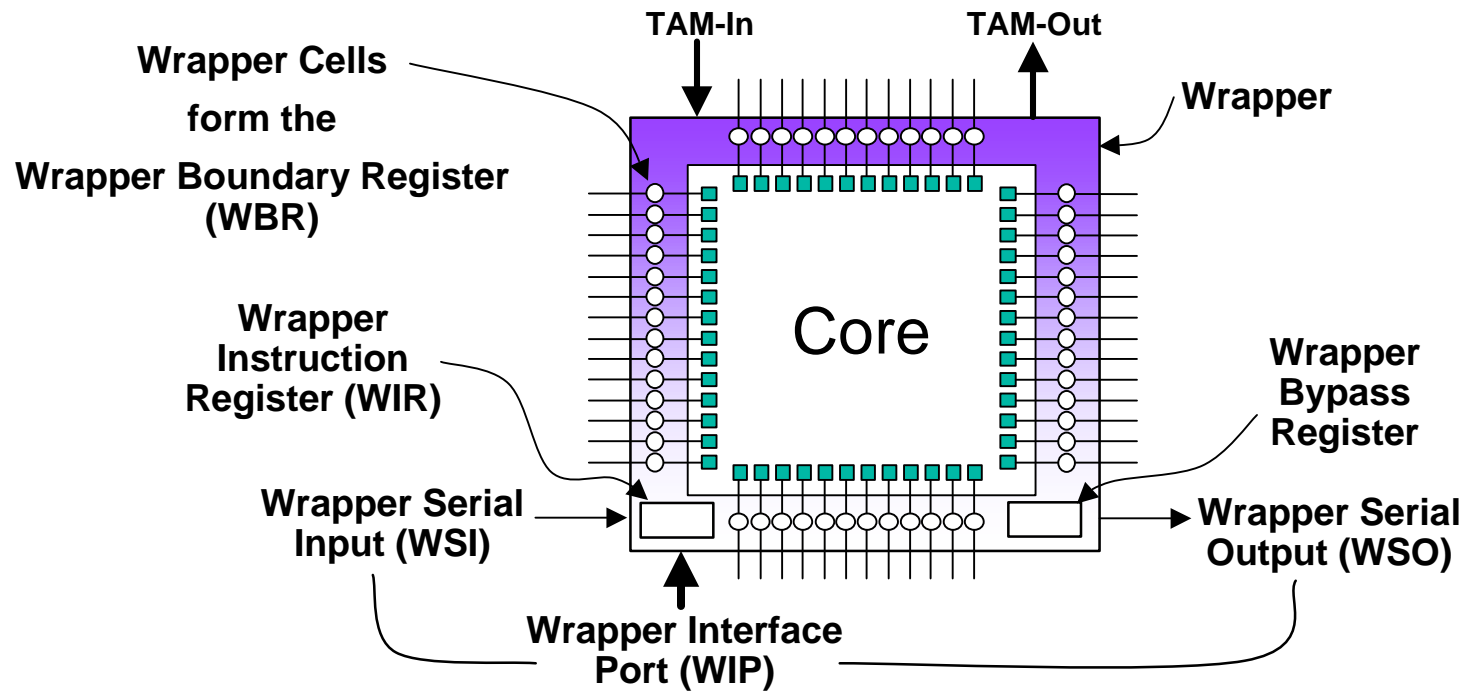
P1500 Architecture

System Chip with P1500 Wrapped Cores



- **TAM Source/Sink**
 - ✓ From chip I/O, test bus/rail/port, BIST, etc...
- **TAM In/Out**
 - ✓ 0 to n lines for parallel and/or serial test data, or test control
- **P1500 Wrapper Interface Port (WIP)**
 - ✓ From chip-level TAP Controller, chip I/O, ...

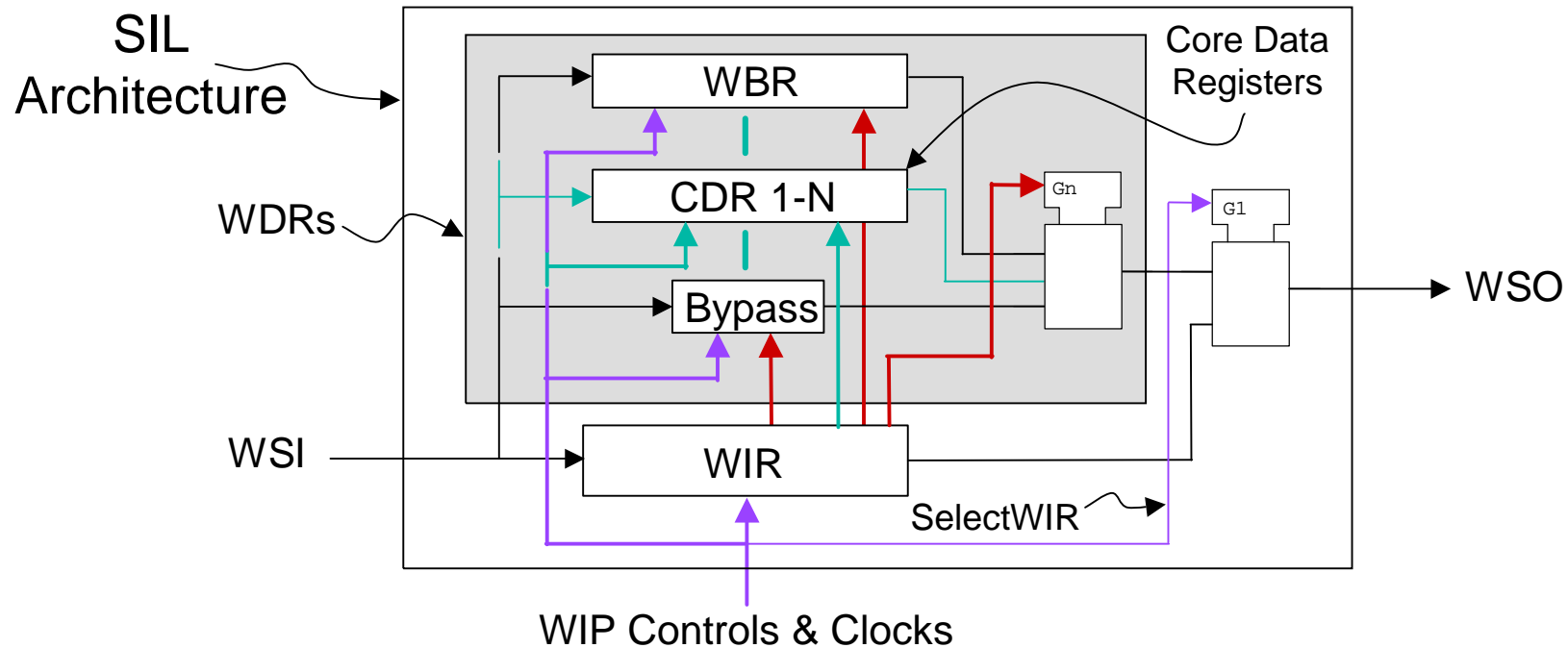
P1500 Architecture Components



□ P1500 Wrapper:

- WIR for loading wrapper instructions
- WBR with Wrapper Cells at each terminal
- A Bypass register for the SIL
- WIP for control of Wrapper Registers via SIL
 - ✓ May also provide controls for PIL/TAM

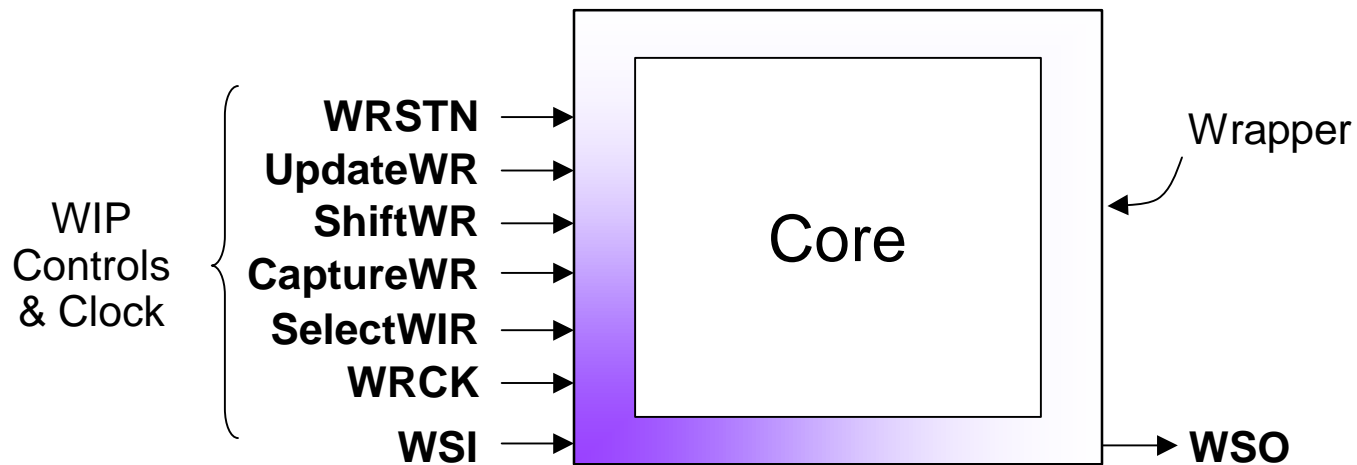
P1500 Serial Interface Layer Architecture



- ❑ WIP selects the WIR or a Wrapper Data Register (WDR) between WSI and WSO
- ❑ Updated WIR output determines:
 - Which WDR (i.e. Bypass, CDR, or WBR) is selected between WSI and WSO
 - The current P1500 Wrapper Mode and (optionally) the Core Mode
 - If a user defined TAM connection & register configuration is enabled
- ❑ The Wrapper Bypass Register provides a scan bypass from WSI to WSO

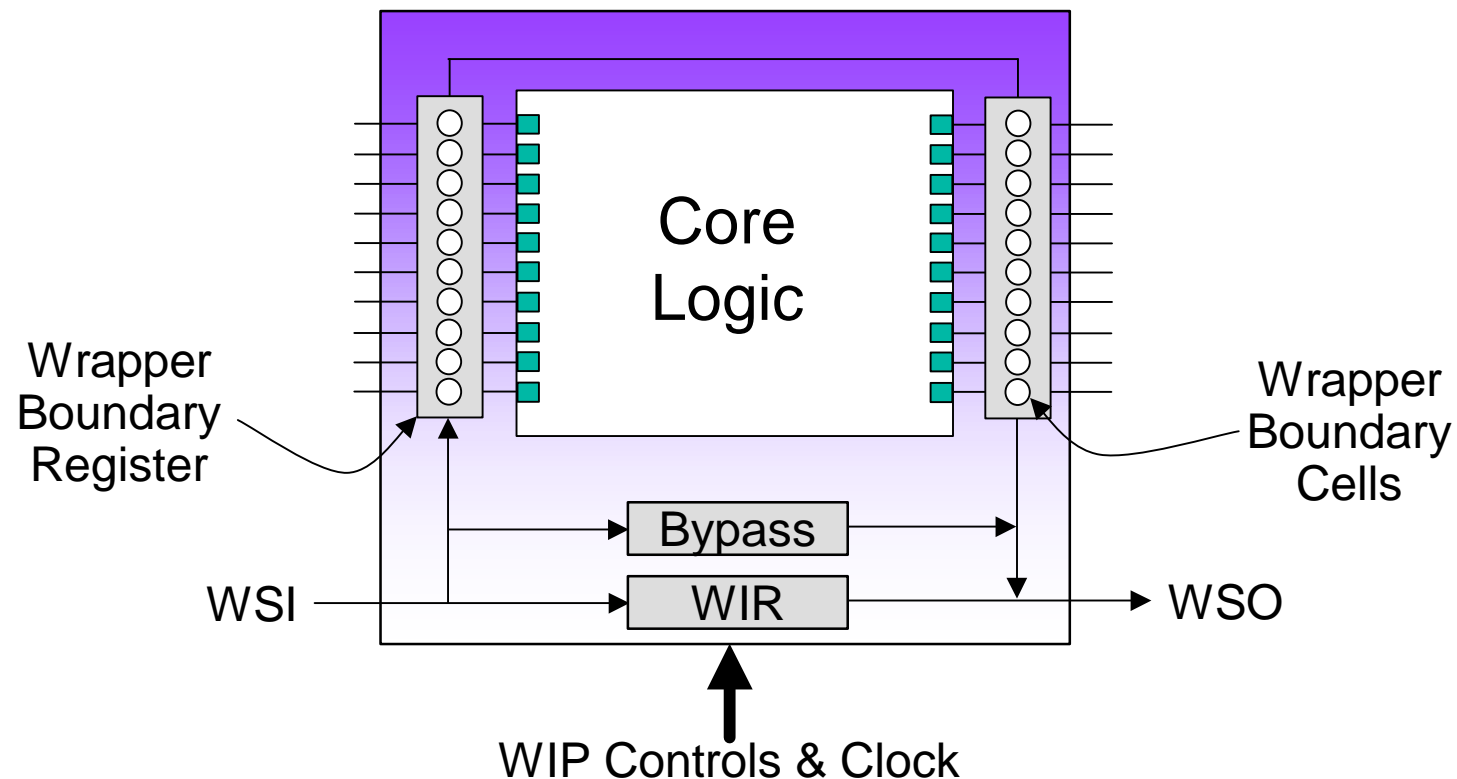
P1500 Wrapper Interface Port (WIP)

WIP Signals for Accessing WIR, Bypass & WDRs



- ❑ The WIP is used to access the WIR, Bypass & other data registers via the SIL
- ❑ WIP Terminals:
 - WRCK is the wrapper clock
 - ✓ Dedicated for WIR and BYPASS, WBR may also use “auxiliary” clock(s)
 - WRSTN is a an asynchronous Wrapper Reset
 - SelectWIR selects whether the WIR or DR(s) is connected between WSI and WSO
 - UpdateWR, ShiftWR and CaptureWR are enables for register operations
 - ✓ May be used for gating WRCK clock internal to Wrapper

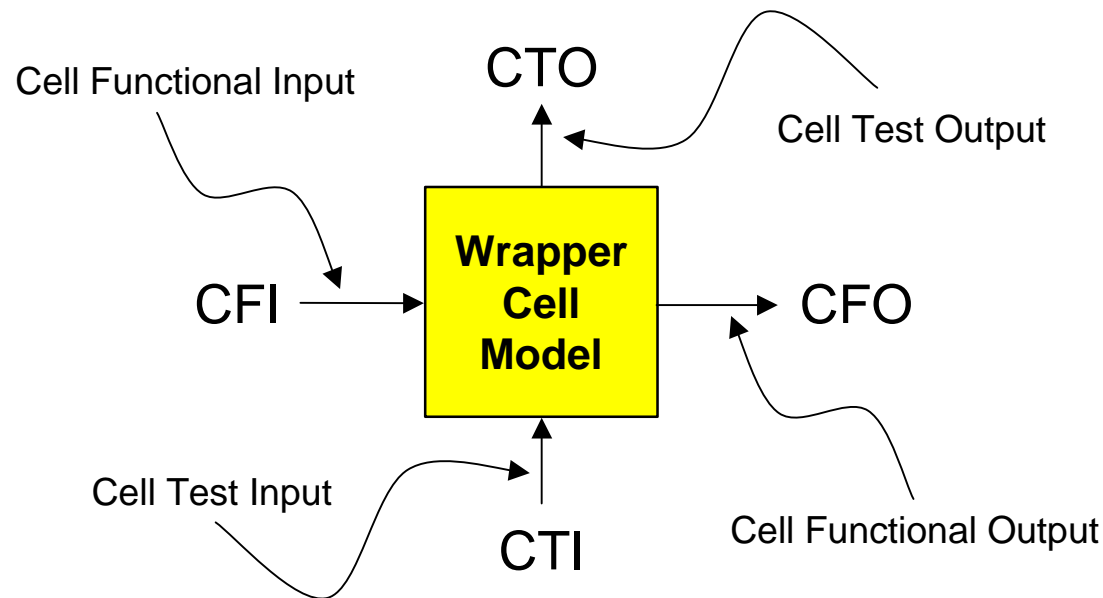
P1500 Wrapper Boundary Cells



- ❑ Wrapper Boundary Cells are required on all functional core terminals
- ❑ Wrapper Boundary Cells are not required on Test terminals or “Special Case” terminals, such as analog.

P1500 Wrapper Boundary Cells

Overview of Cell Modes



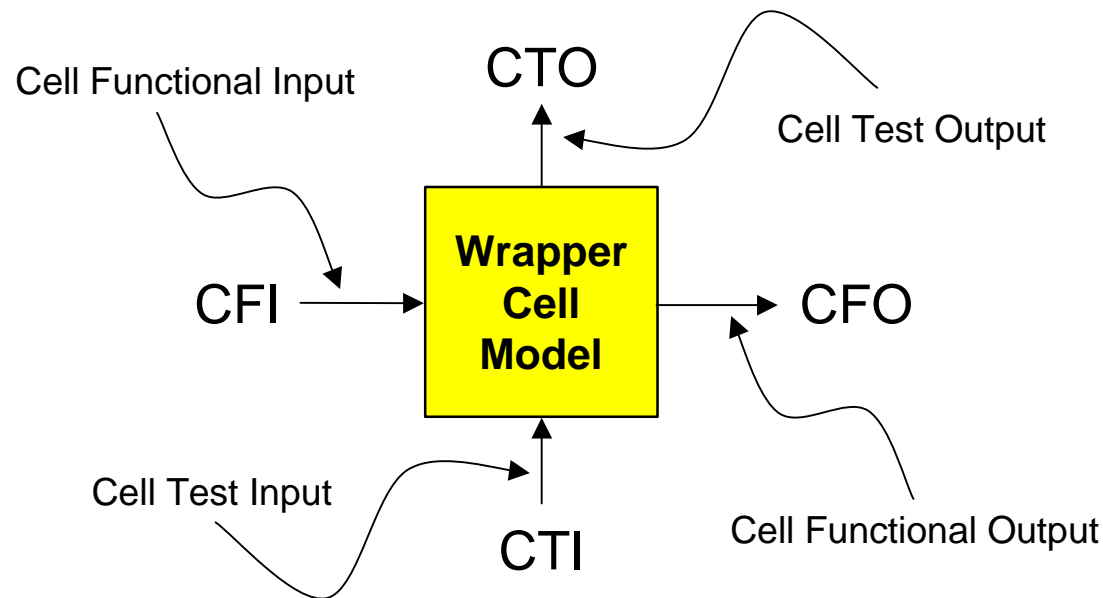
❑ Cell Modes

- ✓ **Normal:** No Effect, core functions normally
- ✓ **Inward Facing:** Affects the core, test is directed towards core
- ✓ **Outward Facing:** Affects the core, test is directed outward from core
- ✓ **Safe:** Affects the core & ensures wrapper does not damage core or system (a recommended mode)

Note: Inward and Outward Facing Test Modes Mirror one another

P1500 Wrapper Boundary Cells

Overview of Cell Events



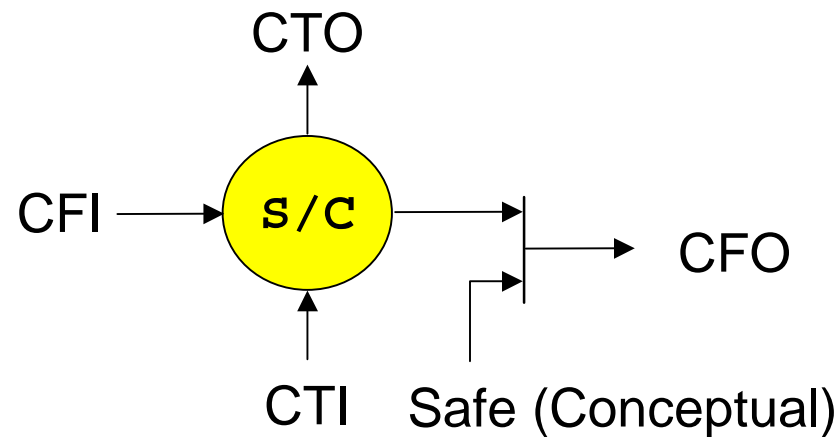
❑ Cell Events

- ✓ **Shift**: Move data through shift path
- ✓ **Capture**: Sample data
- ✓ **Apply**: Moment when test data becomes active and effective
- ✓ **Update**: 1149.1-type Update
- ✓ **Transfer**: Move data from Update element to Shift path

P1500 Wrapper Boundary Cells

Overview of Cell Types

Simple Wrapper Cell Example



❑ Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

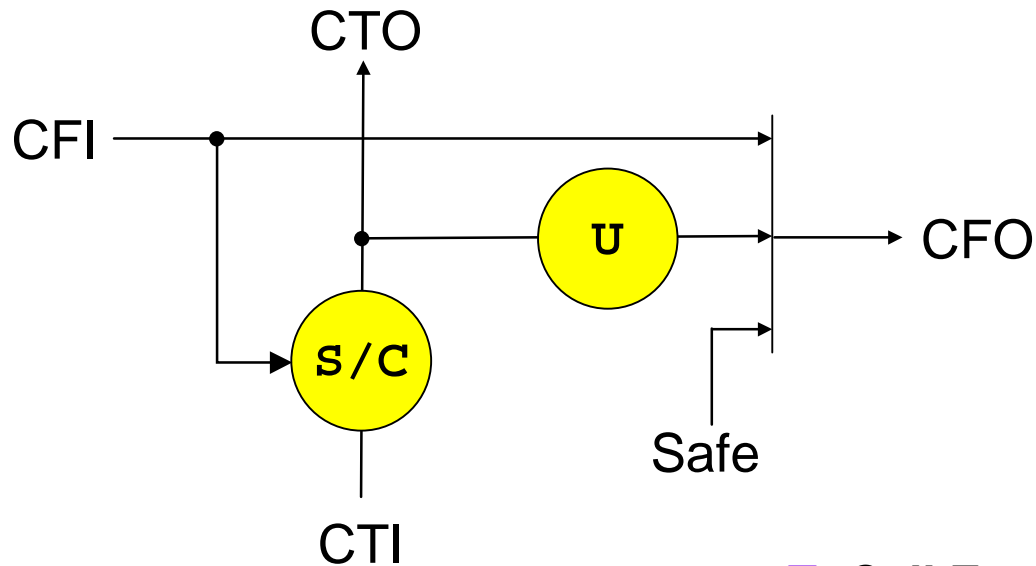
❑ Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply

P1500 Wrapper Boundary Cells

Overview of Cell Types

1149.1 Type Cell Example



❑ Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

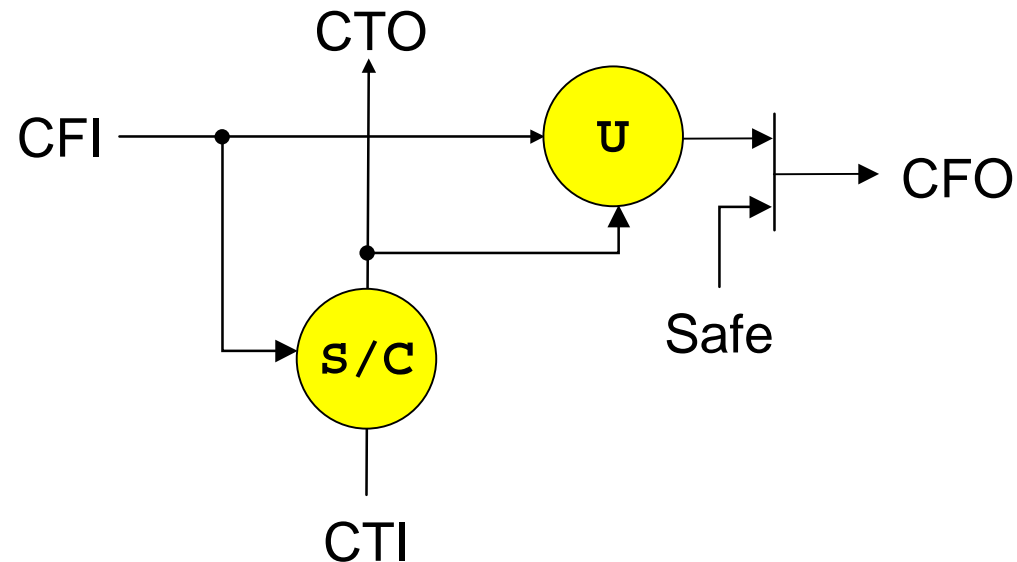
❑ Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update

P1500 Wrapper Boundary Cells

Overview of Cell Types

Cell Example with Shared Update



❑ Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

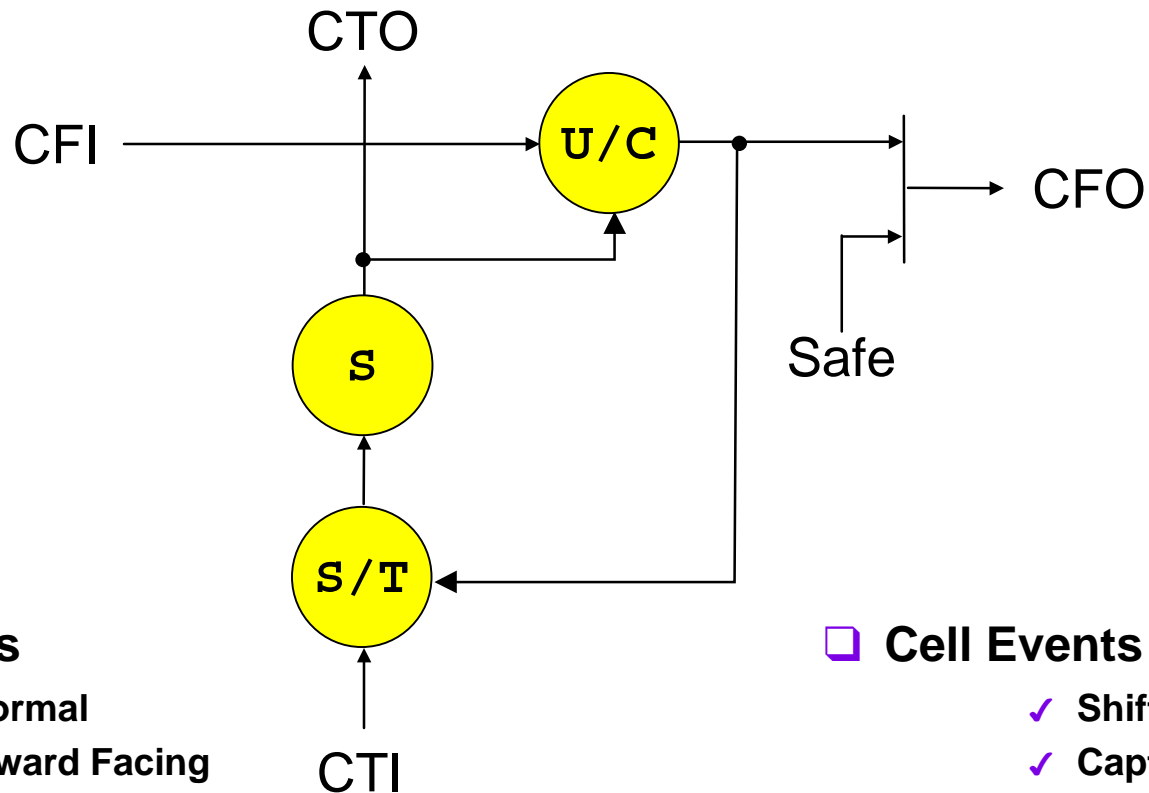
❑ Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update

P1500 Wrapper Boundary Cells

Overview of Cell Types

Cell Example Displaying all Events



❑ Cell Modes

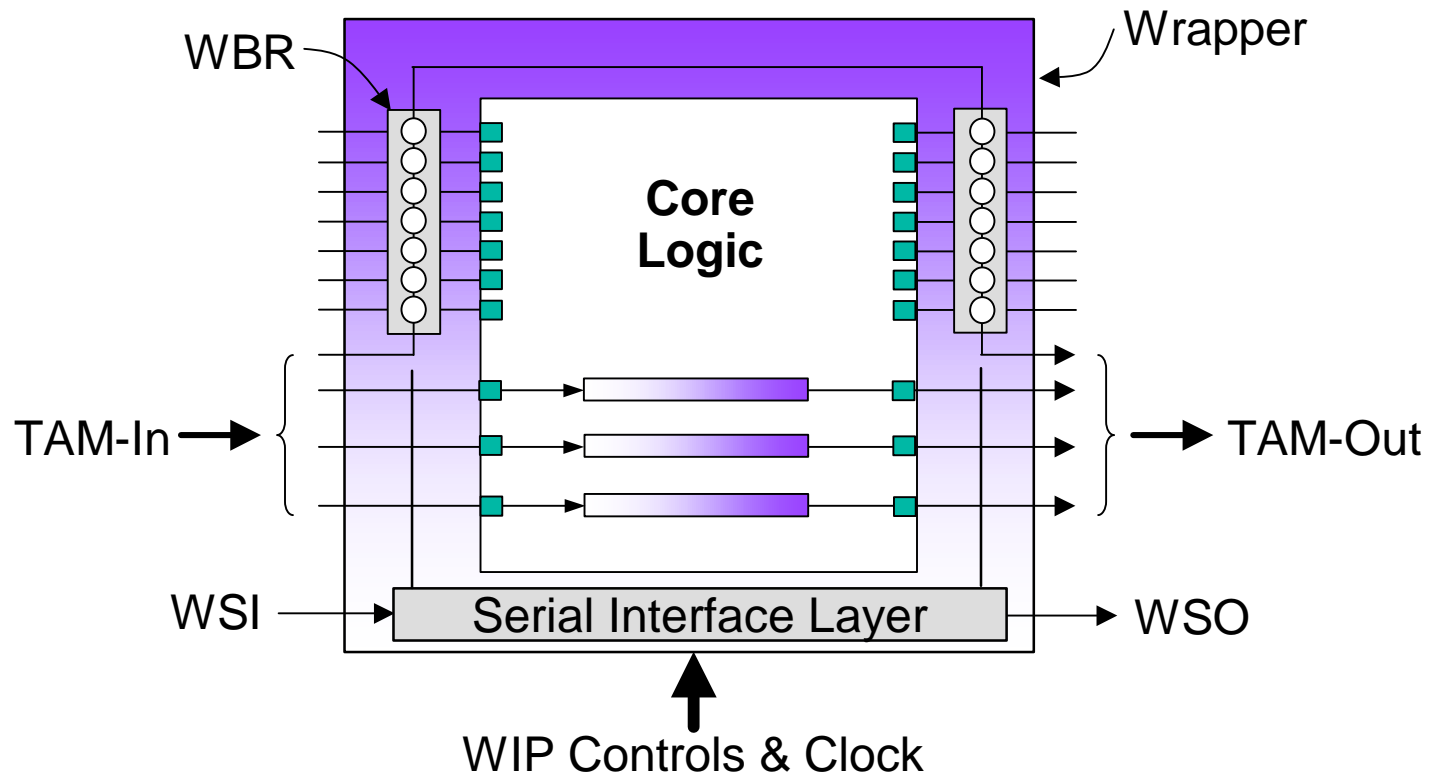
- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

❑ Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update
- ✓ Transfer

P1500 Architecture

Wrapper Example with a Parallel TAM Interface



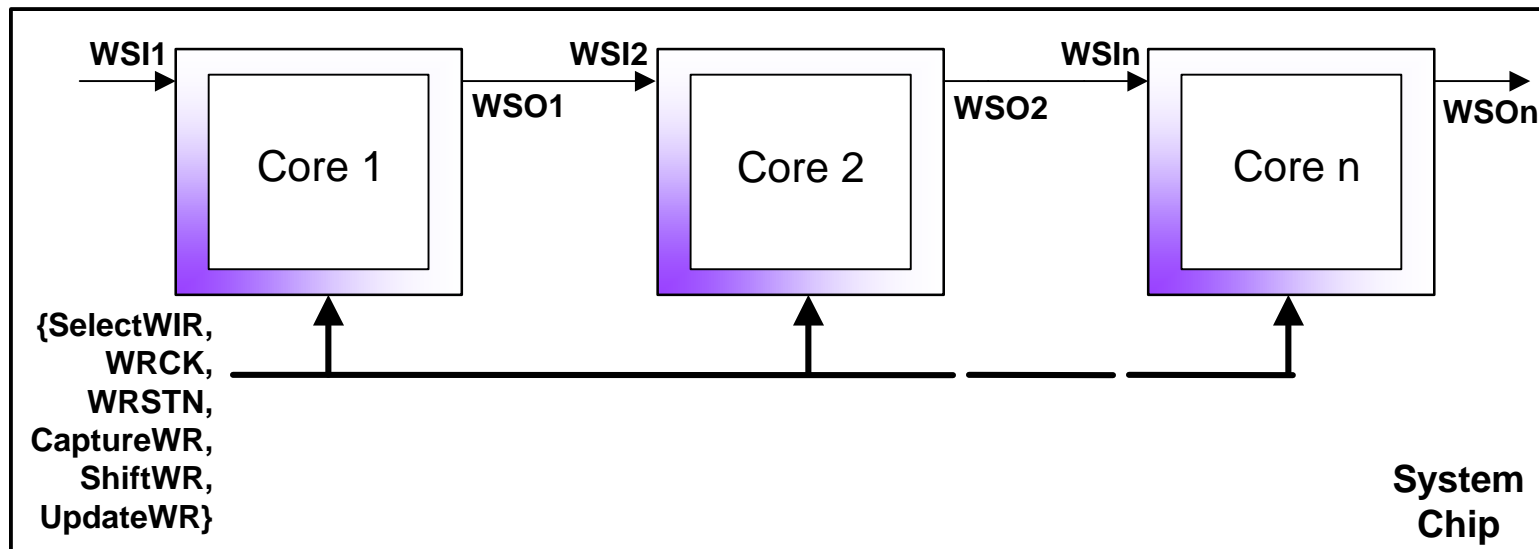
- ❑ Core internal scan paths & WBR are connected in parallel to TAM by a “Core Test” instruction
- ❑ Today, many flavors of “TAMs” & TAM “Interfaces” exist

P1500 Architecture

P1500 System Chip SIL Connections

P1500 Architecture

SoC SIL Connection Examples

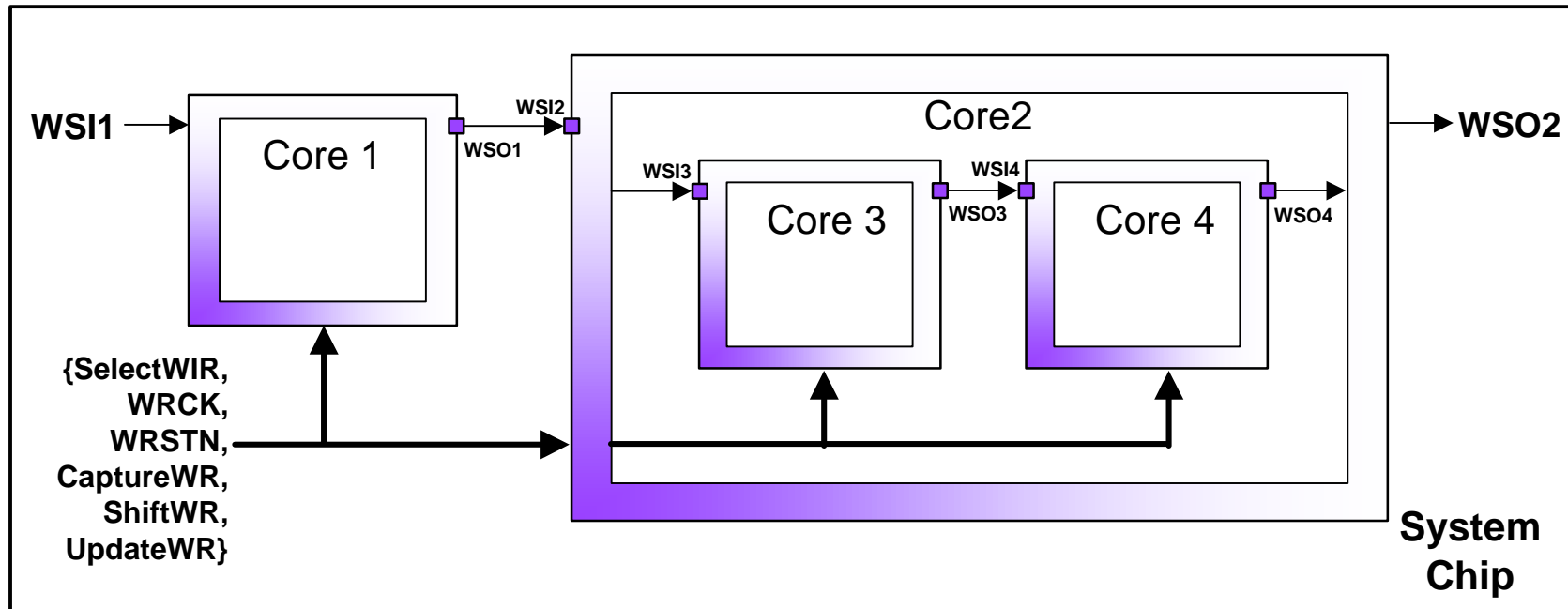


Serial connection of SILs:

- SelectWIR must be common to all cores
- Recommended that other WIP signals

P1500 Architecture

SoC SIL Connection Examples (continued)

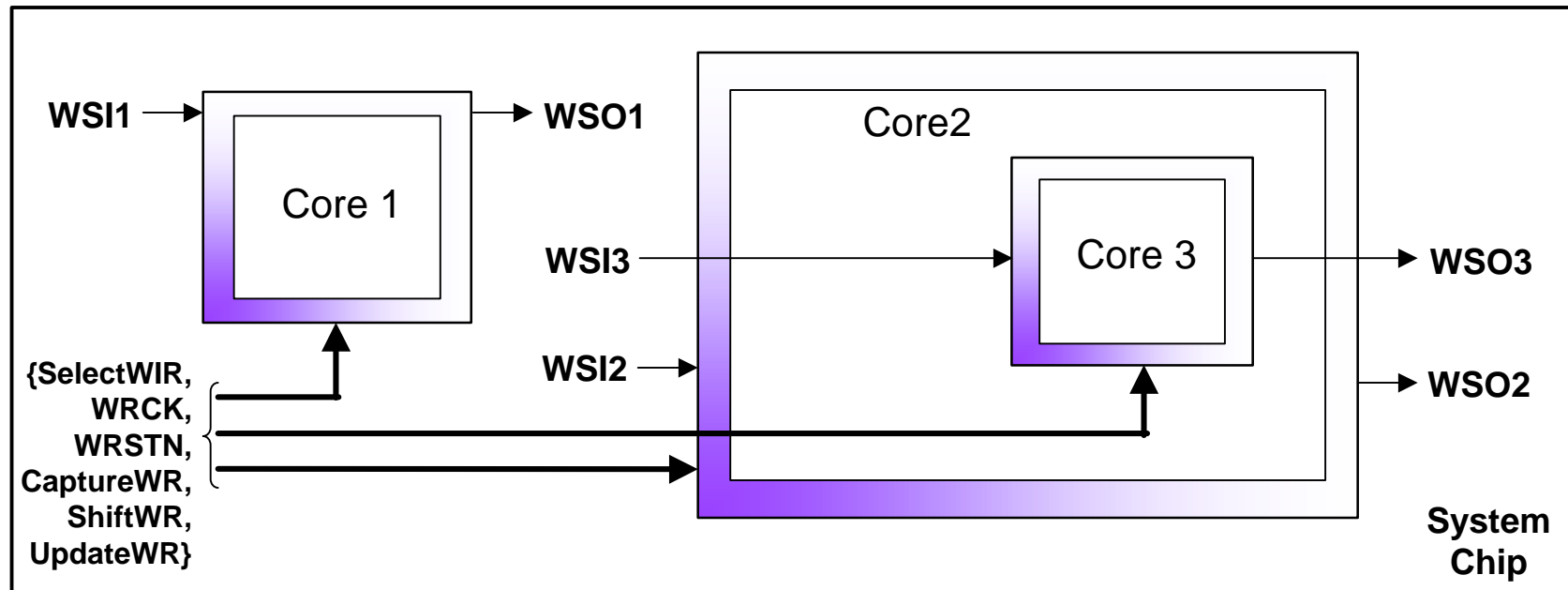


❑ Serial connection of SILs, Core 2 has child cores

- SelectWIR must be common to all cores
- Recommended that other WIP signals
- Many variations of SIL selection with Core2-Core3-Core4
 - ✓ Multiple-bit Bypass Register may be seen through Core2's SIL

P1500 Architecture

SoC SIL Connection Examples (continued)



❑ Multiple / parallel SILs within SoC

- Multiple WIP “busses” within System Chip
- Example where WIPs can be controlled separately via chip-level IEEE 1149.1 TAP

P1500 Instructions

P1500 Instructions

P1500 Instructions

Summary

- **Wrapper External Test (WEXTEST) - Mandatory Instruction**

- ✓ To operate the wrapper to allow for external testing.

- **Wrapper Bypass (WBYPASS) - Mandatory Instruction**

- ✓ To allow functional operation of the core through the wrapper

- **Wrapper Clamp (WCLAMP) – Optional Instruction**

- **Wrapper Preload (WPRELOAD) - Optional Instruction**

- ✓ To allow setup for test

- **Wrapper Safe State (SAFESTATE) - Optional Instruction**

- ✓ To operate the wrapper such that it provides a safe mode for the core and if needed, the logic adjacent to the core (from the outputs of the core).

- **Core Test (CORETEST) – Mandatory Instruction**

- ✓ To operate the wrapper (and TAM) to allow for internal testing or debug.

- **Wrapper Serial Core Test (WSCORETEST) - Optional Instruction**

- **Serial Core Test (SCORETEST) - Optional Instruction**

- ✓ To operate the wrapper to allow for debug or serial test.

CTAG Update

Status Since VTS 2001

- ❑ **Wrapper Serial Interface Layer (SIL) has been stable**
 - **On-going discussions to make WBR Plug-n-Play with WIP and WIR/Bypass**
 - ✓ WBR behavior when operated through WIP
 - ✓ Permission for auxiliary clock(s) to support shared shift cells

- ❑ **Wrapper Parallel Interface Layer (PIL) being specified**
 - **PIL addresses various Wrapper TAM interface types**
 - **Reviewing earlier TAM discussions and working toward a specification**

- ❑ **Key focus is to complete CTAG doc sections and review**
 - **Tiger teams have updated and revised their sections for D0.4 Draft**
 - ✓ WIR Tiger team, sections 3, 4 and 7
 - ✓ Instruction Tiger Team, section 5
 - ✓ WBR Tiger Team, section 6