

Unapproved IEEE P1500 Working Document



***Preliminary Outline of the IEEE
P1500 Scaleable Architecture for
Testing Embedded Cores***

Presented on behalf of the CTAG Team by

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(Excerpts from ITC99)

Presentation Outline

Introduction

- Active Task Force Members
- Task Force Mission, Scope and Current Status

Overview of Proposed Architecture

- System Chip with P1500 Cores

Core Test Requirements

P1500 Architecture Components

- Core Test Wrapper Components
- P1500 Protocol and Behavior
- Look at some examples

Agreed To Motions

Recent Discussion Items

Summary & Future Task Force Activities

P1500 Architecture Task Force

Summary of Task Force Mission and Scope

Goals of IEEE P1500

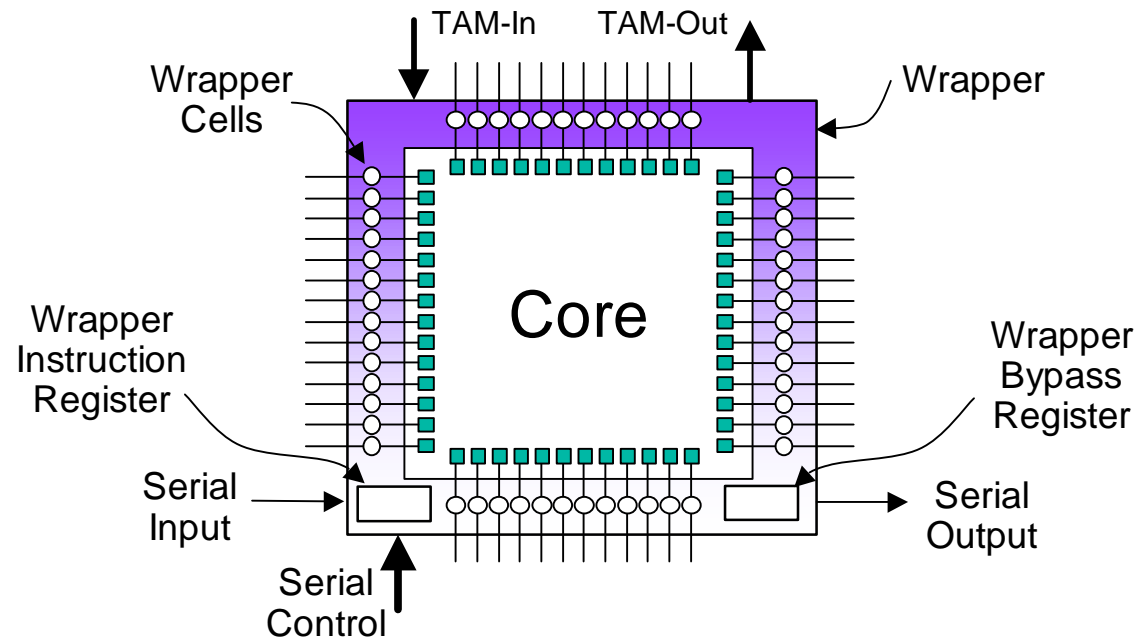
Standardize a Core Test Architecture which:

1. Defines a core test interface between an embedded core and the system chip.
2. Facilitate test reuse for embedded cores through core access and isolation mechanisms, and provide testability for system chip interconnect and logic.
3. Facilitates core test interoperability, with plug-and-play protocols, in order to improve the efficiency of test between core providers and core users.

Scope of IEEE P1500

- ✓ Standardize *core* test mechanisms, for core access and isolation, including protocols and test mode control.
- ✗ *System Chip* test access mechanism is defined by the system chip integrator.
- ✗ The *core test method* is defined by the core provider – P1500 supports, and enables, various different methods (e.g., scan, BIST, I_{ddq} , etc.).

P1500 Architecture Components



□ A P1500 wrapper contains the following:

- A Wrapper Instruction Register for providing wrapper mode control
- Wrapper Cells to provide test functions at the core terminals
- An optional Bypass register for a single bit scan bypass through the wrapper
- A serial interface for providing initialization and communication to the Wrapper Instruction Register, Wrapper Cells, and Bypass register

P1500 Wrapper Instruction Register

Proposed Required Instructions

Normal

- Wrapper cells allow normal core inputs/outputs to pass through the wrapper for normal system operation

Core Test 1–N

- Wrapper cells are configured to disable the core's normal mode & connected to TAM and/or wrapper serial input/output for core test
- Sources & sinks, 1-N, and core test methods are user defined

Serial External Test

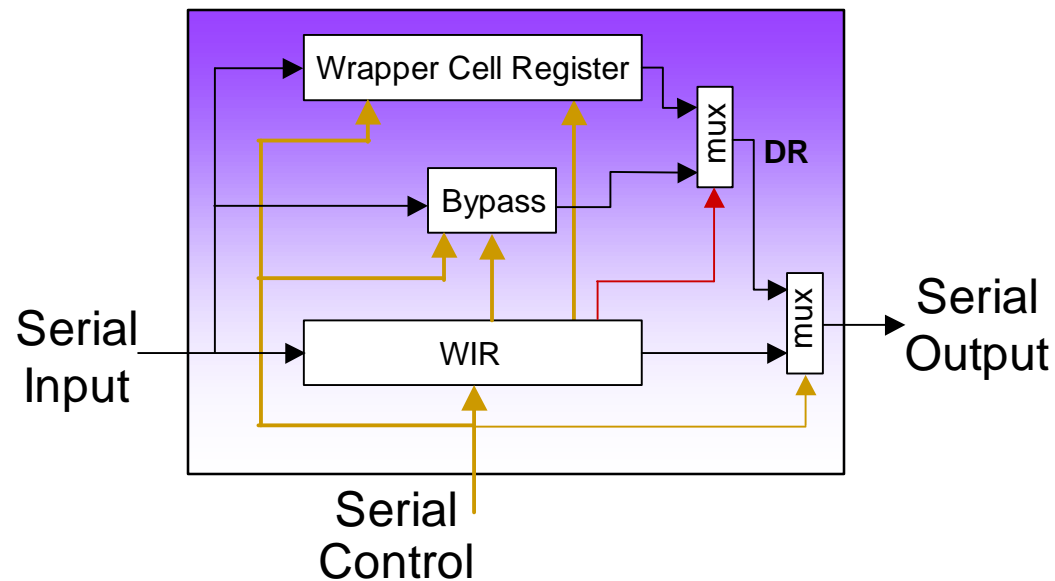
- Wrapper cells are configured to disable the core's normal mode, and are connected serially between the wrapper serial input/output

Isolation

- Wrapper cells are configured to disable the core's normal mode, and enable setting of appropriate core inputs or outputs to constrained and/or disabled values for core isolation

P1500 Wrapper Registers

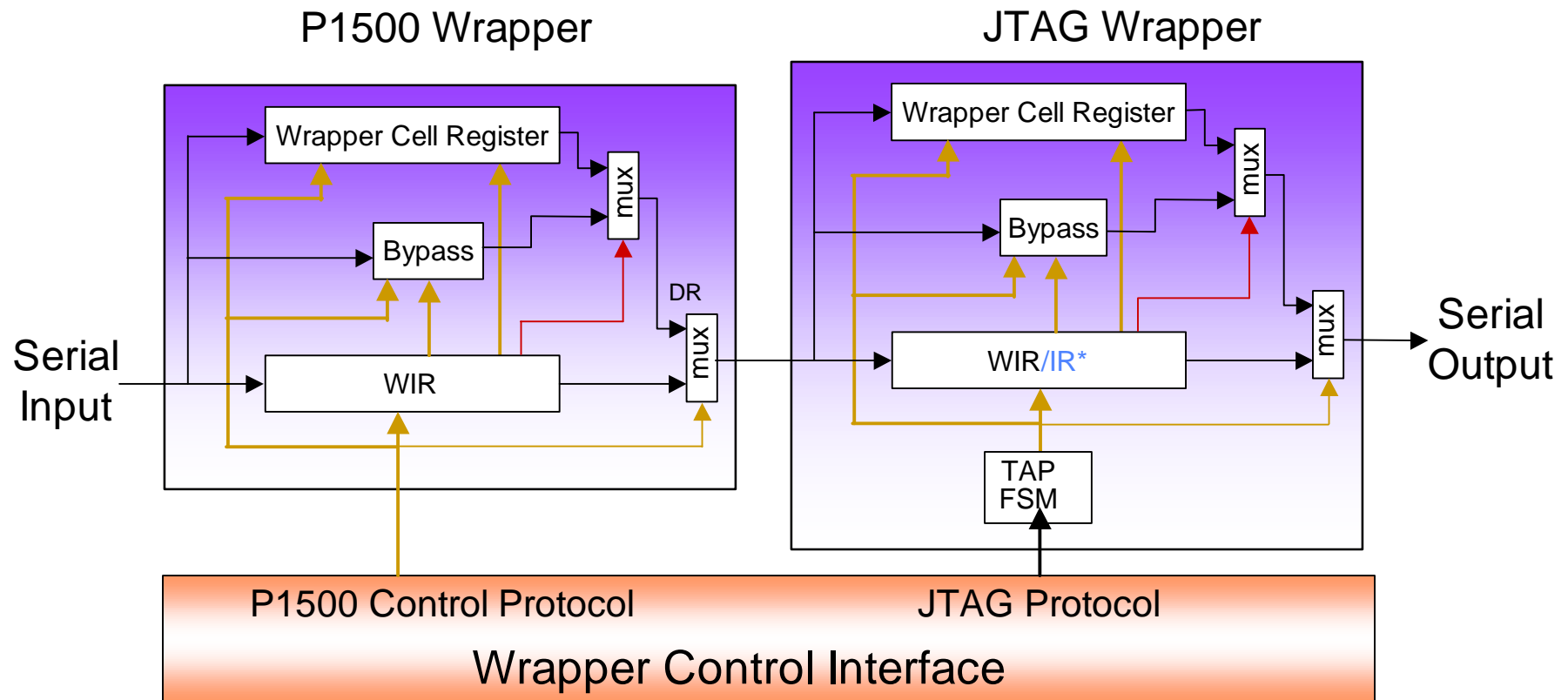
Standard Serial Scan Path Configuration



- ❑ **Serial Control lines enable & perform scan, and select between:**
 - Wrapper Instruction Register (WIR)
 - Or other Data Registers (DRs), e.g. Wrapper Cell Register, Bypass, etc.
- ❑ **Updated WIR then selects between DRs**
- ❑ **Core Test 1-N instructions permit TAM connection & configuration of Wrapper DRs, or internal core registers, to be *used defined* !**

P1500 Wrapper Connection

P1500 Wrapper with 1149.1 Wrapper

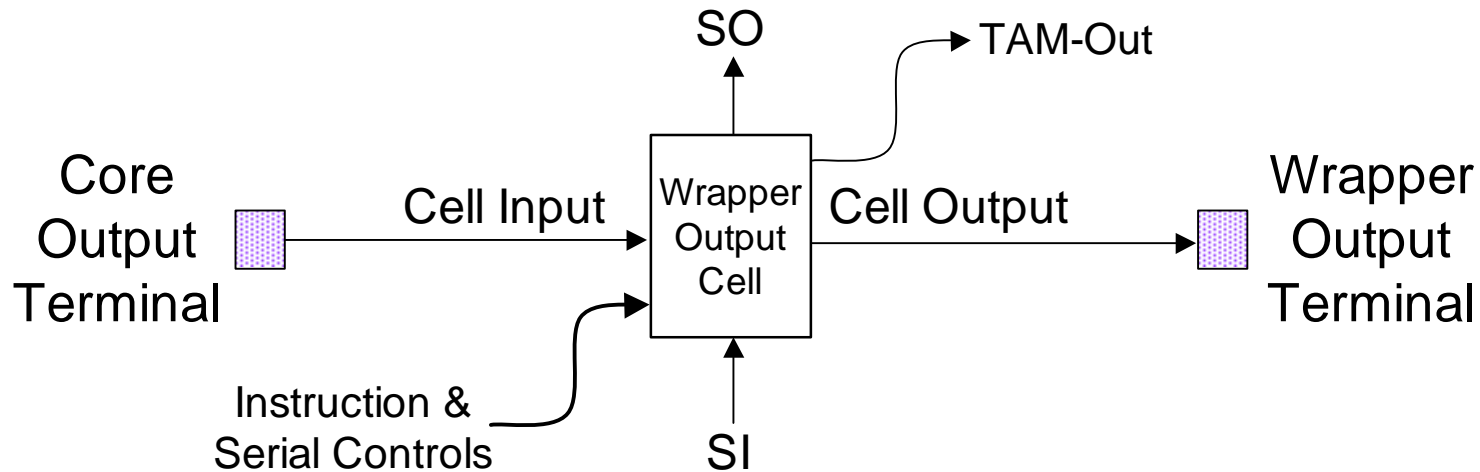


- ❑ Wrapper Control Interface is configured by system chip integrator
- ❑ P1500 & JTAG inter-operate at wrapper & serial data interfaces

* Context of recent discussion as per slide #26

P1500 Wrapper Cell Example

Dedicated Output Cell with Update Stage & TAM-Out



❑ Cell behavior in response to Wrapper Instructions

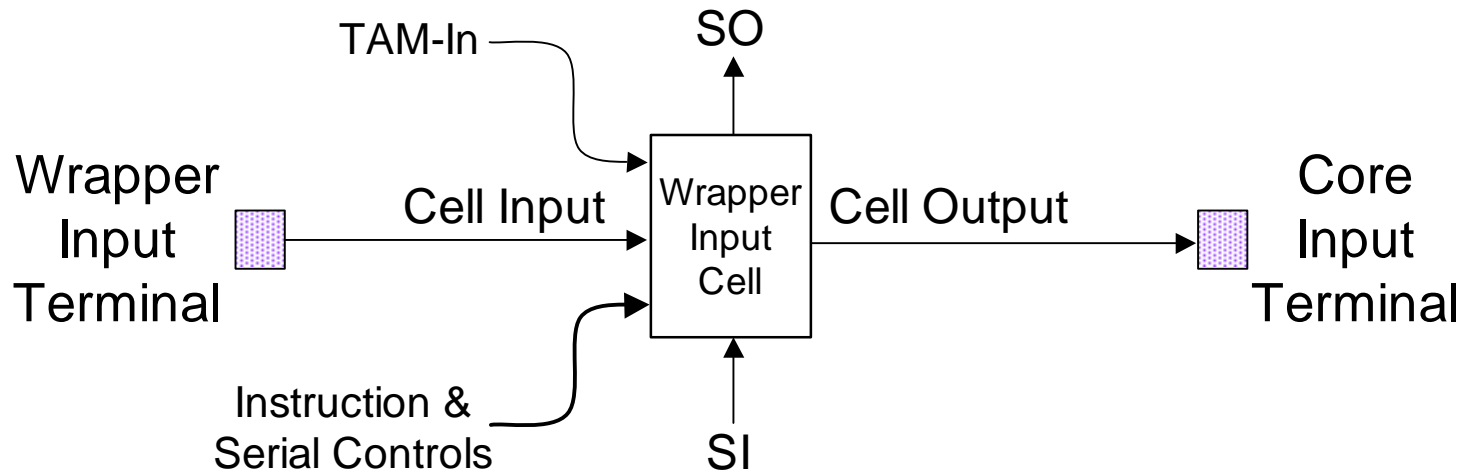
- ✓ **Normal:** Cell output connects to Cell input
- ✓ **Serial External Test:** Cell output is sourced from cell's update stage
- ✓ **Isolation:** Cell output is appropriately disabled or constrained
- ✓ **Core Test 1:** TAM-Out is sink & provides output observation for core test

❑ Cell behavior for Wrapper Scan Protocol

- 1) Captures data at cell input
- 2) Shifts data from scan input (SI) to scan output (SO)
- 3) Updates shift stage data to update stage

P1500 Wrapper Cell Example

Dedicated Input Cell with Update Stage & TAM-In



❑ Cell behavior in response to Wrapper Instructions

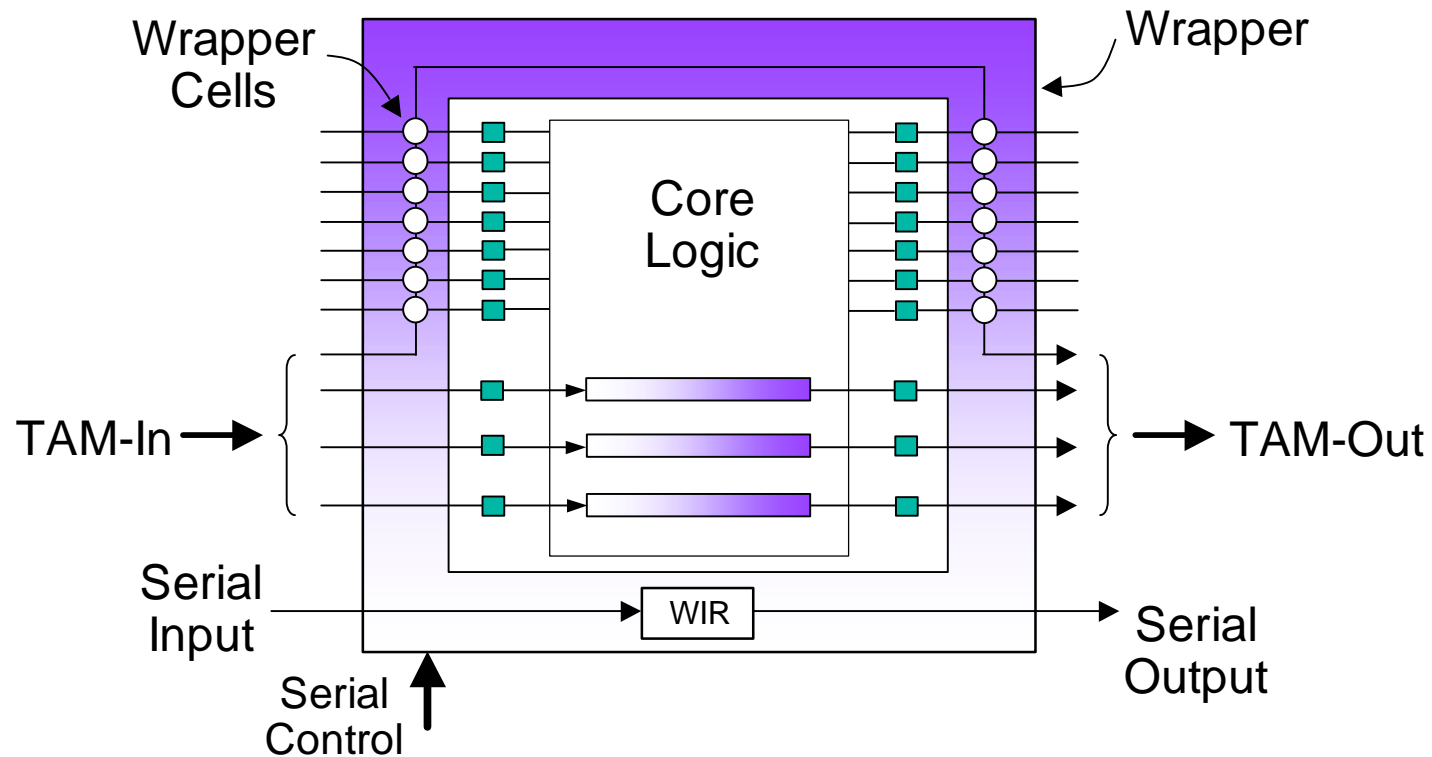
- ✓ **Normal:** Cell output connects to Cell input
- ✓ **Serial External Test:** Cell input is captured into cell's shift stage
- ✓ **Isolation:** Cell output is appropriately constrained
- ✓ **Core Test 1:** TAM-In is source & provides input control for core test

❑ Cell behavior for Wrapper Scan Protocol

- 1) Captures data at cell input
- 2) Shifts data from scan input (SI) to scan output (SO)
- 3) Updates shift stage data to update stage

P1500 TAM Connection Example

Core with Parallel Internal Scan



- ❑ **Core internal scan paths & Wrapper Cell Register are connected in parallel to TAM by a Core Test instruction**
- ❑ **Many other TAM connections and configurations are possible !**