

***Unapproved IEEE P1500 Working Document***

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***Overview of Proposed IEEE P1500  
Scaleable Architecture for Testing  
Embedded Cores***

**Presented on behalf of the CTAG Team by**

**Mike Ricchetti**

**March 13, at DATE 2001**

# ***Presentation Outline***

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## **□ Introduction**

- **CTAG Task Force Mission and Scope**
- **CTAG Members, Organization & Development Phases**

## **□ P1500 Architecture**

- **System Chip with P1500 Wrapped Cores**
- **P1500 Architecture Components**
- **Wrapper Serial Interface Layer (SIL) Architecture**
- **Wrapper Interface Port (WIP)**
- **Wrapper Boundary Register (WBR) Cells**
- **Wrapper Example with a Parallel TAM Interface**

## **□ P1500 Wrapper Instructions**

## **□ Status update since ITC 2000**

# ***P1500 Architecture Task Force***

## ***Summary of Task Force Mission and Scope***

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### **Goals of IEEE P1500**

Standardize a Core Test Architecture which:

1. Defines a core test interface between an embedded core and the system chip.
2. Facilitate test reuse for embedded cores through core access and isolation mechanisms, and provide testability for system chip interconnect and logic.
3. Facilitates core test interoperability, with plug-and-play protocols, in order to improve the efficiency of test between core providers and core users.

### **Scope of IEEE P1500**

- ✓ Standardize *core* test mechanisms, for core access and isolation, including protocols and test mode control.
- ✗ *System Chip* test access mechanism is defined by the system chip integrator.
- ✗ The *core test method* is defined by the core provider – P1500 supports, and enables, various different methods (e.g., scan, BIST,  $I_{ddq}$ , etc.).

# ***P1500 Architecture Task Force***

## ***Active Task Force Members***

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**Lee Whetsel (Task Force Chair) - Texas Instruments**

**Saman Adham - LogicVision**

**Louis Basto - Analog Devices**

**Debashis Bhattacharya - TI**

**Dwayne Burek - LogicVision**

**Bulent Dervisoglu - Cadence**

**C.J. Clark - Intellitech**

**★ Jason Doege - Inovys**

**Grady Giles - AMD**

**Sanjay Gupta - SiberCore**

**Alan Hales - Texas Instruments**

**Andy Halliday - TriMedia Technologies**

**Douglas Kay - Cisco Systems**

**Erik Jan Marinissen - Philips**

**★ Teresa McLaurin - ARM**

**Fidel Muradali - Agilent Technologies**

**Srinivas Patil - Mentor Graphics**

**Rochit Rajsuman - Advantest**

**★ Mike Ricchetti - Intellitech**

**Paul Soong - Nortel**

**Wu Tung - Mentor Graphics**

**Jon Udell - Palmchip**

**Greg Young - Motorola**

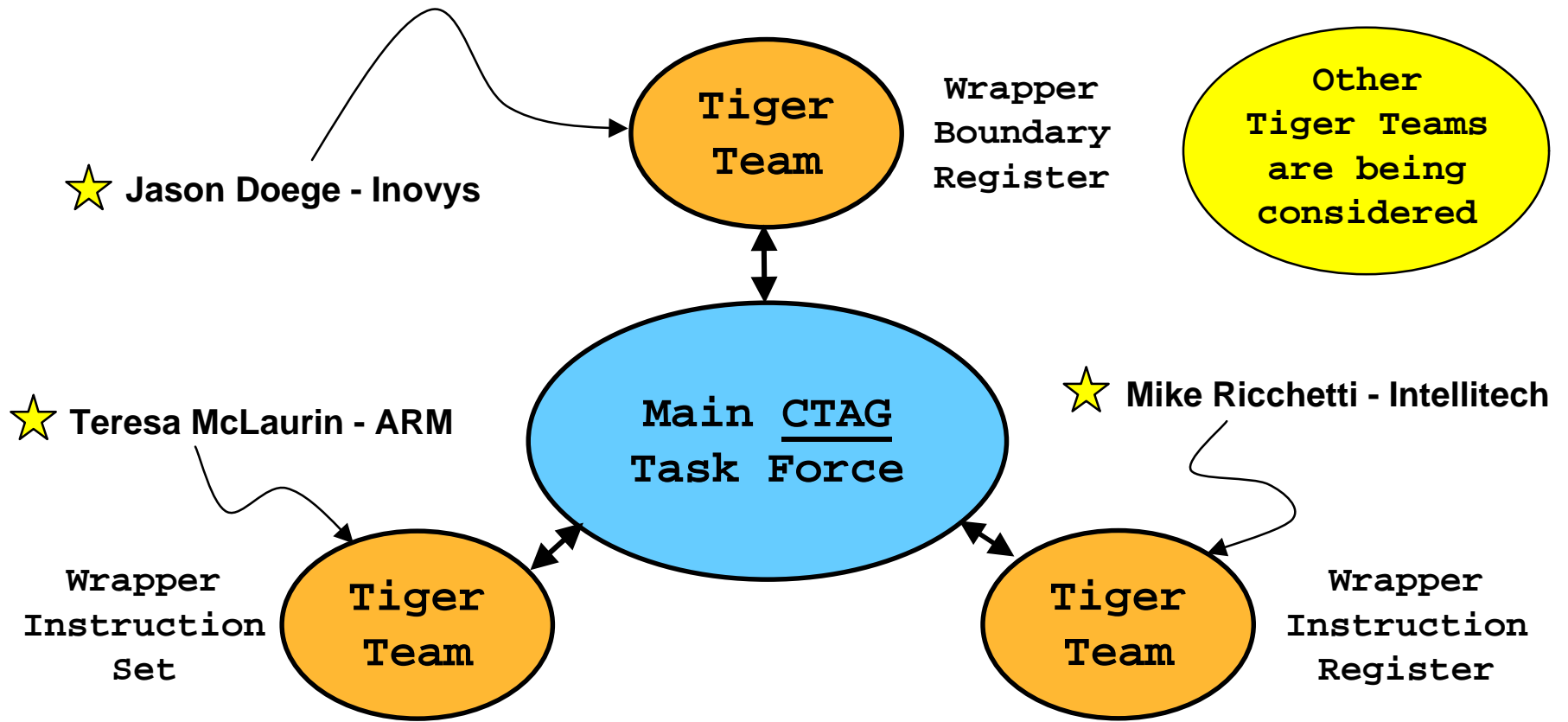
**Alex Zamfirescu - ASC**

**Yervant Zorian - LogicVision**

**★ - Tiger Team Champions**

# P1500 Architecture Task Force

## Organization of Task Force

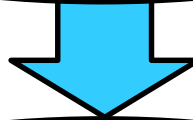


# **P1500 Architecture Task Force**

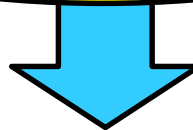
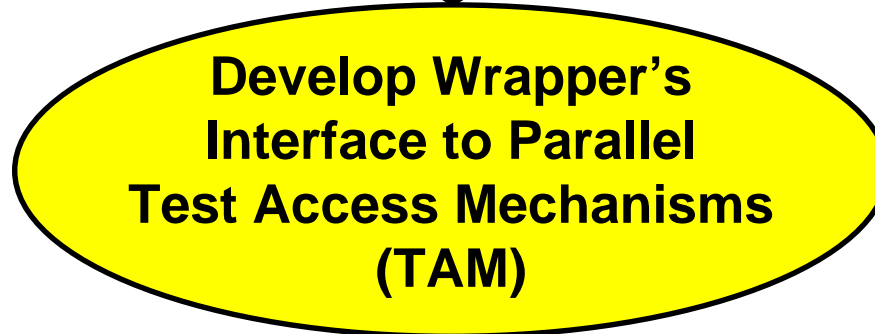
## ***Task Force Wrapper Development Phases***

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**Phase 1**



**Phase 2**



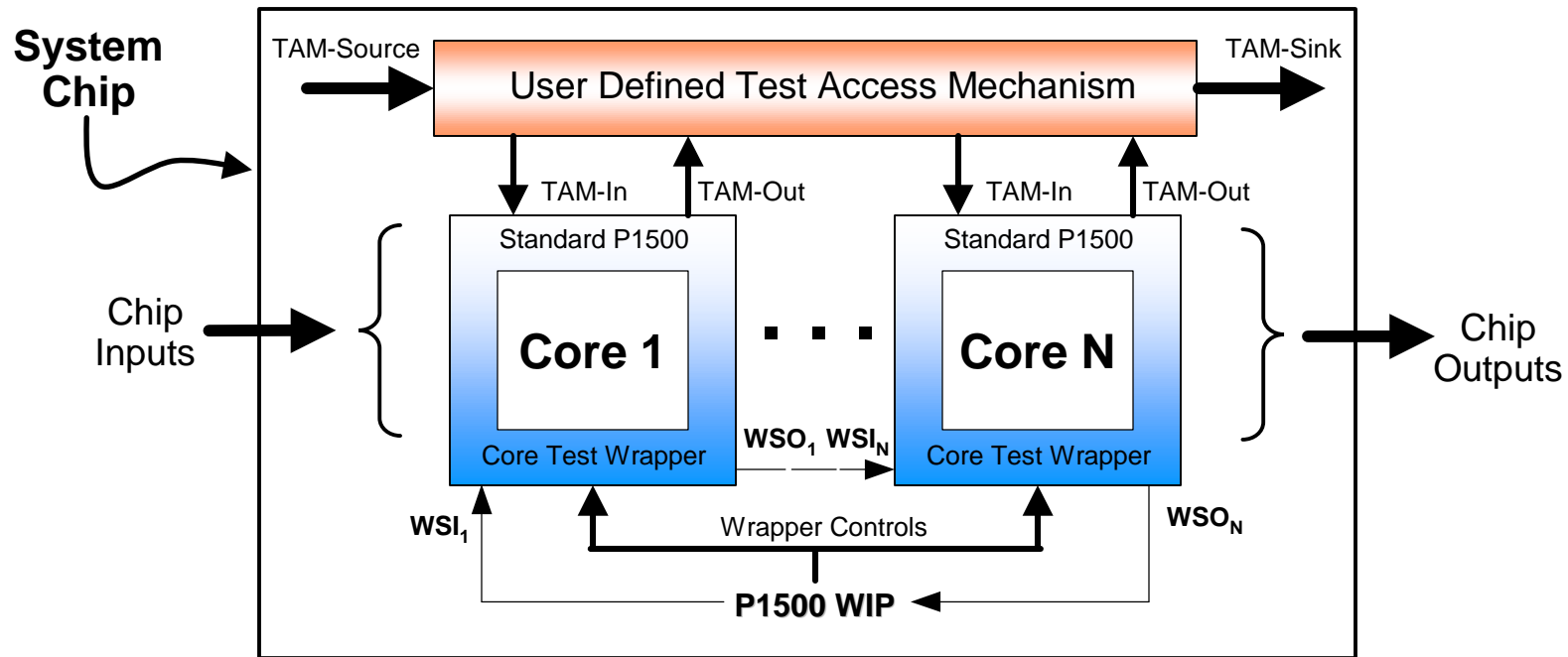
**P1500 Standard**

# ***P1500 Architecture***

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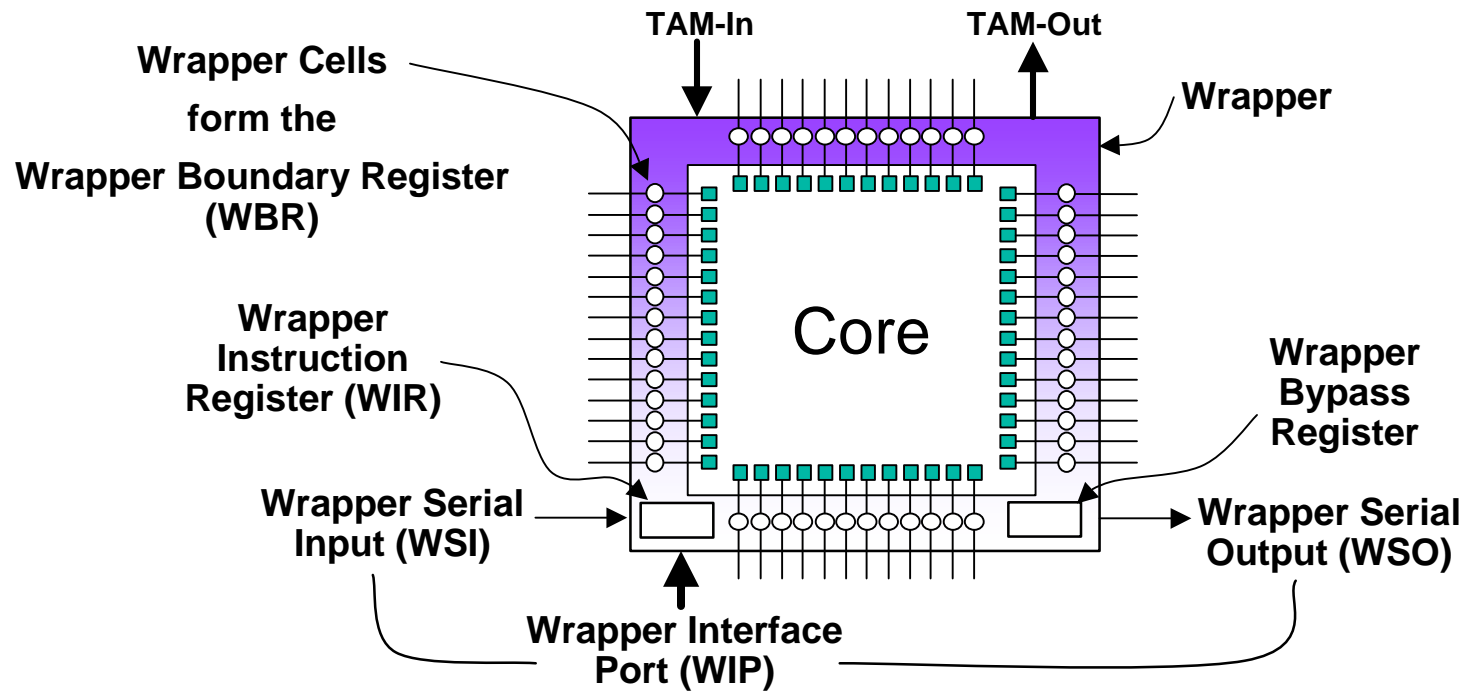
# **P1500 Architecture**

# System Chip with P1500 Wrapped Cores



- **TAM Source/Sink**
  - ✓ From chip I/O, test bus/rail/port, BIST, etc...
- **TAM In/Out**
  - ✓ 0 to n lines for parallel and/or serial test data, or test control
- **P1500 Wrapper Interface Port (WIP)**
  - ✓ From chip-level TAP Controller, chip I/O, etc...

# P1500 Architecture Components

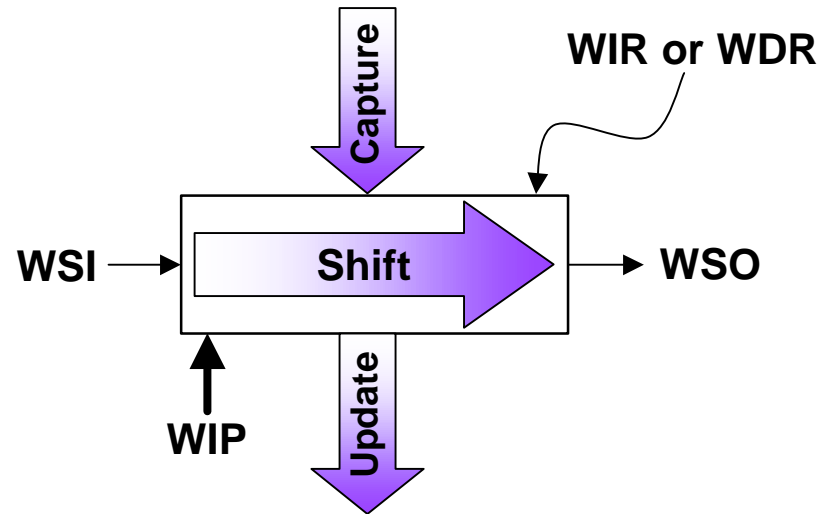


## □ A P1500 Wrapper has the following:

- A WIR for providing wrapper mode control
- Wrapper Cells to provide test functions at the core terminals
- A Bypass register for scan bypass through the wrapper
- The WIP for standard serial control (WIR, Bypass & WBR) and optionally TAM control



# P1500 Wrapper Register Behavior



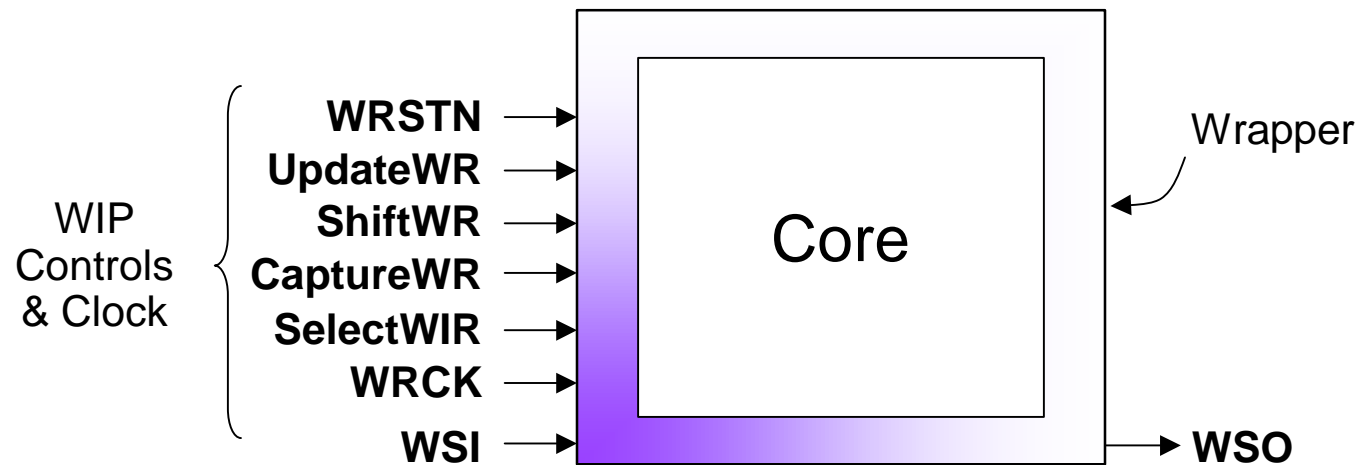
## □ P1500 Wrapper Instruction Register (WIR) and Data Registers provide:

- **Serial *Shift*** from WSI to WSO
- **Parallel *Update***
  - ✓ Updated output data held stable during shift operations from WSI to WSO
  - ✓ Required for WIR to prevent Wrapper & Core Modes from toggling during WIR shift
- **Parallel *Capture***
  - ✓ Required for WBR to provide interconnect and UDL test capability
  - ✓ Optional for WIR to provide capture of test control information, or for testing of WIR circuitry & WSI to WSO scan paths

# ***P1500 Wrapper Interface Port (WIP)***

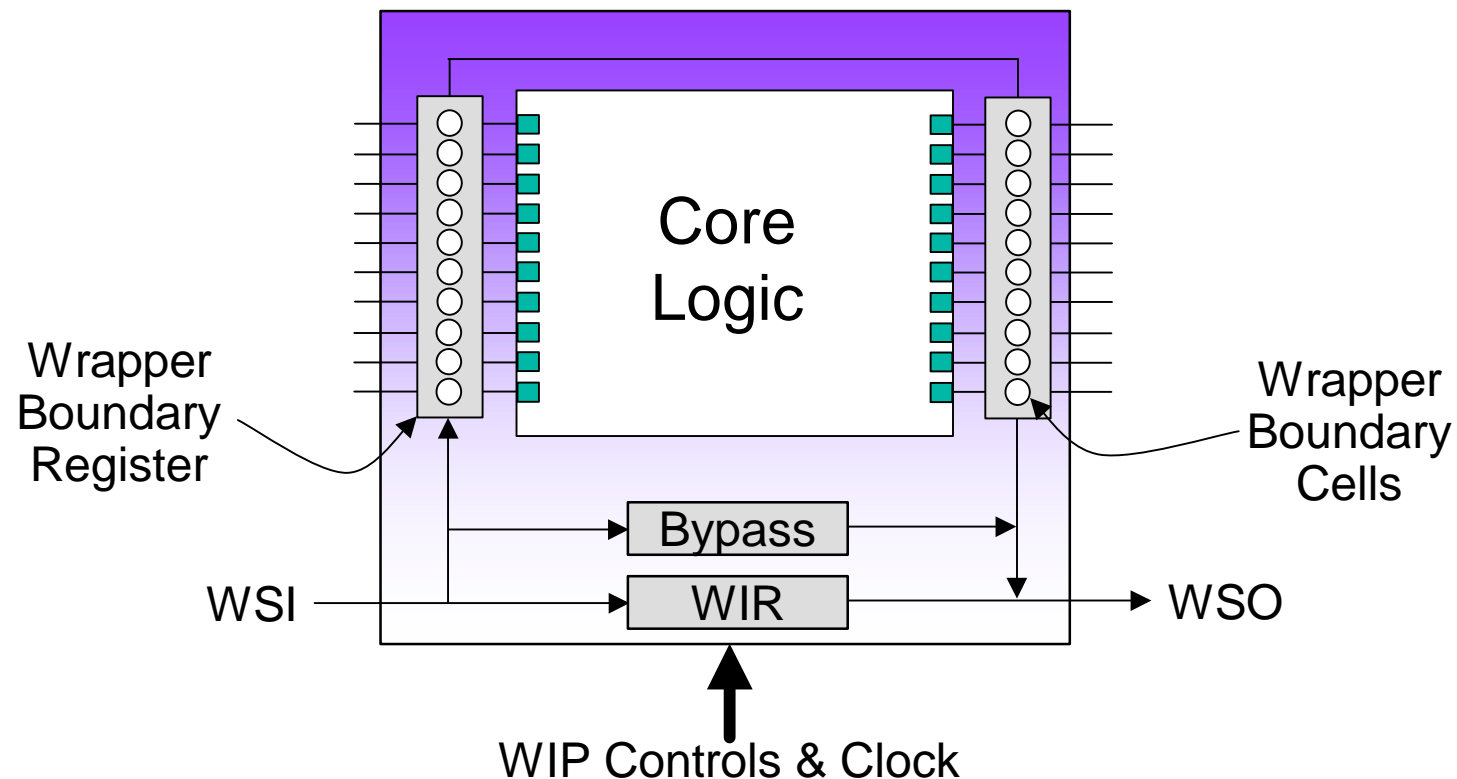
## ***WIP Signals for Accessing WIR, Bypass & WDRs***

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- ❑ **The WIP is currently defined to access the WIR and Bypass**
  - **WIP could be used for other data registers (e.g., WBR & Core Internal Scan)**
- ❑ **WIP Terminals:**
  - **WRCK is the clock used to operate registers**
  - **WRSTN is a dedicated asynchronous Wrapper Reset**
  - **SelectWIR selects whether the WIR or DR(s) is connected between WSI and WSO**
  - **UpdateWR, ShiftWR and CaptureWR are enables for register operations**
    - ✓ **May be used for gating WRCK clock internal to Wrapper**

# P1500 Wrapper Boundary Cells

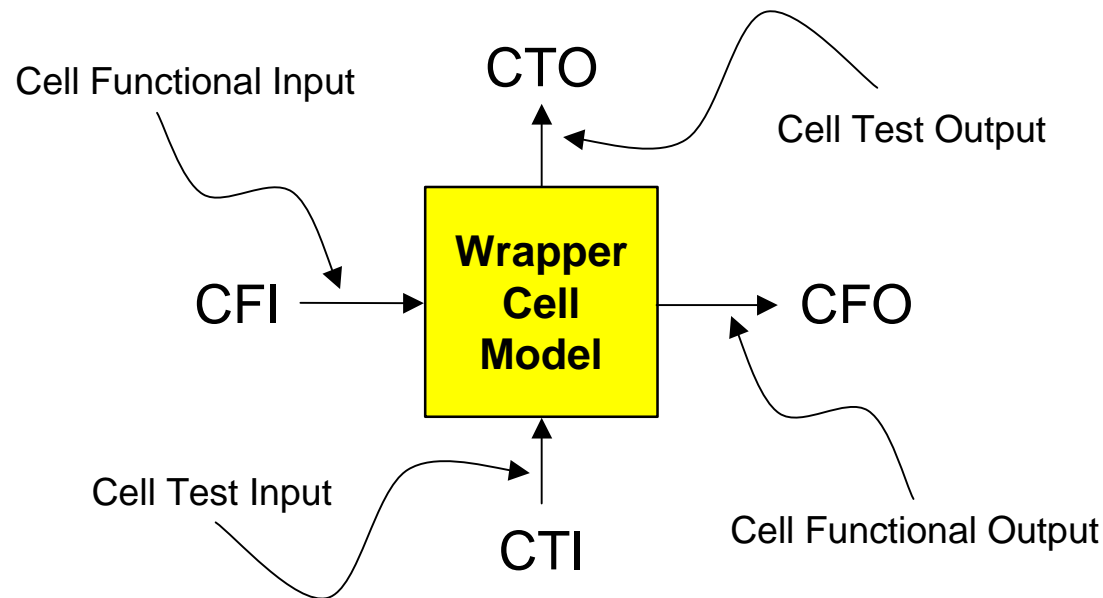


- ❑ Wrapper Boundary Cells are required on all functional core terminals
- ❑ Wrapper Boundary Cells are not required on Test terminals or “Special Case” terminals, such as analog.

# P1500 Wrapper Boundary Cells

## Overview of Cell Modes

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### ❑ Cell Modes

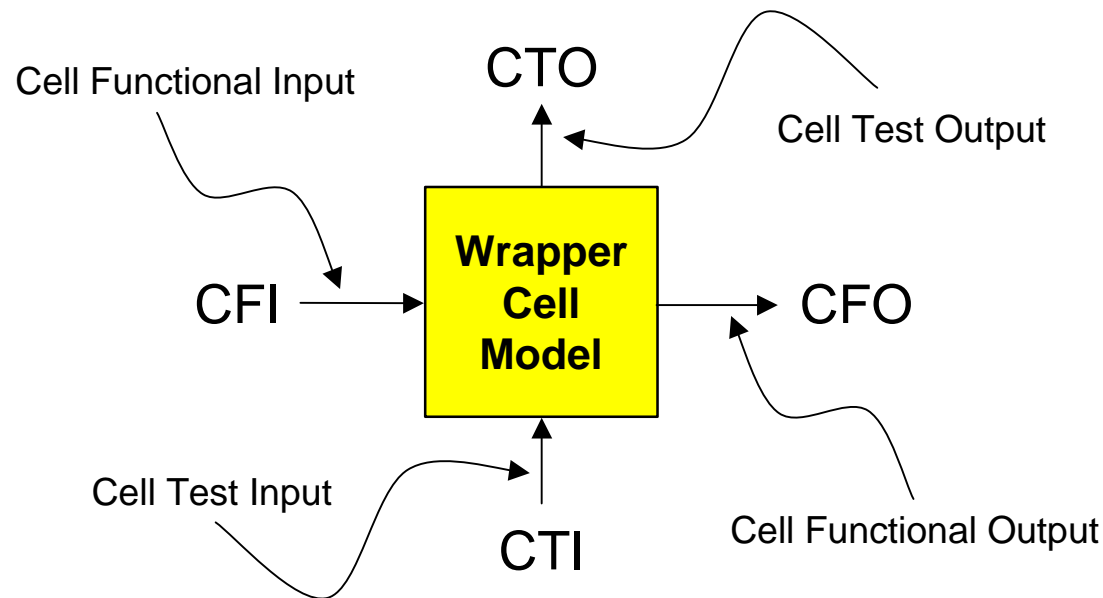
- ✓ **Normal**: No Effect, core functions normally
- ✓ **Inward Facing**: Affects the core, test is directed towards core
- ✓ **Outward Facing**: Affects the core, test is directed outward from core
- ✓ **Safe**: Affects the core & ensures wrapper does not damage core or system (a recommended mode)

Note: Inward and Outward Facing Test Modes Mirror one another

# P1500 Wrapper Boundary Cells

## Overview of Cell Events

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### □ Cell Events

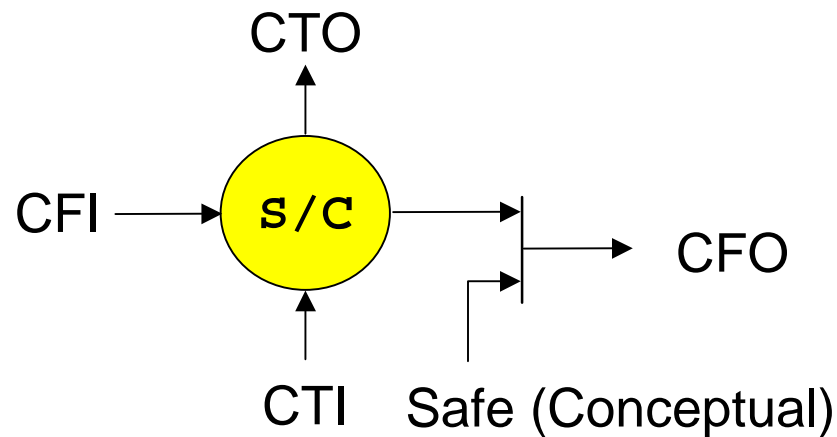
- ✓ **Shift:** Move data through shift path
- ✓ **Capture:** Sample data
- ✓ **Apply:** Moment when test data becomes active and effective
- ✓ **Update:** 1149.1-type Update
- ✓ **Transfer:** Move data from Update element to Shift path

# P1500 Wrapper Boundary Cells

## Overview of Cell Types

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### Simple Wrapper Cell Example



#### ❑ Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

#### ❑ Cell Events

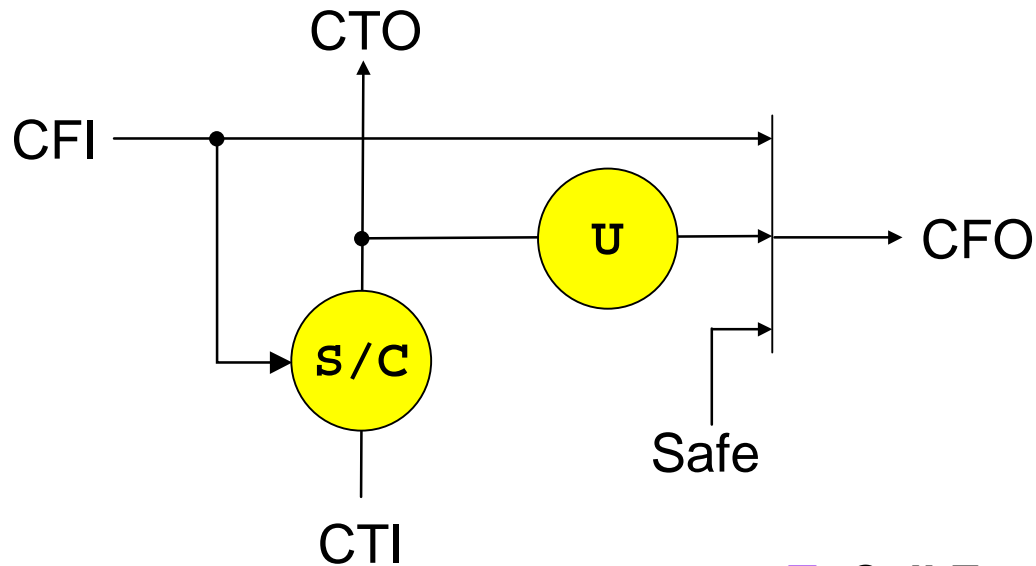
- ✓ Shift
- ✓ Capture
- ✓ Apply

# P1500 Wrapper Boundary Cells

## Overview of Cell Types

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### 1149.1 Type Cell Example



#### ❑ Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

#### ❑ Cell Events

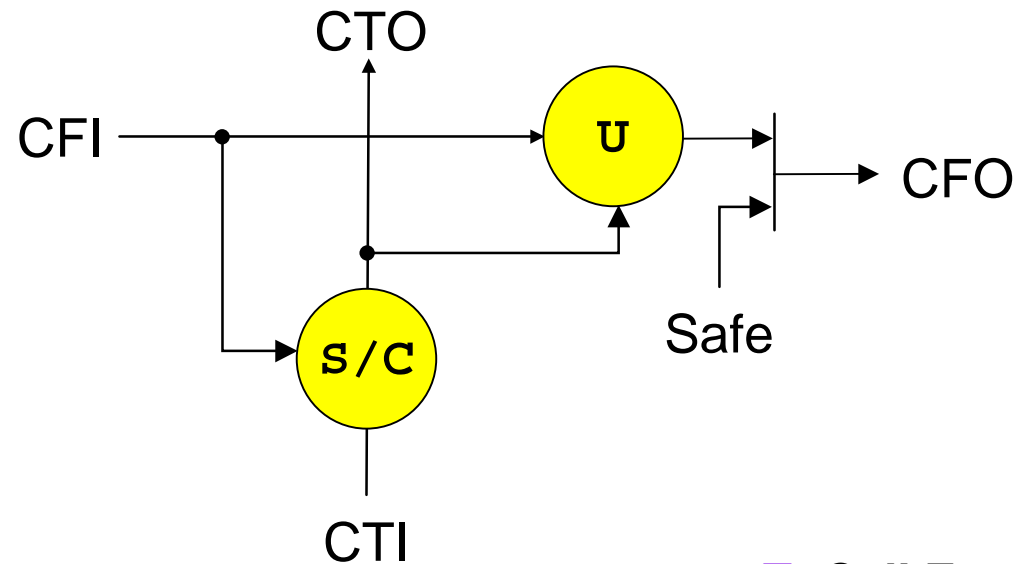
- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update

# P1500 Wrapper Boundary Cells

## Overview of Cell Types

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### Cell Example with Shared Update



#### ❑ Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

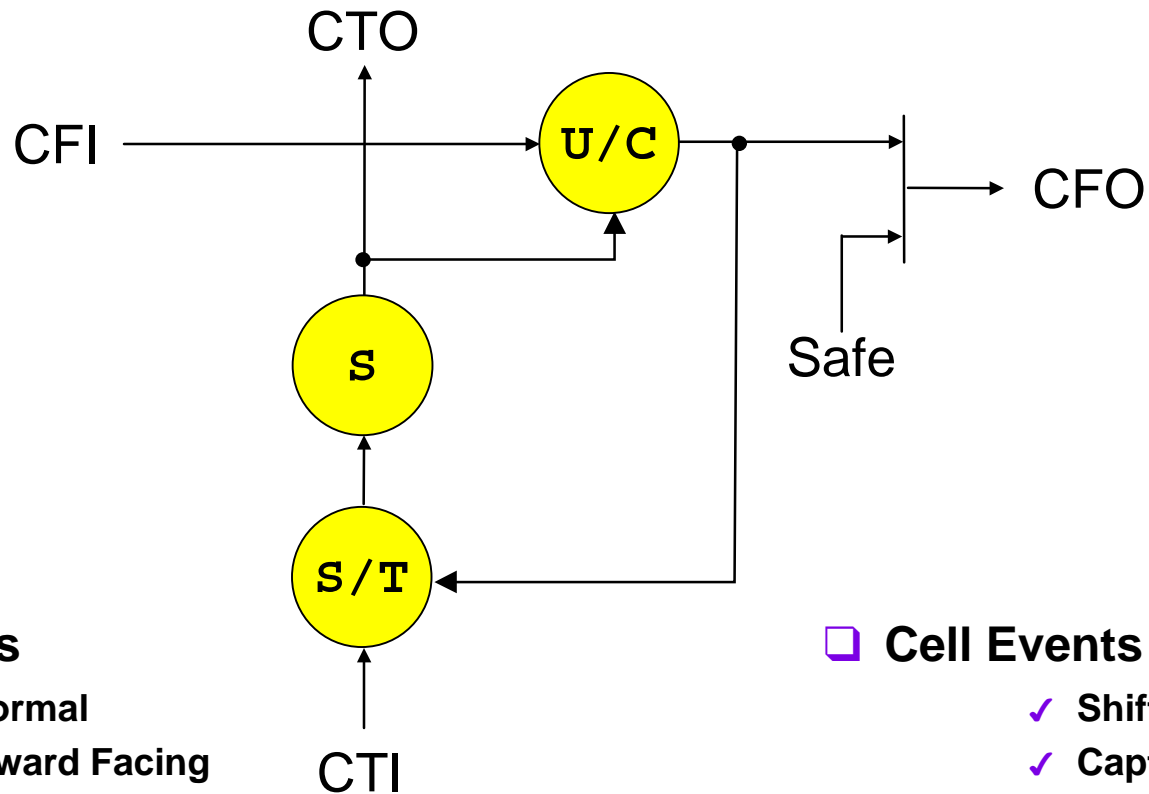
#### ❑ Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update

# P1500 Wrapper Boundary Cells

## Overview of Cell Types

### Cell Example Displaying all Events



#### Cell Modes

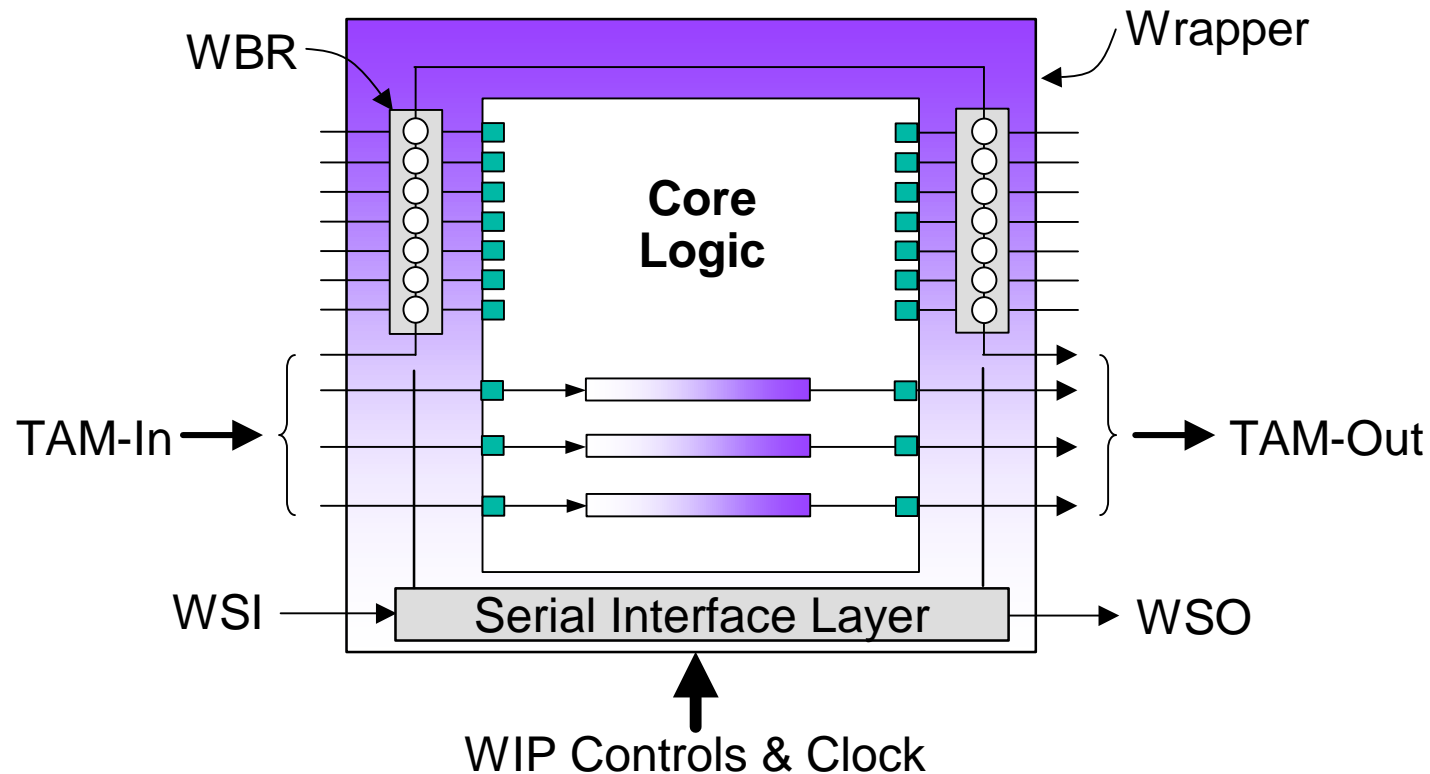
- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

#### Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update
- ✓ Transfer

# P1500 Architecture

## Wrapper Example with a Parallel TAM Interface



- ❑ Core internal scan paths & WBR are connected in parallel to TAM by a “Core Test” instruction
- ❑ Today, many flavors of “TAMs” & TAM “Interfaces” exist

# *P1500 Instructions*

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# **P1500 Instructions**

# ***P1500 Instructions***

## ***Mission Statement***

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### **To Define Instructions for the WIR;**

- To operate the wrapper to allow for internal and external testing.

- **CORETEST and WEXTEST**

- To operate the wrapper such that it provides a safe mode for the core and if needed, the logic adjacent to the core (from the outputs of the core).

- **SAFESTATE**

- To operate the wrapper to allow for debug.

- **WSCORETEST, SCORETEST, CORETEST**

- To operate the wrapper to allow IddQ measurements.

- **SCORETEST**

# ***P1500 Instructions***

## ***Mission Statement***

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### **To Define Instructions for the WIR; (continued)**

To test the wrapper logic.

- **WSCORETEST**

To allow functional operation through the wrapper

- **WBYPASS**

To allow setup for test

- **WPRELOAD, WCLAMP**

# ***P1500 Instructions***

## ***Status***

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### **□ Serial Instruction Set**

- **Wrapper External Test (WEXTEST) - Mandatory Instruction**
- **Wrapper Bypass (WBYPASS) - Mandatory Instruction**
- **Wrapper Safe State (SAFESTATE) - Optional Instruction**
- **Wrapper Clamp (WCLAMP) – Mandatory Instruction**
- **Wrapper Preload (WPRELOAD) - Mandatory Instruction**
- **Wrapper Serial Core Test (WSCORETEST) - nearing completion**
- **Serial Core Test (SCORETEST) - nearing completion**
- **Core Test (CORETEST) – nearing completion**

# ***P1500 Instructions***

## ***WEXTEST Instruction (SIL)***

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**WEXTEST allows testing of off-core logic and interconnect.**

### **Rules**

- WEXTEST Instruction Mandatory
- Wrapper Boundary Register accessed serially between WSI and WSO
- Core in a Safe Mode
- All signals driven out of the wrapper output terminals are defined by the values held in the wrapper boundary register
- Wrapper input terminals load only during capture
- 3-state output cell must be loaded with safe data by use of WPRELOAD

# ***P1500 Instructions***

## ***WEXTEST Instruction (SIL)***

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### **Recommendations**

- Core should be put in a quiet mode
- Wrapper output terminals should be driven by the state of the wrapper boundary cell
- Where shared wrapper cells are used, the outputs should be safe during shift.

### **Permissions**

- Binary code for the instruction may be defined by the user

# ***P1500 Instructions***

## ***WBYPASS Instruction (SIL)***

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**WBYPASS allows the Wrapper Boundary Register to be bypassed from WSI to WSO. This instruction also forces the core into its normal operation mode.**

### **Rules**

- WBYPASS instruction mandatory
- Wrapper Bypass Register accessed serially between WSI and WSO
- Operation of test logic will not affect functional operation
- All wrapper cells will perform their system function
- Wrapper input terminals load only during capture

### **Permissions**

- Binary code for the instruction may be defined by the user

# ***P1500 Instructions***

## ***WCLAMP Instruction (SIL)***

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**WCLAMP clamps the state of the output terminals of the WBR and Selects the Bypass Register between WSI and WSO.**

### **Rules**

- WBYPASS Register selected
- Data on the output terminals defined by the WBR
- Core in a safe mode
- Parallel output states shall not change
- States on the inputs to the core shall not damage the core

### **Recommendations**

- Core should be put in a quiet mode

### **Permissions**

- Binary code for the instruction may be defined by the user

# ***P1500 Instructions***

## ***SAFESTATE Instruction (SIL)***

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**Same function as WCLAMP, but does not require use of the WPRELOAD instruction. Clamped values must be safe. Important enough for its own instruction.**

### **Rules**

- WBYPASS Register selected
- Data on output terminals driven by safe values
- Core in a safe mode
- Parallel output states shall not change
- States on the inputs to the core shall not damage the core

### **Recommendations**

- Core should be put in a quiet mode

### **Permissions**

- Binary code for the instruction may be defined by the user

# ***P1500 Instructions***

## ***WPRELOAD Instruction (SIL)***

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**WPRELOAD loads a Dedicated Shift Path in the WBR with desired values, then Updates the Update Stage.**

### **Rules**

- If there is a dedicated shift path in the WBR, WPRELOAD is Mandatory
- Dedicated shift path is serial – connected between WSI and WSO
- Shift does not affect the core or user-defined logic
- Data will be loaded to the update stage during the update operation
- States on the inputs to the core shall not damage the core

### **Recommendations**

- Core should be put in a quiet mode

### **Permissions**

- Binary code for the instruction may be defined by the user

# ***P1500 Instructions***

## ***CORETEST Instruction***

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### **CORETEST configures the Wrapper for Core Testing Rules**

- At least one CORETEST instruction is mandatory
- During CORETEST, no external logic or core shall be affected

### **Permissions**

- Binary code for the instruction may be defined by the user
- Any number of CORETEST instructions may be defined

# ***P1500 Instructions***

## ***WSCORETEST Instruction (SIL) (In discussion)***

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### **WSCORETEST configures the Wrapper Serially for Core Testing**

#### **Rules**

- WBR serial access is between WSI and WSO
- Core must be capable of single-step operation
- Core outputs are defined by the WBR during the Apply cycle only
- All non-clock core input values are driven by the WBR
- Core output data shall be loaded into the WBR before shifting the WBR

#### **Recommendations**

- External Logic should not affect the input cells of the WBR

#### **Permissions**

- Binary code for the instruction may be defined by the user

# ***P1500 Instructions***

## ***Wrapper Serial CORETEST Instruction (SIL)***

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**Configures the Wrapper Serially for Core Testing**

**Rules**

**Recommendations**

**Permissions**

Written, but currently in the approval cycle.

# ***P1500 Instructions***

## ***Serial CORETEST Instruction (SIL)***

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**Configures the Wrapper and Internal Scan Chains  
Serially for Core Testing**

**Rules**

**Recommendations**

**Permissions**

Will exactly follow the WSCORETEST Rules, but will attach the internal serial scan chain as well.

# **CTAG Update**

## **Status Since ITC 2000**

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- ❑ **Wrapper Serial Interface Layer (SIL) is stable**
  - Resolution of SIL connection discussions from ITC 2000
  - A few details remain, but are being worked out:
    - ✓ For example, general WIP timing and better WART definition
  
- ❑ **Wrapper Parallel Interface Layer (PIL) being specified**
  - PIL addresses various Wrapper TAM interface types
  - Reviewing earlier TAM discussions and working toward a specification
  
- ❑ **Key focus is to complete CTAG doc sections and review**
  - Tiger teams are updating and revising their sections
    - ✓ WIR Tiger team, sections 3, 4 and 7
    - ✓ Instruction Tiger Team, section 5
    - ✓ WBR Tiger Team, section 6