

Unapproved IEEE P1500 Working Document



***Update of Proposed IEEE P1500
Scaleable Architecture for Testing
Embedded Cores***

Presented on behalf of the CTAG Team by

Lee Whetsel

October 2, at ITC 2000

Presentation Outline

□ Introduction

- **CTAG Task Force Mission and Scope**
- **Organization & Members**

□ System Chip Example with P1500 Wrapped Cores

□ P1500 Architecture

- **Wrapper Components**
- **Wrapper Serial Interface Layer (SIL) Architecture**
- **Wrapper Interface Port (WIP)**
- **Wrapper Boundary Cells**
- **Wrapper Example with a Parallel TAM Interface**

□ P1500 Wrapper Instructions

P1500 Architecture Task Force

Summary of Task Force Mission and Scope

Goals of IEEE P1500

Standardize a Core Test Architecture which:

1. Defines a core test interface between an embedded core and the system chip.
2. Facilitate test reuse for embedded cores through core access and isolation mechanisms, and provide testability for system chip interconnect and logic.
3. Facilitates core test interoperability, with plug-and-play protocols, in order to improve the efficiency of test between core providers and core users.

Scope of IEEE P1500

- ✓ **Standardize *core* test mechanisms, for core access and isolation, including protocols and test mode control.**
- ✗ ***System Chip* test access mechanism is defined by the system chip integrator.**
- ✗ **The *core test method* is defined by the core provider – P1500 supports, and enables, various different methods (e.g., scan, BIST, I_{ddq} , etc.).**

P1500 Architecture Task Force

Active Task Force Members

Lee Whetsel (Task Force Chair) - Texas Instruments

Saman Adham - LogicVision

Debashis Bhattacharya - TI

Dwayne Burek - LogicVision

Bulent Dervisoglu - Cadence

C.J. Clark - Intellitech

Mike Collins - Collins Design

★ Jason Doege - Inovys

Grady Giles - AMD

Sanjay Gupta - SiberCore

Alan Hales - Texas Instruments

Andy Halliday - TriMedia Technologies

Douglas Kay - Cisco Systems

Erik Jan Marinissen - Philips

★ Teresa McLaurin - ARM

Fidel Muradali - Agilent Technologies

Srinivas Patil - Mentor Graphics

Rochit Rajsuman - Advantest

★ Mike Ricchetti - Intellitech

Eddie Rodriguez - Intel

Paul Soong - Nortel

Wu Tung - Mentor Graphics

Jon Udell - Palmchip

Greg Young - Motorola

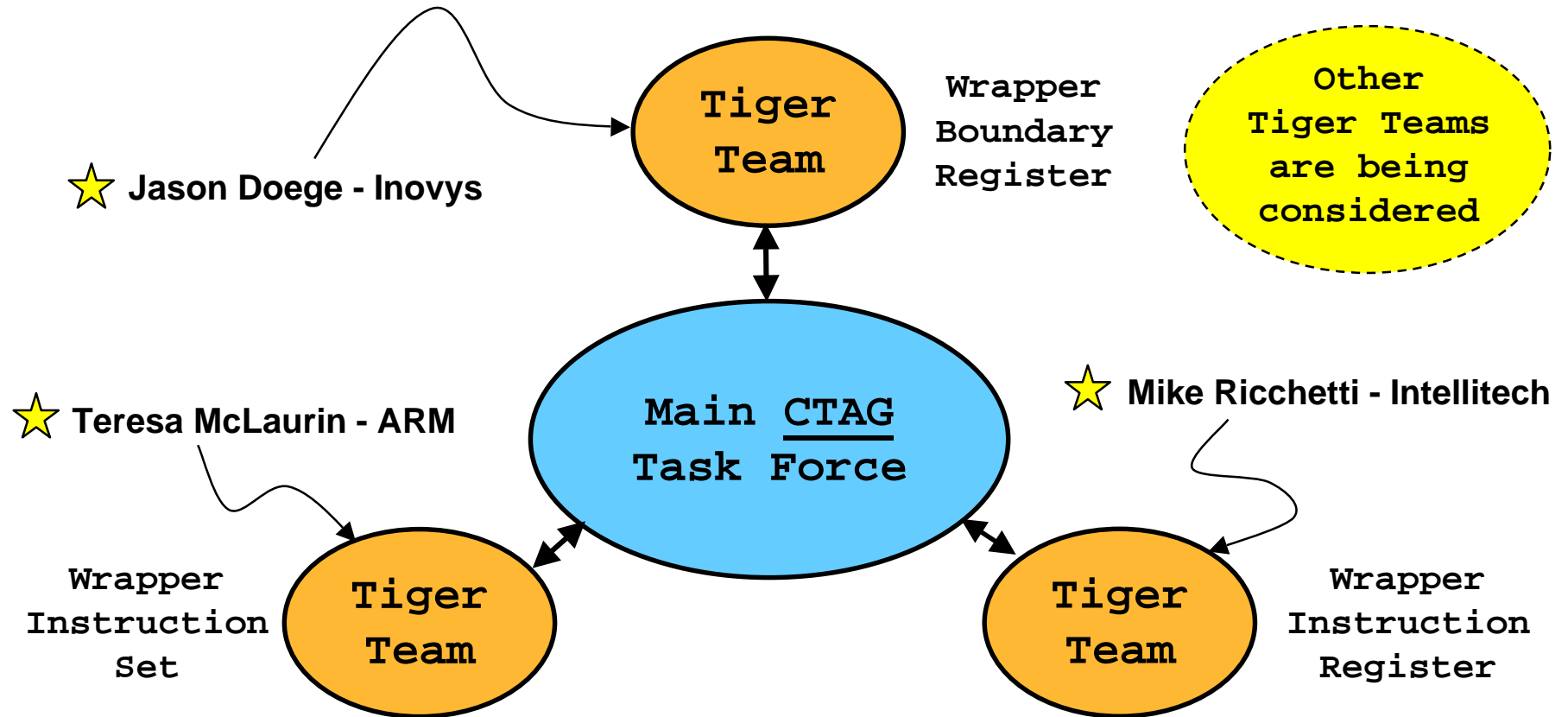
Alex Zamfirescu - ASC

Yervant Zorian - LogicVision

★ - Tiger Team Champions

P1500 Architecture Task Force

Organization of Task Force



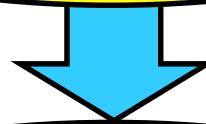
CTAG = ~~Joint~~ (Core) Test Action Group (Adopted Name from JTAG)

P1500 Architecture Task Force

Task Force Wrapper Development Phases

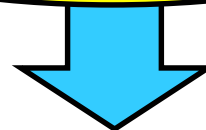
Phase 1

**Develop Wrapper's
Serial Interface Layer
(SIL)**



Phase 2

**Develop Wrapper's
Interface to Parallel
Test Access Mechanisms
(TAM)**

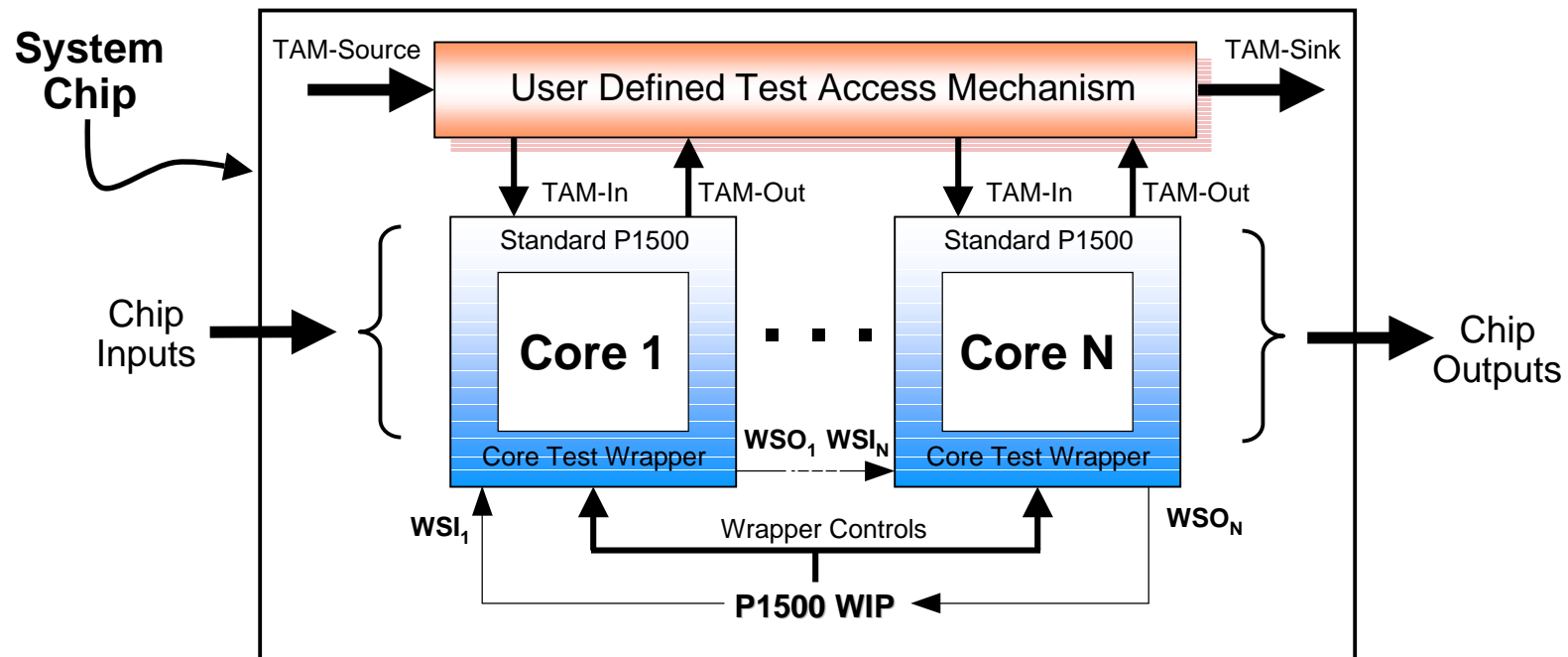


P1500 Standard

P1500 Architecture

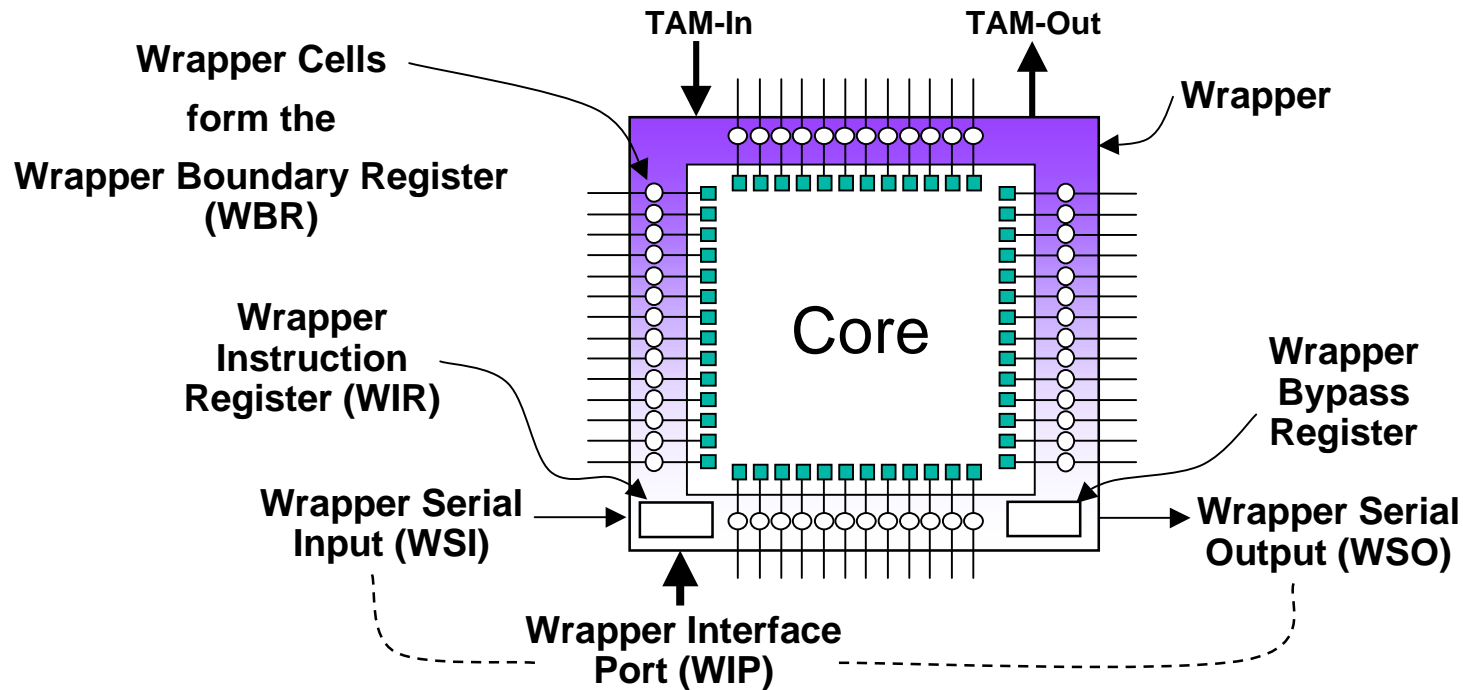
P1500 Architecture

System Chip with P1500 Wrapped Cores



- **TAM Source/Sink**
 - ✓ From chip I/O, test bus/rail/port, BIST, etc...
- **TAM In/Out**
 - ✓ 0 to n lines for parallel and/or serial test data, or test control
- **P1500 Wrapper Interface Port (WIP)**
 - ✓ From chip-level TAP Controller, chip I/O, etc...

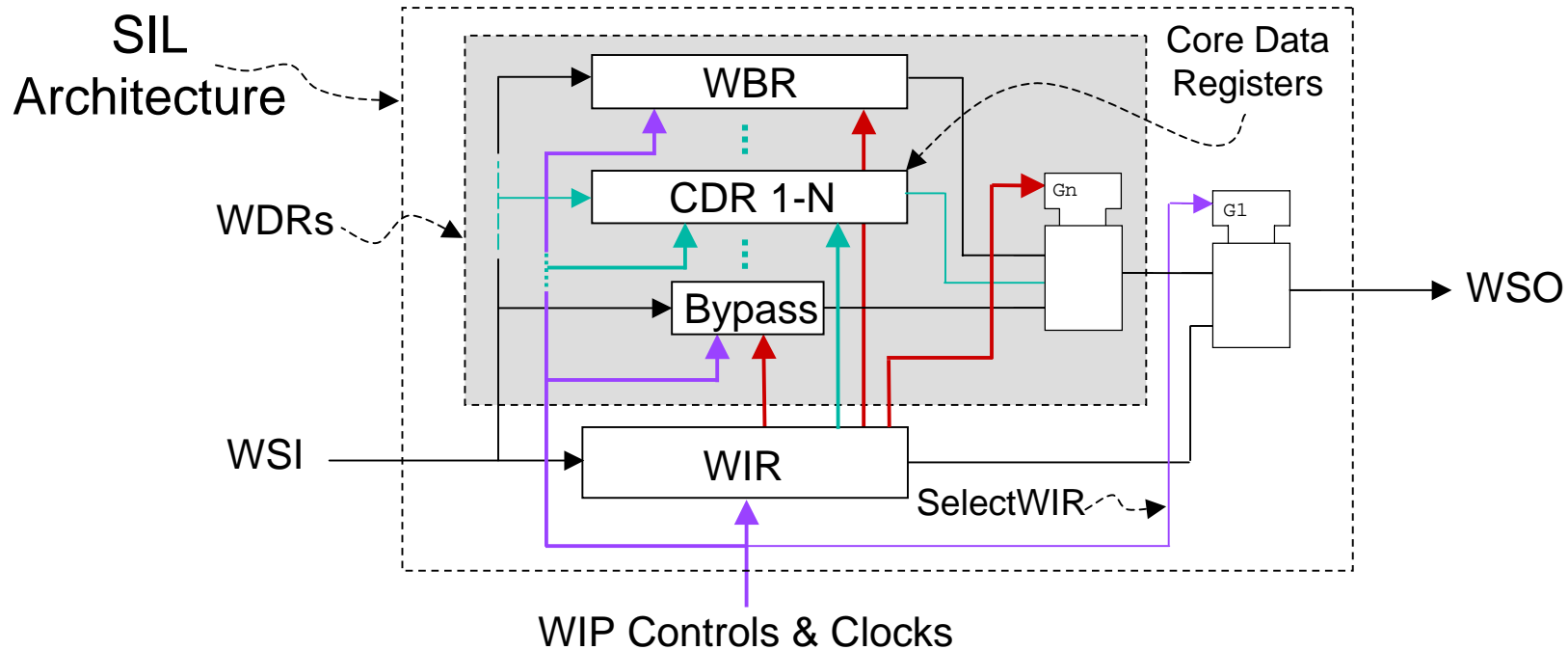
P1500 Architecture Components



□ A P1500 Wrapper has the following:

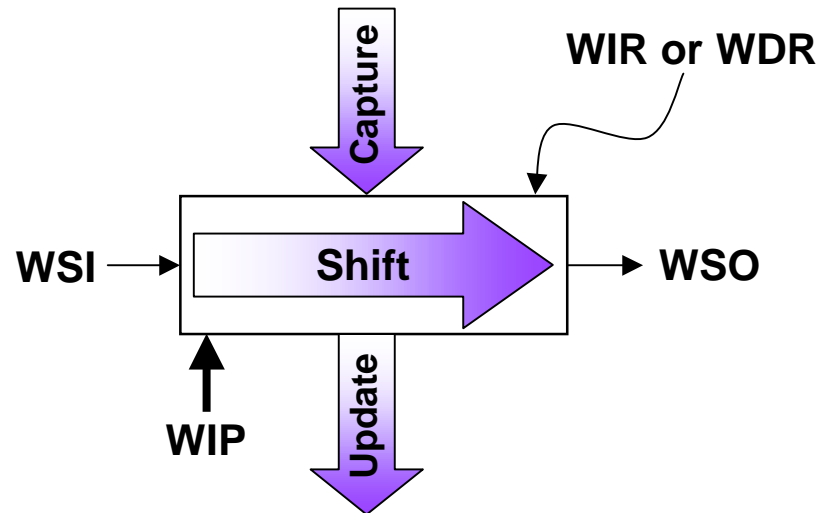
- A WIR for providing wrapper mode control
- Wrapper Cells to provide test functions at the core terminals
- A Bypass register for scan bypass through the wrapper
- The WIP for standard serial control (WIR, Bypass & WBR) and optionally TAM control

P1500 Serial Interface Layer Architecture



- ❑ WIP selects the WIR or a Wrapper Data Register (WDR) between WSI and WSO
- ❑ Updated WIR output determines:
 - Which WDR (i.e. Bypass, CDR, or WBR) is selected between WSI and WSO
 - The current P1500 Wrapper Mode and (optionally) the Core Mode
 - If a user defined TAM connection & register configuration is enabled
- ❑ The Wrapper Bypass Register provides a scan bypass from WSI to WSO

P1500 Wrapper IR (WIR) & Wrapper DR (WDR) Behavior

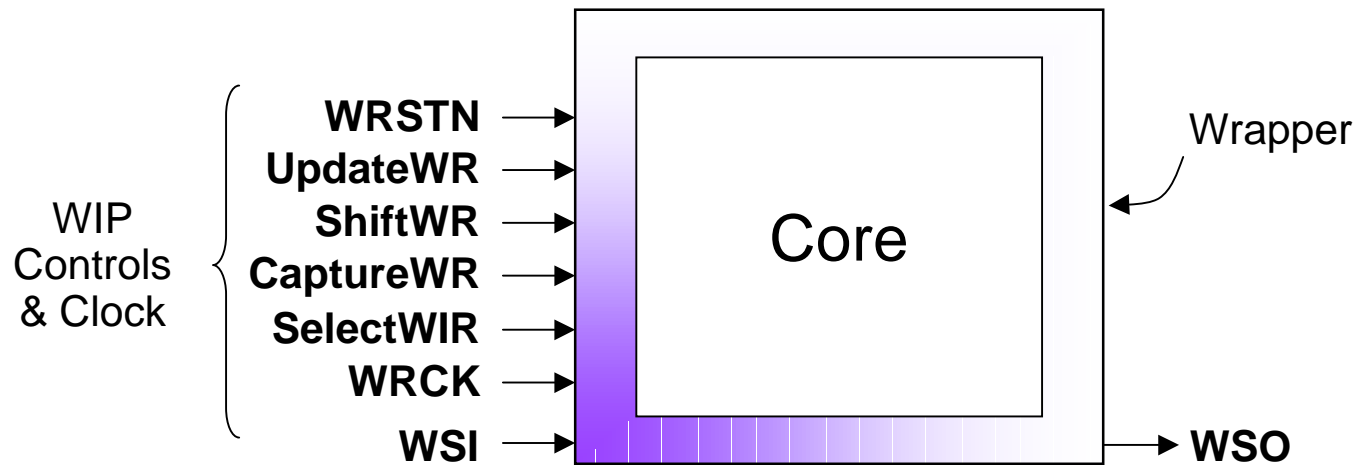


□ **Standard P1500 Wrapper Instruction and Data Registers provide:**

- **Required Serial *Shift* from WSI to WSO**
- **Optional parallel *Update***
 - ✓ Updated output data held stable during shift operations from WSI to WSO
 - ✓ Required for WIR to prevent Wrapper & Core Modes from toggling during WIR shift
- **Optional parallel *Capture***
 - ✓ Required for WBR to provide interconnect and UDL test capability
 - ✓ Optional for WIR to provide capture of test control information, or for testing of WIR circuitry & WSI to WSO scan paths

P1500 Wrapper Interface Port (WIP)

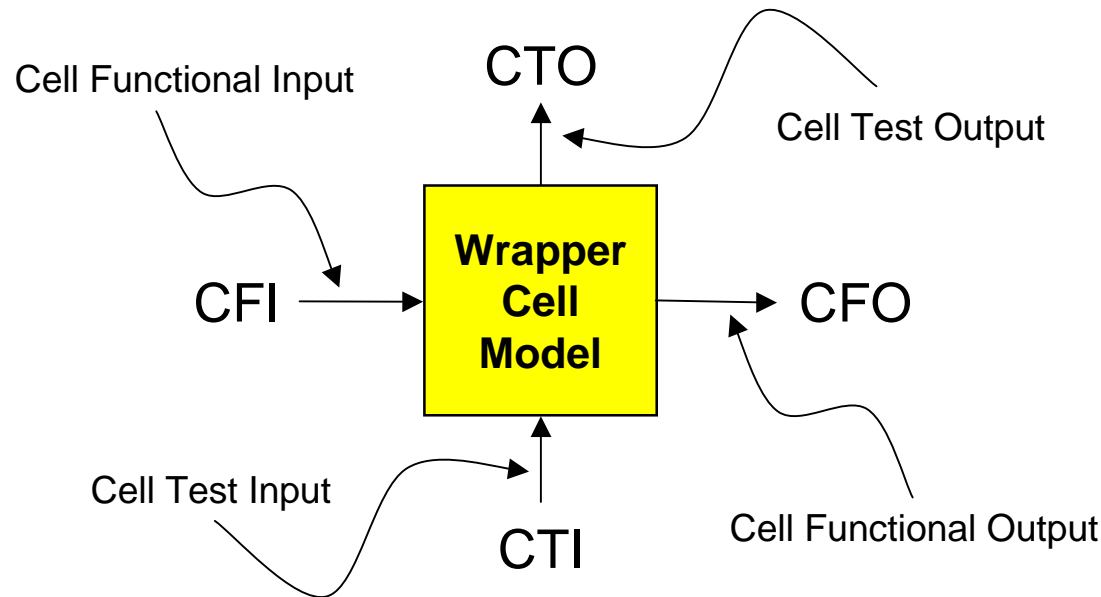
WIP Signals for Accessing WIR, WDR, & Bypass



- ❑ **The WIP is currently defined to access only the WIR, Bypass, and WBR**
 - WIP could also be used to access CDRs (e.g., core internal scan data registers)
- ❑ **WIP Terminals:**
 - WRCK is the clock used to operate the registers
 - WRSTN is a dedicated asynchronous Wrapper Reset
 - SelectWIR selects whether or not the WIR is connected between WSI and WSO
 - UpdateWR, ShiftWR and CaptureWR are enables for register operations
 - ✓ May be used for clock gating

P1500 Wrapper Boundary Cells

Overview of Cell Modes



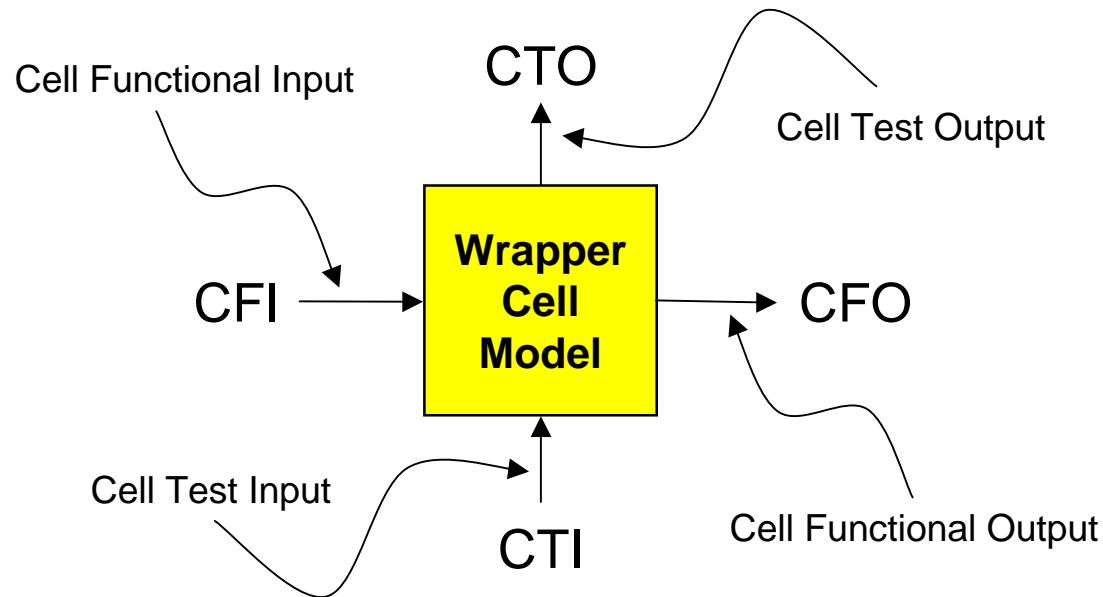
❑ Cell Modes

- ✓ **Normal**: No Effect, core functions normally
- ✓ **Inward Facing**: Affects the core, test is directed towards core
- ✓ **Outward Facing**: Affects the core, test is directed outward from core
- ✓ **Safe**: Affects the core & ensures wrapper does not damage core or system (a recommended mode)

Note: Inward and Outward Facing Test Modes Mirror one another

P1500 Wrapper Boundary Cells

Overview of Cell Events



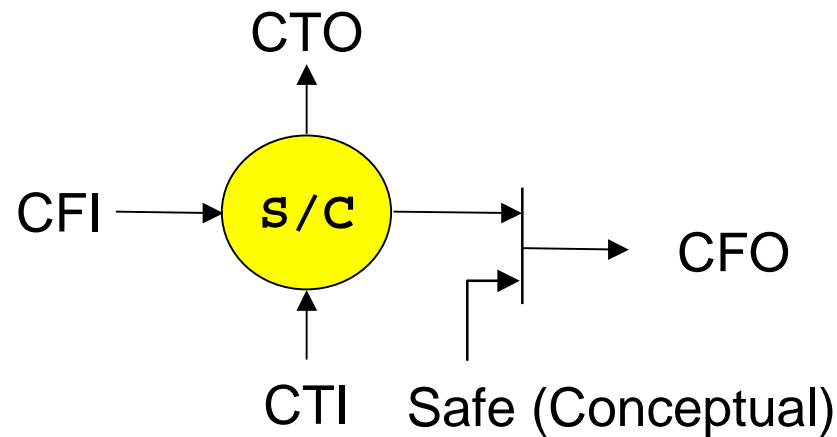
❑ Cell Events

- ✓ **Shift:** Move data through shift path
- ✓ **Capture:** Sample data
- ✓ **Apply:** Moment when test data becomes active and effective
- ✓ **Update:** 1149.1-type Update
- ✓ **Transfer:** Move data from Update element to Shift path

P1500 Wrapper Boundary Cells

Overview of Cell Types

Simple Wrapper Cell Example



❑ Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

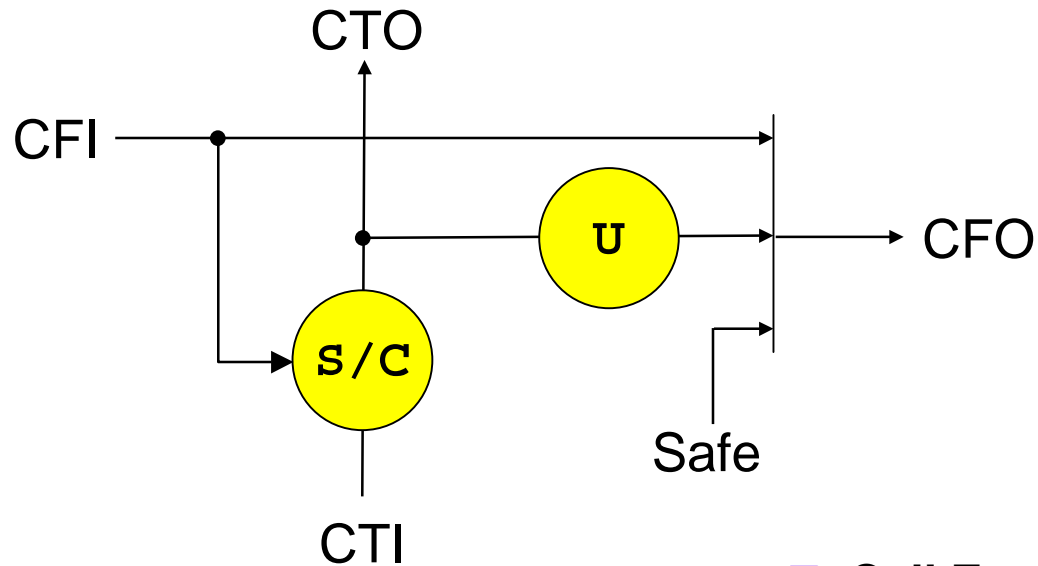
❑ Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply

P1500 Wrapper Boundary Cells

Overview of Cell Types

1149.1 Type Cell Example



Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

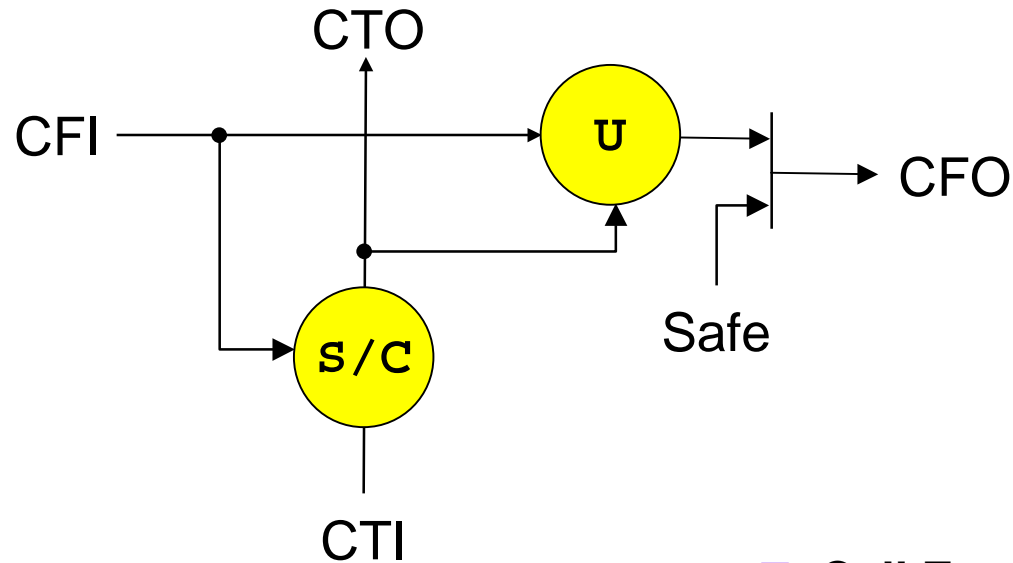
Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update

P1500 Wrapper Boundary Cells

Overview of Cell Types

Cell Example with Shared Update



Cell Modes

- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

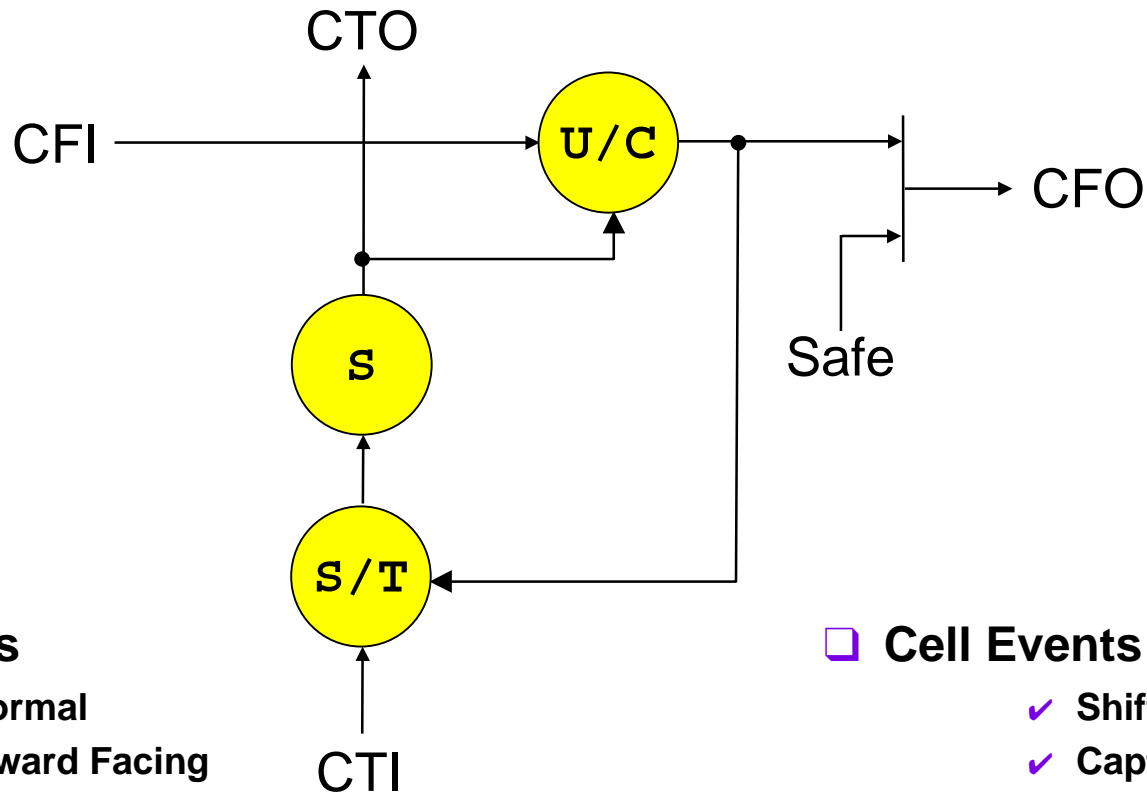
Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update

P1500 Wrapper Boundary Cells

Overview of Cell Types

Cell Example Displaying all Events



Cell Modes

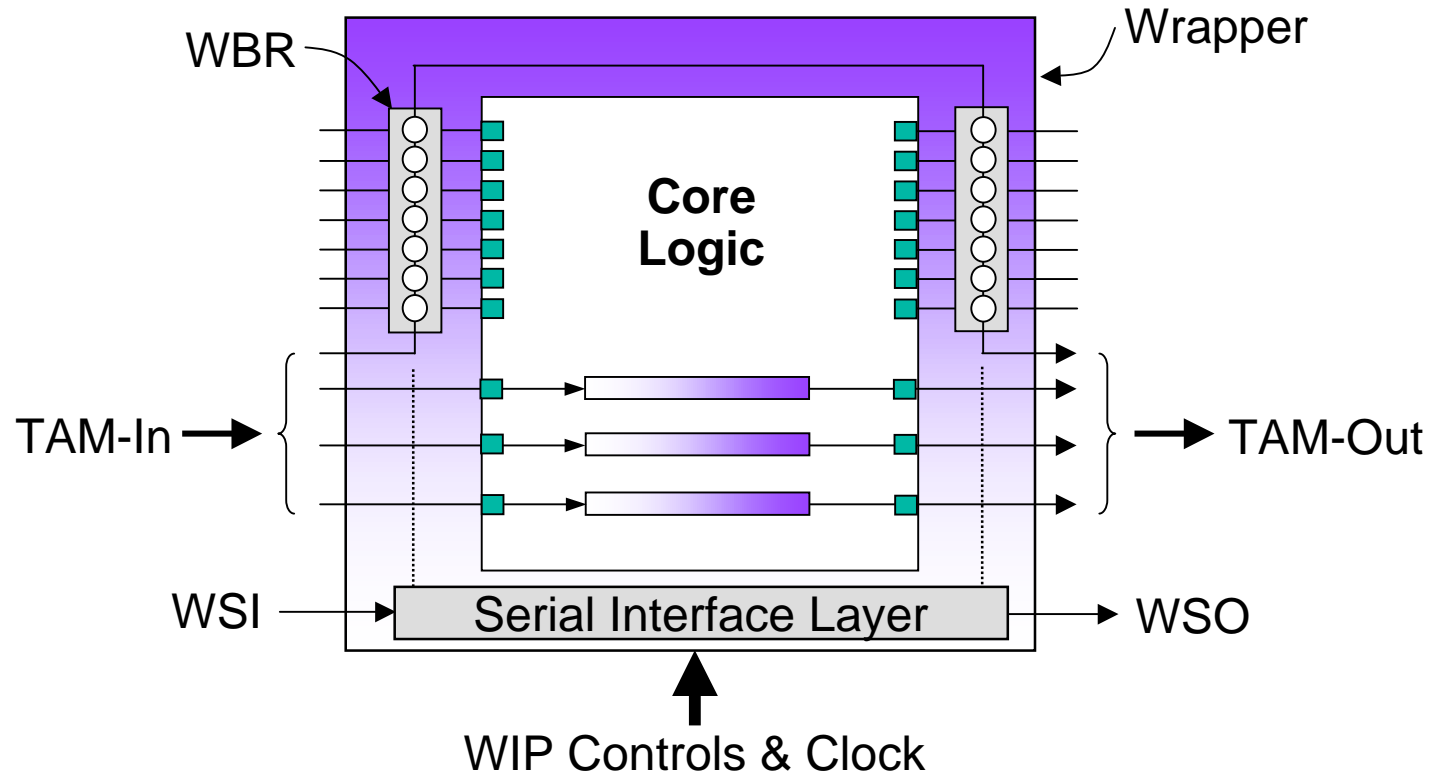
- ✓ Normal
- ✓ Inward Facing
- ✓ Outward Facing
- ✓ Safe

Cell Events

- ✓ Shift
- ✓ Capture
- ✓ Apply
- ✓ Update
- ✓ Transfer

P1500 Architecture

Wrapper Example with a Parallel TAM Interface



- ❑ Core internal scan paths & WBR are connected in parallel to TAM by a “Core Test” instruction
- ❑ Today, many flavors of “TAMs” & TAM “Interfaces” exist

P1500 Instructions

P1500 Instructions

P1500 Instructions

Mission Statement

To Define Instructions for the WIR;

- To operate the wrapper to allow for internal and external testing.

- **CORETEST and WEXTEST**

- To operate the wrapper such that it provides a safe mode for the core and if needed, the logic adjacent to the core (from the outputs of the core).

- **SAFESTATE**

- To operate the wrapper to allow for debug.

- **WSCORETEST, SCORETEST, CORETEST**

- To operate the wrapper to allow IddQ measurements.

- **SCORETEST**

P1500 Instructions

Mission Statement

To Define Instructions for the WIR; (continued)

To test the wrapper logic.

- **WSCORETEST**

To allow functional operation through the wrapper

- **WBYPASS**

To allow setup for test

- **WPRELOAD, WCLAMP**

P1500 Instructions

Status

□ Serial Instruction Set

- **Wrapper External Test (WEXTEST) - Mandatory Instruction**
- **Wrapper Bypass (WBYPASS) - Mandatory Instruction**
- **Wrapper Safe State (SAFESTATE) - Optional Instruction**
- **Wrapper Clamp (WCLAMP) – Mandatory Instruction**
- **Wrapper Preload (WPRELOAD) - Mandatory Instruction**
- **Wrapper Serial Core Test (WSCORETEST) - nearing completion**
- **Serial Core Test (SCORETEST) - nearing completion**
- **Core Test (CORETEST) – nearing completion**

P1500 Instructions

WEXTEST Instruction (SIL)

WEXTEST allows testing of off-core logic and interconnect.

Rules

- WEXTEST Instruction Mandatory
- Wrapper Boundary Register accessed serially between WSI and WSO
- Core in a Safe Mode
- All signals driven out of the wrapper output terminals are defined by the values held in the wrapper boundary register
- Wrapper input terminals load only during capture
- 3-state output cell must be loaded with safe data by use of WPRELOAD

P1500 Instructions

WEXTEST Instruction (SIL)

Recommendations

- Core should be put in a quiet mode
- Wrapper output terminals should be driven by the state of the wrapper boundary cell
- Where shared wrapper cells are used, the outputs should be safe during shift.

Permissions

- Binary code for the instruction may be defined by the user

P1500 Instructions

WBYPASS Instruction (SIL)

WBYPASS allows the Wrapper Boundary Register to be bypassed from WSI to WSO. This instruction also forces the core into its normal operation mode.

Rules

- WBYPASS instruction mandatory
- Wrapper Bypass Register accessed serially between WSI and WSO
- Operation of test logic will not affect functional operation
- All wrapper cells will perform their system function
- Wrapper input terminals load only during capture

Permissions

- Binary code for the instruction may be defined by the user

P1500 Instructions

WCLAMP Instruction (SIL)

WCLAMP clamps the state of the output terminals of the WBR and Selects the Bypass Register between WSI and WSO.

Rules

- WBYPASS Register selected
- Data on the output terminals defined by the WBR
- Core in a safe mode
- Parallel output states shall not change
- States on the inputs to the core shall not damage the core

Recommendations

- Core should be put in a quiet mode

Permissions

- Binary code for the instruction may be defined by the user

P1500 Instructions

SAFESTATE Instruction (SIL)

Same function as WCLAMP, but does not require use of the WPRELOAD instruction. Clamped values must be safe. Important enough for its own instruction.

Rules

- WBYPASS Register selected
- Data on output terminals driven by safe values
- Core in a safe mode
- Parallel output states shall not change
- States on the inputs to the core shall not damage the core

Recommendations

- Core should be put in a quiet mode

Permissions

- Binary code for the instruction may be defined by the user

P1500 Instructions

WPRELOAD Instruction (SIL)

WPRELOAD loads a Dedicated Shift Path in the WBR with desired values, then Updates the Update Stage.

Rules

- If there is a dedicated shift path in the WBR, WPRELOAD is Mandatory
- Dedicated shift path is serial – connected between WSI and WSO
- Shift does not affect the core or user-defined logic
- Data will be loaded to the update stage during the update operation
- States on the inputs to the core shall not damage the core

Recommendations

- Core should be put in a quiet mode

Permissions

- Binary code for the instruction may be defined by the user

P1500 Instructions

CORETEST Instruction

CORETEST configures the Wrapper for Core Testing Rules

- At least one CORETEST instruction is mandatory
- During CORETEST, no external logic or core shall be affected

Permissions

- Binary code for the instruction may be defined by the user
- Any number of CORETEST instructions may be defined

P1500 Instructions

WSCORETEST Instruction (SIL) (In discussion)

WSCORETEST configures the Wrapper Serially for Core Testing

Rules

- WBR serial access is between WSI and WSO
- Core must be capable of single-step operation
- Core outputs are defined by the WBR during the Apply cycle only
- All non-clock core input values are driven by the WBR
- Core output data shall be loaded into the WBR before shifting the WBR

Recommendations

- External Logic should not affect the input cells of the WBR

Permissions

- Binary code for the instruction may be defined by the user

P1500 Instructions

Wrapper Serial CORETEST Instruction (SIL)

Configures the Wrapper Serially for Core Testing

Rules

Recommendations

Permissions

Written, but currently in the approval cycle.

P1500 Instructions

Serial CORETEST Instruction (SIL)

**Configures the Wrapper and Internal Scan Chains
Serially for Core Testing**

Rules

Recommendations

Permissions

Will exactly follow the WSCORETEST Rules, but will attach the internal serial scan chain as well.