

P1500's Core Test Language

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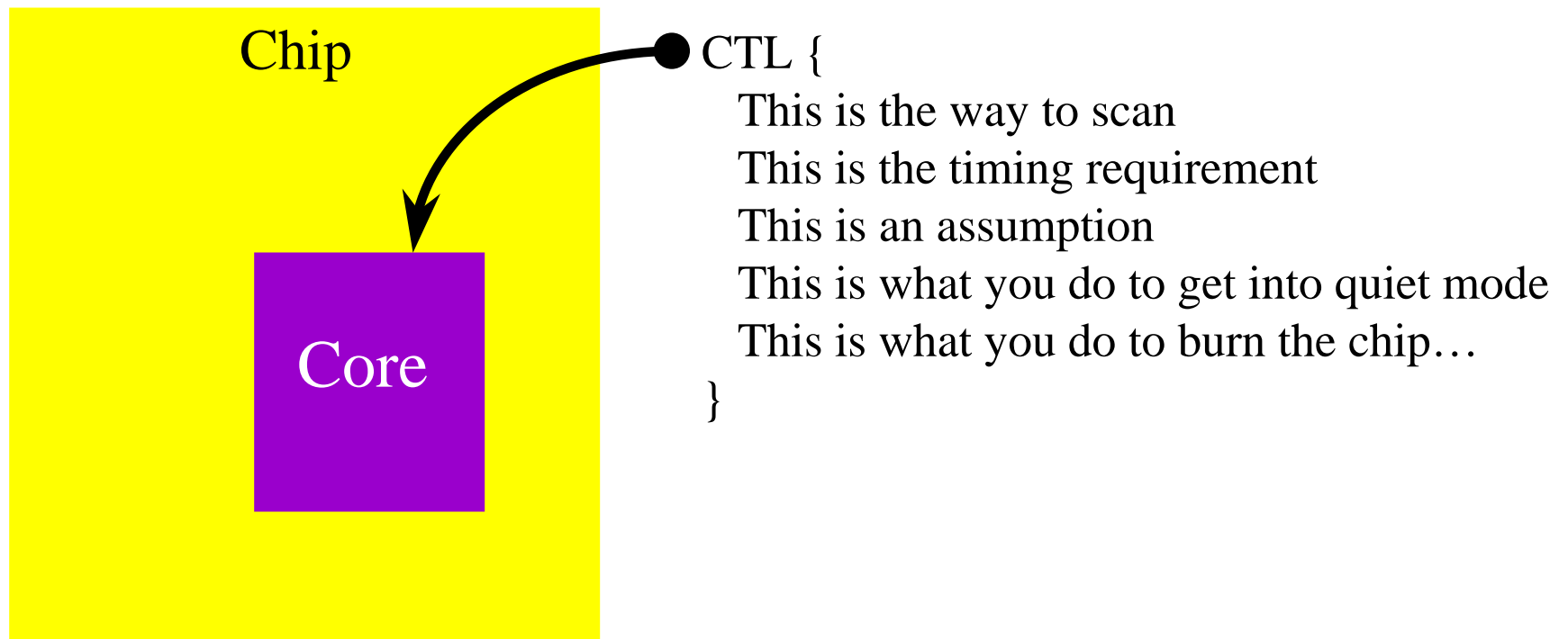
Tony Taylor (Synopsys)



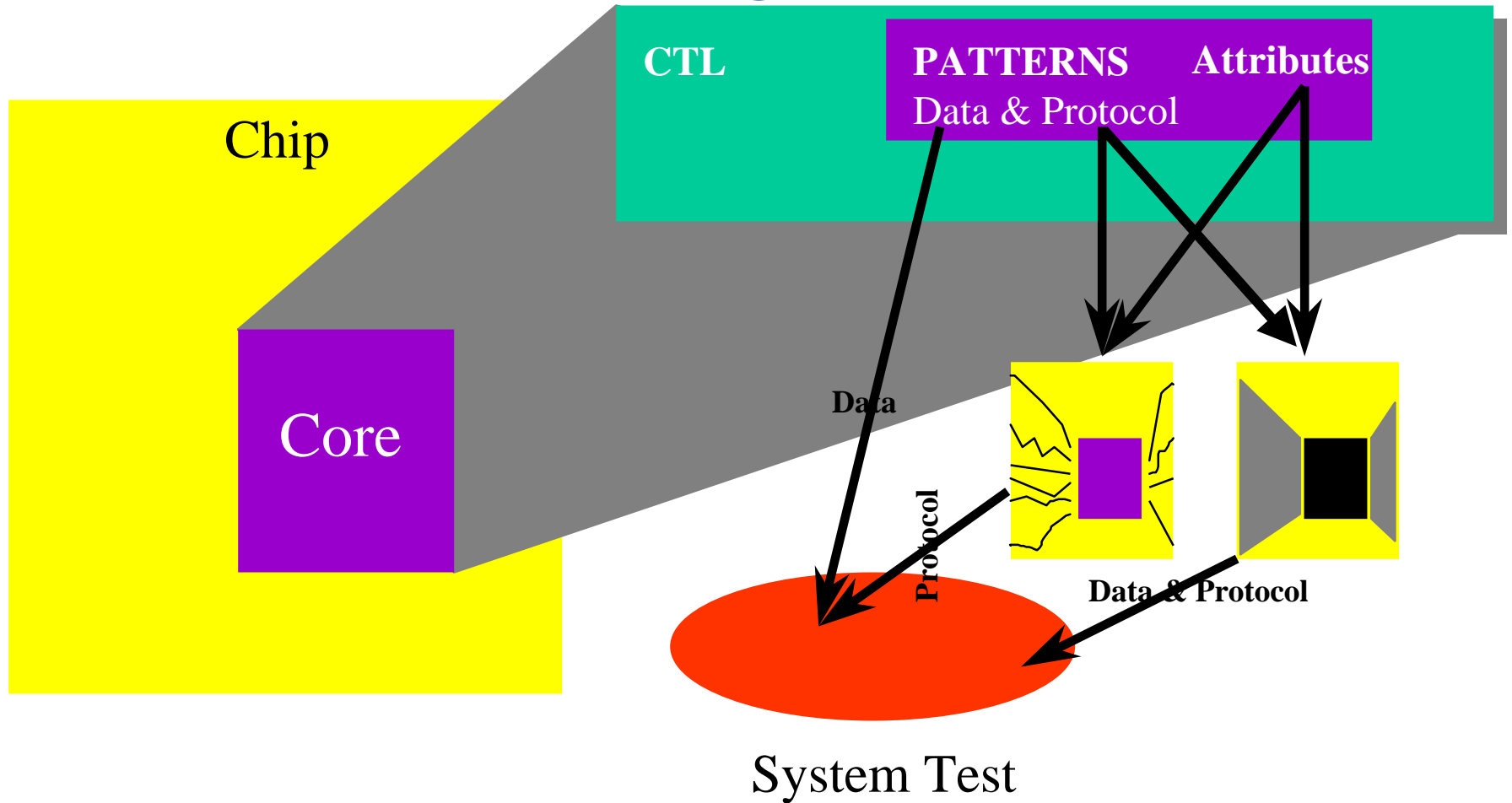
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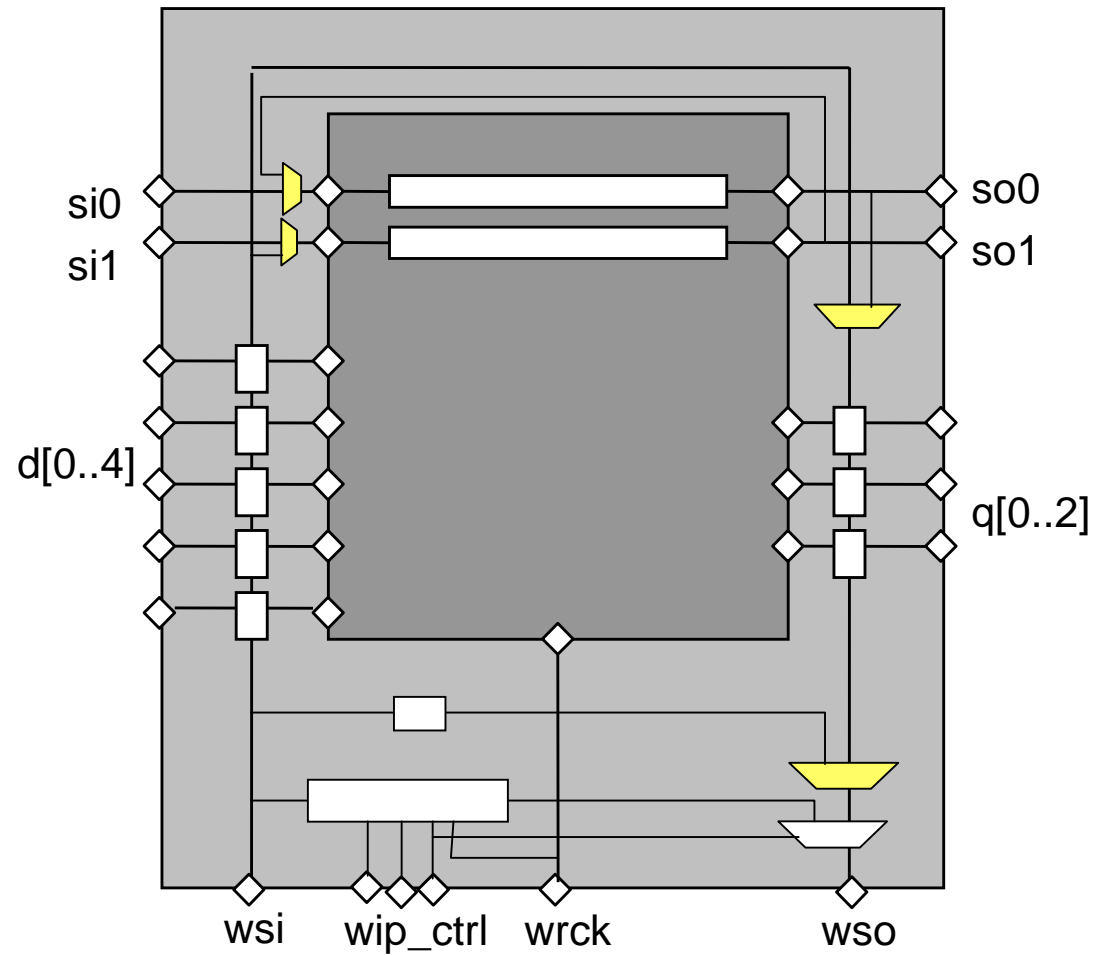
One CTL Per Design



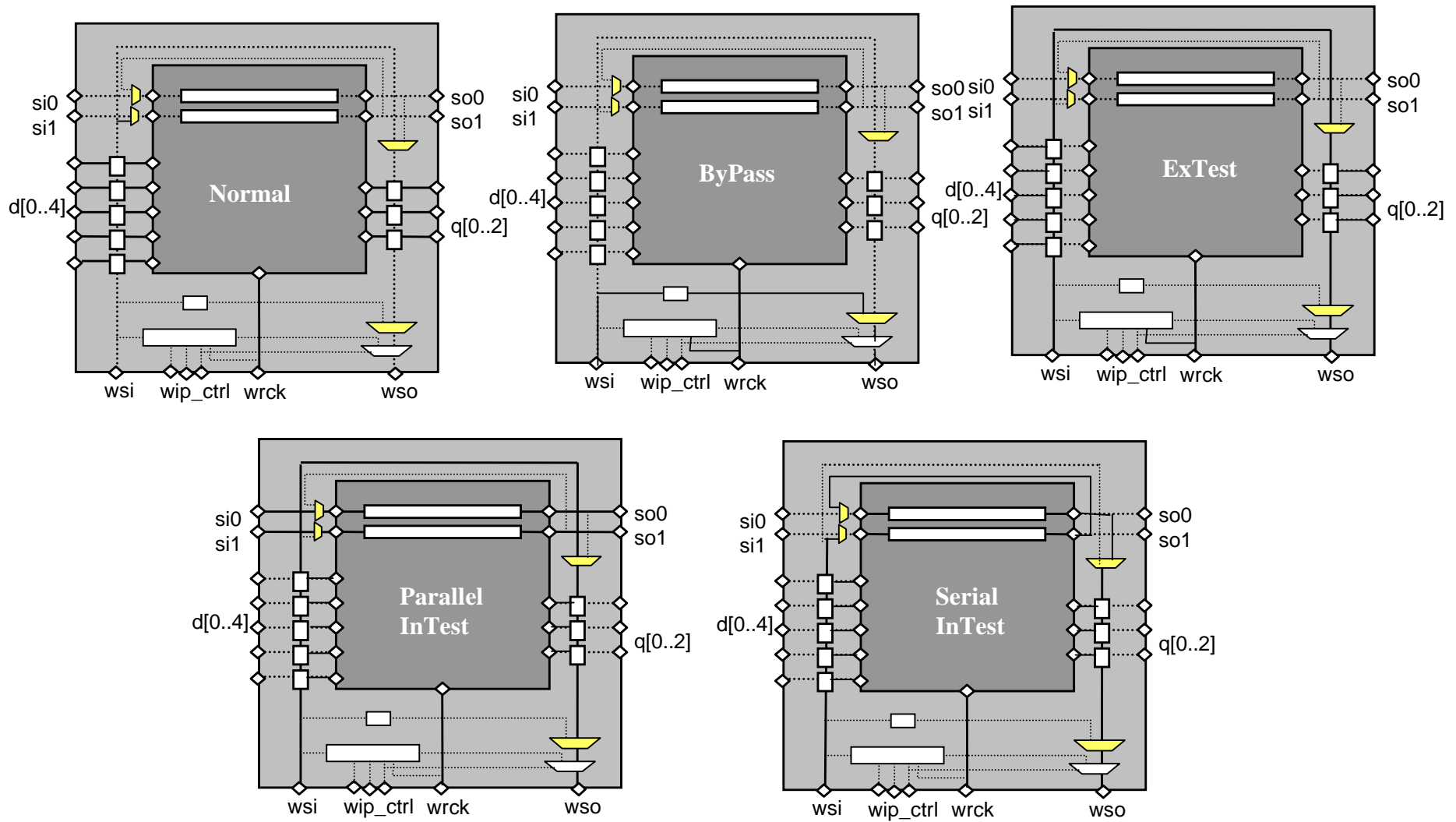
Test Your Chip Using CTL and Not the Logic Model



Example Design To Be Described in CTL



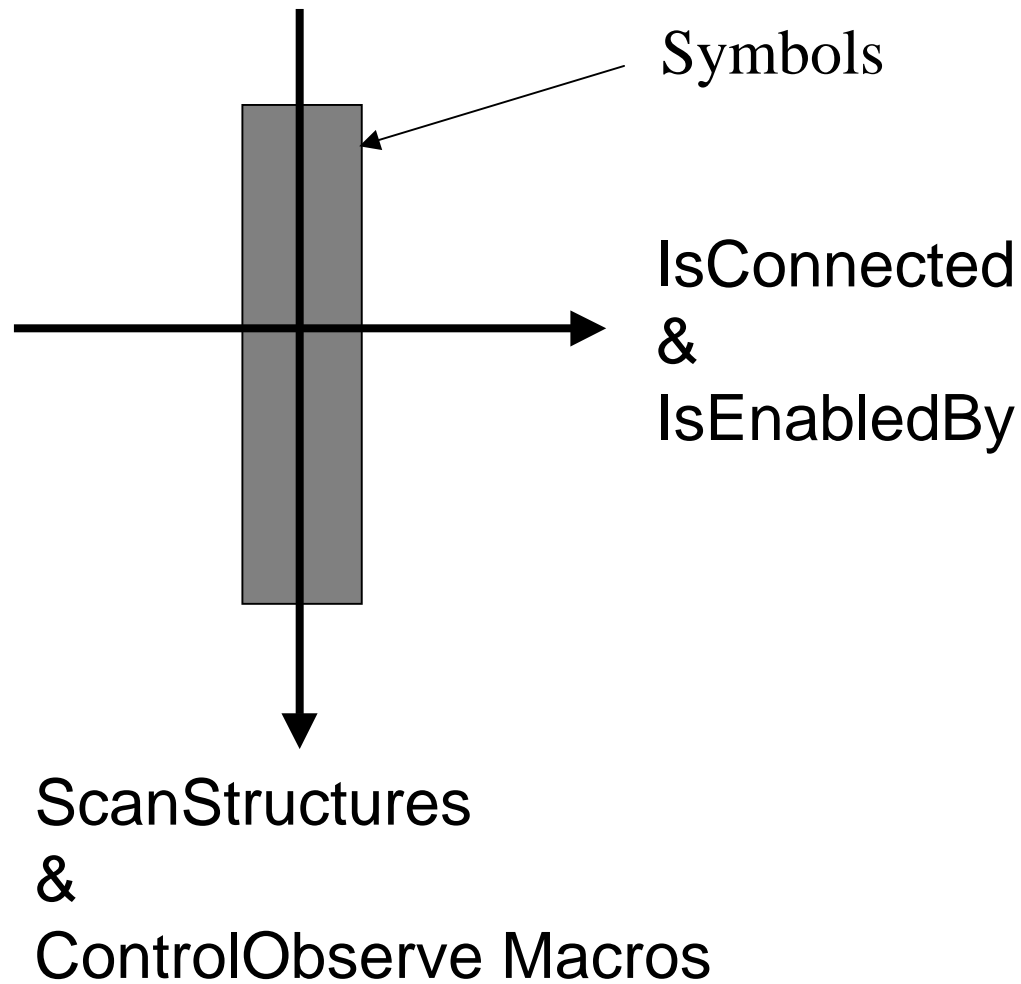
A Design Has Many Modes



Things That Need To Be Described

- For Each Mode:
 - Connections
 - Protocols
 - Attributes on a signal by signal basis
- General Designs
- All Test Methods

Connections



Protocols

A sequence of events described by Vectors.

```
Macro {  
    Vector { .... }  
    Vector { .... }  
    Shift { .... }  
    Vector { .... }  
}
```

Some special protocols are identifiable

- Initialization of the Mode
- Control, Observe, ControlObserve
- Instruction

Attributes on Signals

- DataType
 - Set, Reset, ScanIn, ScanOut, Clock, Read, Write, ScanEnable, TestData, TestMode ...
- DataRate
 - Events, Vectors, Patterns
- Properties
 - LevelSensitive, ScanStable, Transitions, Pullup, PullDown, DriveAccuracy, StrobeAccuracy, ElectricalProperties.
- Relationships between signals
 - Differential, Unique, Port, Scan, Equivalent
- Standardized names of Pins and Cells

Framework for the Information

```
Environment {
```

```
  CTL {
```

```
  }
```

```
  CTL mode1 {
```

```
    TestMode InternalTest;
```

```
  }
```

```
  CTL mode2 {
```

```
    TestMode ExternalTest;
```

```
  }
```

```
}
```

```
CTL modeX {
```

```
  TestMode X;
```

```
  Attributes;
```

```
  Connections;
```

```
  Protocols;
```

```
}
```

Mixed Signal Testing

- Today's CTL should be able to describe the digital side of mixed signal test methods.
- We should test CTL from a BSDL/ABSDL point of view.
- At some point CTL will have to upgrade to handle analog natively.