

Unapproved IEEE P1500 Working Document



CTAG WIR Tiger Team Status

**Prepared by Mike Ricchetti for
P1500 Working Group Meeting
October 29, 2001 at ITC**

Presentation Outline

- History of the WIR Tiger Team
 - Past activities and current focus

- Major Technical Activities since last ITC
 - P1500 System Chip SIL Connections: DAC 2001
 - TECS 2001 Paper by Lee and Mike:
“Tapping into IEEE P1500 Domains”

- Recent Status and Updates
 - Draft D0.5 updates

History of WIR Tiger Team

Past Activities and Current Focus

❑ Formed to specify the P1500 Wrapper Instruction Register (WIR)

- Mike, Fidel, Alan and Lee
- In addition to WIR Specification:
 - ✓ Specification of Wrapper Interface Port (WIP)
 - ✓ Specification of Wrapper Bypass Register (WBY)
 - ✓ SIL and TAP connections at System Chip Level

❑ Our work has been complete and stable for some time

- Initial specifications were developed by the Tiger Team and proposed to CTAG Task Force
- Authored WIP, WIR, WBY & SIL Connection sections in the P1500 Draft

❑ Focus is now on refinements to the WIR TT sections in the Draft

- Tiger Team has been in “hibernation” for some time
- Continue to work with CTAG Task Force to update our specifications

System Chip SIL Connections

Overview

□ Scope & Purpose of Specifications for SIL Connections

- CTAG specification is “Core Centric”
- Wanted to provide guidance at SoC level & for hierarchical cores
- Analogous to IEEE 1149.1 interconnection of TAPs at board level

□ P1500 System Chip SIL Connections

- See Chapter 12 in D0.5 Draft (also see DAC 2001 CTAG slides)
- SILs may be connected in a manner appropriate for the system chip design
- The only Rule is for serial connection of SILs:
 - ✓ SelectWIR must be common to all SILs when connected in series
 - ✓ It is Recommended that all WIP signals be connected in common
 - ✓ CTAG permits the WBY to be multiple bits
- What we support is a “design hierarchy” for CTAG cores
 - ✓ This is NOT support for a hierarchical P1500 protocol !
 - ✓ CTL needs to support this too, and we are working with them to assure this is ok

System Level TAP Controller Connection

□ Paper written by Lee and Mike was presented at TECS 2001

- Whetsel, Lee, and Ricchetti, Mike, “Tapping into IEEE P1500 Domains”, Digest of IEEE Testing Embedded Core-Based Systems (TECS) Workshop, April 2001, Marina Del Ray, CA.

□ Motivation and Objectives

- Wide industry adoption of 1149.1 TAP protocol for test, ISC, debug
 - ✓ 1149.1, 1149.4, 1532, IEEE-ISTO 5001 (Nexus), MIPS EJTAG, ...
 - ✓ Provides silicon to systems level reuse through a common protocol !
- Show compatibility of 1149.1 TAP, P1500 cores and TAPed Cores
 - ✓ How can we merge the three domains so they interoperate ?
- Explore tradeoffs, 1149.1 compliance issues, BSD/CTL considerations

□ This is a good start on solutions, and some of the issues

- Plans are to bring this into CTAG discussions in near future

P1500 and TAPed Core Example #1

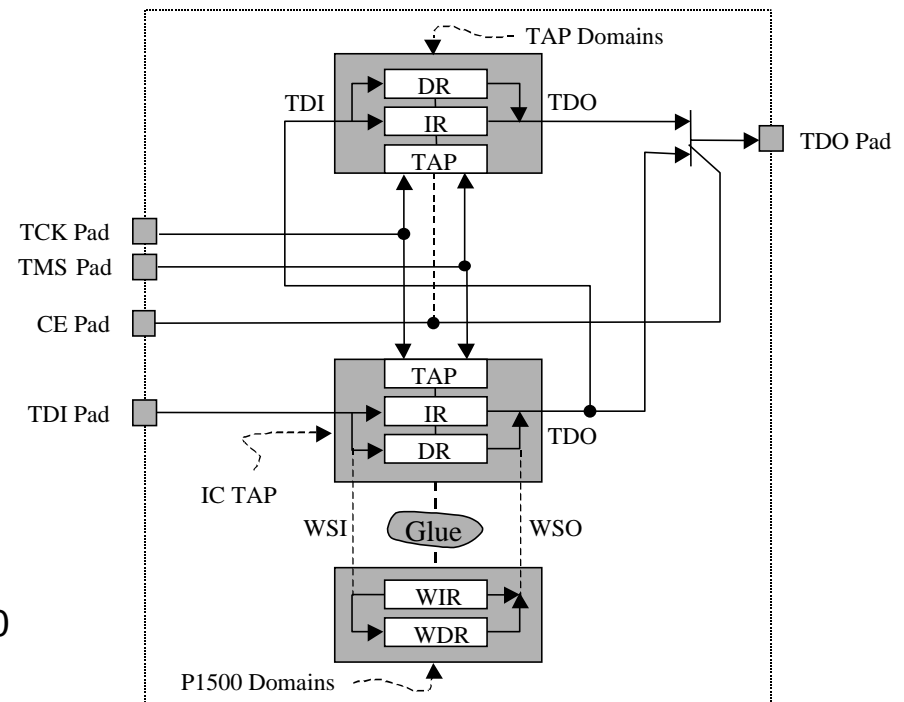
□ TAP + TAPed Core + P1500

- WIR and WDRs accessed as DRs using 2 TAP instructions
- IC + TAPed Cores are serially chained, and controlled by CE

□ WIR is controlled by the DR FSM States of the IC TAP

□ Violates .1 fixed length DR rules

- P1500 instructions should be private in IC BSDL ...
- Or have CE force Bypass in IC TAP for P1500 instructions



P1500 and TAPed Core Example #2

□ TAP + TAPed Core + P1500

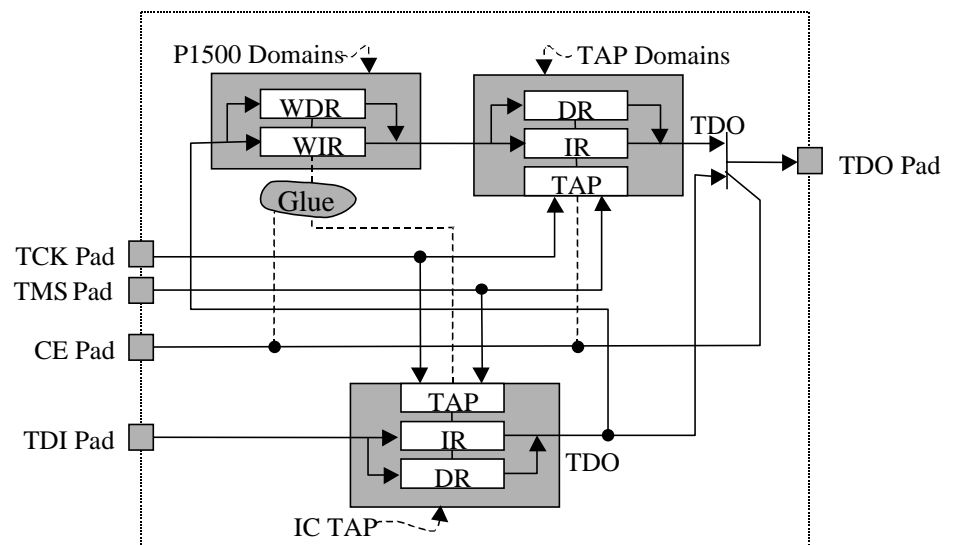
- IC + TAPed Cores + P1500 Cores are all serially chained, and controlled by CE

□ WIR is now controlled by IR FSM states of IC TAP

- Simultaneous Capture, Shift and Update of IRs and WIRs

□ No P1500 instructions in IC TAP !

- Always have fixed length DRs even if ~CE, since IR+WIR+IR



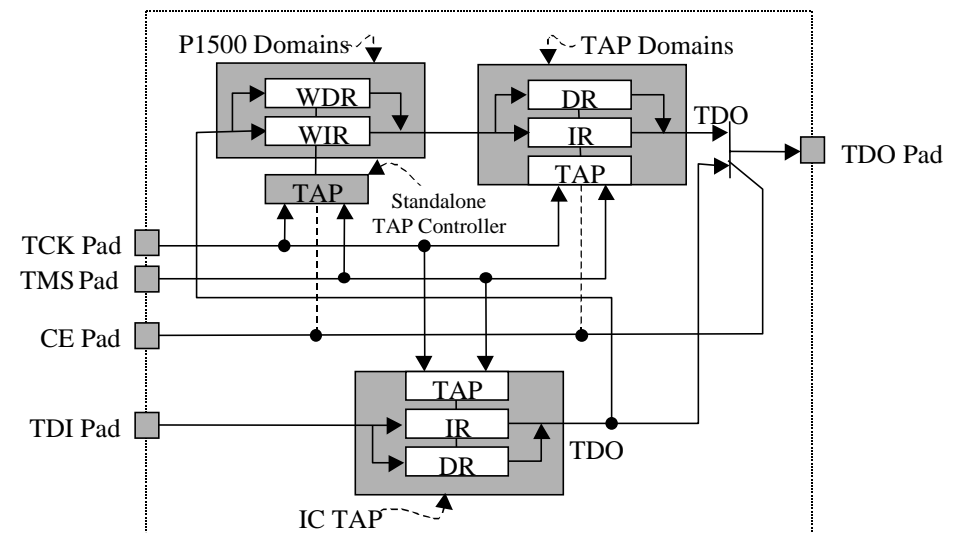
P1500 and TAPed Core Example #3

□ TAP + TAPed Core + P1500

- Serial chain, controlled by CE, as in Example #2

□ Standalone TAP added for P1500 Core Domain

- All P1500 Cores can be controlled by one, dedicated, TAP
- Eliminates P1500 Glue Logic interface in IC TAP



Recent Status and Update

Since DAC 2001

□ Updates to P1500 Draft D0.5:

- We received good written feedback on D0.4 Draft
 - ✓ Typos, grammar fixed
 - ✓ Removed references to “WART”
 - ✓ Changed WIP, WIR, WBY and SIL Connection figures to grayscale
 - ✓ WIR requires at least 2 bits (was 3), there are only 3 mandatory instructions
 - ✓ Now use only “Wrapper Bypass Register” and “WBY”
 - ✓ Added WSOR to figures and in Specifications & Descriptions text
 - ✓ Clarified that WIP section only defines terminals, not timing or protocol
 - ✓ Clarified use of Auxiliary Clock in WIP
 - ✓ Added WIP TransferDR terminal to figures, Specifications & Descriptions text
 - ✓ Added timing diagram for WIR Shift followed by WIR Update to help clarify existing timing Rules
 - ✓ Added Rule for common connection of SelectWIR when SIL are connected in series