

## Status Report

# P1500 Documentation Task Force

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Erik Jan Marinissen / P1500 DocTF / October 29, 2001

# Task Force Organization

- **Mission**

Produce first full draft document of P1500 standard for non-merged digital logic and memory cores

- **Target**

Document progress of technical Task Forces with at most one WG meeting delay

- **Members**

- Rohit Kapur (Synopsys)
- Erik Jan Marinissen\* (Philips Research)
- Nilanjan Mukherjee (Mentor Graphics)
- Mike Ricchetti (Intellitech)
- Jon Udell (Palmchip)

- **Meetings**

- Biweekly teleconference meetings of 1.5 hours  
Thanks to Mentor Graphics (Nilanjan) for providing facilities!
- Password-protected web site at IEEE computer

# Draft Releases

- P1500/D0.1 released January 31, 2000
- P1500/D0.2 released May 5, 2000 (VTS'00)
- P1500/D0.3 released January 4, 2001
- P1500/D0.4 released June 15, 2001 (DAC'01)
- P1500/D0.5 released October 29, 2001 (ITC'01)

## Distribution

- PDF document available at CTAG and CTL-TF password-protected web sites and via e-mail to Merged Cores TF
- Selected 'experts' (see under Review)

# IEEE P1500/D0.5 Disclaimers

- This is an unapproved draft of a proposed IEEE standard
- All text is preliminary and subject to change
- Certain sections are still empty
- This document cannot be well understood without proper introduction

In order not to create misunderstanding for those previously not involved in IEEE P1500 or for those unaware of the current status of IEEE P1500, we do not yet release this document to the general public!

# P1500/D0.5 Changes

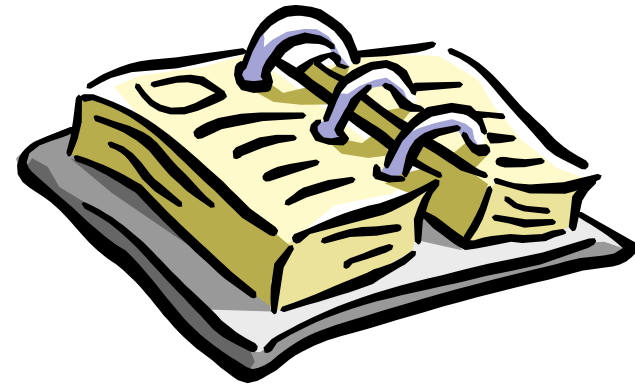
- Syntax and semantics definitions moved out to P1450.6
- No “Parts” hierarchy any longer, but continuous section- and page numbering (in line with IEEE guidelines)
- Technical updates in all sections of document
- Handling of editorial review comments
- Last-version check by DocTF team to get typos out

# Table of Contents P1500/D0.5

Title, Abstract, Key Words

Introduction, Participants, Acknowledgements,  
Table of Contents

1. Overview
2. References
3. Definitions, Acronyms and Abbreviations
4. Structure of This Standard
5. Dual Compliance Levels
6. Overview of Scalable Architecture Hardware
7. Wrapper Interface Port
8. Wrapper Instruction Register
9. Wrapper Bypass Register
10. WIR Instructions
11. Wrapper Boundary Register
12. P1500 System Chip Configuration
13. Compliance Definitions
- A. Glossary
- B. Bubble Diagram Definition



92 pages

# Review Procedures

- Since P1500/D0.3:  
Selected set of ‘external’ reviewers per document version
- Review comments of Working Group members are always welcome
  - Slight increase in Working Group review comments
- Since P1500/D0.4:  
We only accept review comments in MS-Excel for easy handling
  - Separation of editorial and technical comments
  - Handling in a subsequent version

# Review Template

Document Version	Reviewer	Comment Number	Comment Type	Page Number	Section Number / Paragraph number	Line Number in Draft	Comment	Recommended Changes	Resolution
D0.4									

# External Reviewers

- **P1500/D0.3**

- Ben Bennetts (Bennetts Associates) done
- Erica Cota + Luigi Carro (UFRGS / UCSD) done
- Paulo Prinetto (Politecnico di Torino) done
- Al Crouch (Motorola) done (D0.4)
- Pat McHugh (Lockheed Martin) not done

- **P1500/D0.4**

- Jürgen Alt (Infineon) done
- Hermann Obermeier (Infineon) done
- Frank Pöhl (Infineon) done
- Cheng-Weng Wu (Hsinchu University) done
- Gunnar Carlsson (Ericsson) done
- Samy Makar (Transmeta + VSIA) not done
- Greg Maston (Synopsys + IEEE1450) not done
- Gordon Robinson (3MTS) not done

# P1500 DocTF Continues...

- Continue biweekly teleconference meetings
- 'To Do' list:
  - Reviewer comments handling
  - Working together with technical Task Forces to complete texts
  - Writing of (currently missing) introductory texts