

Partial Wrapper: Figure 10.31

Rohit Kapur

```
Signals {
    IN0 In; T1 In; IO_FACE In; IN1 In;
    XFER In; SHFT In; CAPT In; WRCK In; MODE In;
    OUT Out; T0 Out;
}
SignalGroups {
    all[0..10]='IN0+T1+...+T0';
}
Variables {
    SignalVariable scaninvals[0..5];
    SignalVariable scanoutvals[0..5];
}

Timing { WaveformTable time {
    Period '100ns';
    all[0..10] { 01x { '0ns' D/U/N; }
    WRCK { P { '0ns' D; '50ns' U; '60ns' D; } }
}}

MacroDefs {
    setupMode { W time; V { IO_FACE=#; MODE=#; } }
    do_test_sa {
        W time;
        C { SHFT=1; XFER=0; CAPT=0; }
        Shift { V { T1='scaninvals[0..5]'; WRCK=P; } }
        V { SHFT=0; CAPT=1; WRCK=P; }
        C { SHFT=1; CAPT=0; }
        Shift { V { T0='scanoutvals[0..5]'; WRCK=P; } }
        V { WRCK=0; }
    }
}

ScanStructures scnchn {
    bdry {
        Length 6;
        ScanIn T1;
        ScanOut T0;
        ScanMasterClock WRCK;
        ScanEnable 'SHFT&~XFER&~CAPT';
        ScanCells c[0..5];
    }
}

PatternBurst B1 {
    PatList {
        P2;
        Stuck_at_tests;
    }
}

PatternExec E1 {
    PatternBurst B1;
}

Environment {
    CTL model {
        TestMode Normal;
    }
}
```

```

Internal {
    MODE { DataType TestMode {ActiveState D;}}
    `IN0+IN1+OUT' { DataType Functional; }
    WRCK { DataType Functional MasterClock;
          InputProperty Edge;}
    `XFER+SHFT+CAPT+IO_FACE+T1+T0' {DataType Unused;}
}
PatternInformation { Pattern P1 { Purpose EstablishMode;}}
}
CTL mode2 {
TestMode InternalTest;
Internal {
    `MODE+IO_FACE' { DataType TestMode {ActiveState U;}}
    `IN0+IN1' { DataType Functional Unused; }
    OUT { DataType Functional Unused;
         OutputProperty ScanUnstable;}
    WRCK { DataType TestClock ScanMasterClock CaptureClock
          {AssumedInitialState D;}
          InputProperty Edge;
          DriveRequirements {
            TimingSensitive {
              Period Min `100ns';
              Period Max `1000ns';
              Pulse High Min `10ns';}}
          }
    T1 {DataType TestData ScanDataIn;}
    T0 {DataType TestData ScanDataOut;
        LaunchClock WRCK LeadingEdge;}
    SHFT { DataType TestControl ScanEnable {ActiveState U;}}
    `XFER+CAPT' { DataType TestControl {ActiveState U;}}
}
PatternInformation {
    Pattern P2 { Purpose EstablishMode;}
    PatternExec E1 {Purpose Production;}
    Macro do_test_sa {
        Purpose DoTest; UseByPattern Scan; CycleCount 14;}
    Pattern stuck_at_tests {
        Purpose Scan;
        Fault {
            Type StuckAt;
            Boundary Primitive;
            FaultCount 299;
            FaultsDetected 295;
        }
        Macro do_test_sa;
        CycleCount 140;
    }
}
}
CTL mode3 {
TestMode ExternalTest;
DomainReferences { ScanStructures scnchn;}
Internal {
    MODE { DataType TestMode {ActiveState U;}}
    IO_FACE { DataType TestMode {ActiveState D;}}
    `IN0+IN1' { DataType Functional TestData;
              IsConnected In {
                StateElement Scan `c[1]+c[3]';
                IsEnabledBy `~a&b' {
                    a { Type Signal; Name XFER;}
                    b { Type Signal; Name CAPT;}
                }
                CaptureClock WRCK { LeadingEdge;

```

```

        StateAfterClock Connection;}
        Wrapper IEEE1500 CellID SC_SD2_CIO;
    }
}
OUT { DataType Functional TestData;
    IsConnected Out {
        StateElement Scan c[5];
        Wrapper IEEE1500 CellID SC_SD2_CIO;
        LaunchClock WRCK { LeadingEdge;
            StateAfterClock ExpectUnknown;}
    }
}
WRCK { DataType Functional TestClock ScanMasterClock
    CaptureClock {AssumedInitialState D;}
    InputProperty Edge;
    DriveRequirements {
        TimingSensitive {
            Period Min '100ns';
            Period Max '1000ns';
            Pulse High Min '10ns';}}
}
T1 {DataType TestData ScanDataIn {ScanDataType Boundary;}
    IsConnected In {
        Wrapper IEEE1500 CellID WC_SD2_CIO;
        IsEnabledBy 'a&~b&~c' {
            a { Type Signal; Name SHFT;}
            b { Type Signal; Name XFER;}
            c { Type Signal; Name CAPT;}
        }
    }
    Wrapper IEEE1500 PinID WSI;}
    CaptureClock WRCK { LeadingEdge; }
}
T0 {DataType TestData ScanDataOut {ScanDataType Boundary;}
    LaunchClock WRCK {LeadingEdge;}
    IsConnected Out {
        Wrapper IEEE1500 CellID WC_SD2_CIO;
    }
    Wrapper IEEE1500 PinID WSO;
}
SHFT { DataType TestControl ScanEnable {ActiveState U;}}
'XFER+CAPT' { DataType TestControl {ActiveState U;}
    DriveRequirements {
        TimingSensitive {
            Reference WRCK {
                ReferenceEdge Leading;
                Setup '10ns';
            }
        }
    }
}
}
}
PatternInformation {
    Pattern P3 { Purpose EstablishMode; }
}
}
}
Pattern P1 { Macro setupMode { IO_FACE=x; MODE=0;}}
Pattern P2 { Macro setupMode { IO_FACE=1; MODE=1;}}
Pattern P3 { Macro setupMode { IO_FACE=0; MODE=1;}}

```

```
Include file_stuck_at_tests IfNeed Patterns;
```