

WORKSHOP LOCATION

TECS 2000 will be held at the Omni Montreal Hotel, Montreal, Quebec, Canada, May 3-4, 2000, immediately following VTS 2000. Montreal is served by Montreal International Airport at Dorval located about 14 miles (22 km) west of downtown Montreal. It is approximately 25 minutes away from the city.

REGISTRATION

All Workshop participants require registration. Either register using the TECS 2000 Registration Form (<http://grouper.ieee.org/groups/1500/tecs/00/index.html>) or using the VTS 2000 Registration Form.

Early Registration*

IEEE/CS Member	\$210
IEEE Student Member	\$100
Non-Members	\$260

Registration at Hotel**

IEEE/CS Member	\$260
Student Member	\$110
Non-Members	\$320

* Discount Rates available until April 14

** Register at the VTS Registration Counter at the Omni Montreal Hotel.

Registration includes the welcome address, workshop technical sessions, workshop informal proceedings, evening reception, break refreshments, breakfast and lunch. Separate registration is required for all other VTS 2000 events.

HOTEL RESERVATIONS

To reserve a room at the hotel, please phone the hotel (+1-514-284-1110) and provide a credit card deposit. Identify the event by reservation code name **IEEE-VTS**. Deadline for reduced group rates is April 7, 2000. For more information on area hotels, please contact the TTTC Office (+1-540-937-8280).

INFORMATION

For more information on the Workshop, please check:

<http://grouper.ieee.org/groups/1500/tecs/00/index.html>

Or contact: Yervant Zorian, Phone: +1-408-453-0146,
Email: zorian@logicvision.com

Or contact the TTTC Office: IEEE TTTC, 1474 Freeman Dr, Amisville, VA 20106, USA . Phone: +1-540-937-8280, Fax: +1-540-937-7848, Email: tttc@computer.org

WORKSHOP COMMITTEE

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TECS 2000

4th IEEE International Workshop on Testing Embedded Core-based System-Chips

Omni Montreal Hotel
Montreal, Quebec, Canada
May 3-4, 2000

TECHNICAL PROGRAM

Sponsored by

*TTTC - The IEEE Computer Society
Test Technology Technical Council*

In Conjunction with

*VTS 2000 - The 18th IEEE VLSI Test
Symposium*

In Cooperation with

*VSIA - The Virtual Socket Interface Alliance
RAPID - Reusable Application-Specific
Intellectual Property Developers*

WORKSHOP SCOPE

Embedded cores, or pre-designed Intellectual Property (IP) blocks, are finding growing use in microelectronic system-chips. The increase in design reuse that core-based systems make possible adds to the complexity of testing the complete system-on-chip and even portions of it. TECS 2000 is the Workshop that dedicates its program to the state-of-the-art practices and emerging trends in testing embedded core-based system-chips. It brings together the core creators, integrators, manufacturers and ATE suppliers while providing an informal forum for presenting and discussing the new developments in testing such systems.

Yervant Zorian

WORKSHOP AT A GLANCE

WEDNESDAY, MAY 3, 2000

2:00 pm - 6:00 pm	Registration
4:00 pm - 4:45 pm	Opening Session
4:45 pm - 6:45 pm	Session 1: Current Practices in System-on-Chip Test
6:45 pm - 8:00 pm	Reception
8:00 pm - 9:30 pm	Panel Session: The Role for Academic Research in SOC Test

THURSDAY, MAY 4, 2000

7:00 am - 8:00 am	Continental Breakfast
8:00 am - 10:00 am	Session 2: New Approaches in Testing Embedded Cores
10:00 am - 10:30 am	Coffee Break
10:30 am - 12:30 pm	Session 3: Experiences in Testing Core-based Systems
12:30 pm - 2:00 pm	Lunch
2:00 pm - 4:30 pm	Session 4: Advanced Solutions for SOC Test and Verification

PROCEEDINGS

Informal Proceedings will be made available to all attendees. This will include extended abstracts, summaries or papers provided by authors based on their presentations.



WEDNESDAY, MAY 3, 2000

REGISTRATION 2:00 pm - 6:00 pm

OPENING SESSION 4:00 pm - 4:15 pm

Welcome Address

Y. Zorian, General Chair

Session 1: 4:15 pm - 6:45 pm
CURRENT PRACTICES IN SYSTEM-ON-CHIP TEST
Moderator: L. Whetsel - Texas Instruments

- 1.1 *Test Access Methodology for System-on-Chip Testing*, T.J. Chakraborty, C-H. Chiang - Bell Labs, Lucent Technologies
- 1.2 *A Practical DFT Strategy for a System-on-Chip*, N. H. Tan - Infineon Technologies
- 1.3 *Embedded Macro Test Support in IBM's Test Bench Tools*, B. Keller, R. Kerr, B. Koenemann, D. Pruden, R. Walther - IBM
- 1.4 *A Novel Approach for Designing Hierarchical Test Access Controller for Embedded Core Designs in a SOC Environment*, B. Dervisoglu - Intellitech, J. Swamy - Cadence
- 1.5 *Evaluating Different Approaches for Embedded and External Testing*, M. Lobetti-Bodoni - Siemens Information and Communication Networks, A. Benso, S. Di Carlo - Politecnico di Torino

Session 1 Discussion Panel:

D. Burek - LogicVision
R. Kapur - Synopsys
J. Udell - PalmChip

RECEPTION 6:45 pm - 8:00 pm

Panel Session: 8:00 pm - 9:30 pm
THE ROLE FOR ACADEMIC RESEARCH IN SOC TEST
Coorganized with:



Moderator: M. Chandramouli - Synopsys
Organizer: E.J. Marinissen - Philips Research
Panelists:

K. Chakrabarty - Duke University
S. Davidson - Sun Microsystems
S. Dey - UCSD
S. Gupta - USC
M. Lousberg - Philips
F. Muradali - Agilent
I. Phillips - ARM

THURSDAY, MAY 4, 2000

Continental Breakfast 7:00 am - 8:00 am

Session 2: 8:00 am - 10:00 am
NEW APPROACHES IN TESTING EMBEDDED CORES
Moderator: C. Papachristou - Case Western University

- 2.1 *On Design-for-Testability for Circuits Comprised of Non-Isolated Legacy Cores*, I. Pomeranz - University of Iowa, Y. Zorian - LogicVision
- 2.2 *On Using Golomb Codes and Internal Scan Chains for Test Data Compression / Decompression in a System-on-a-Chip*, A. Chandra, K. Chakrabarty - Duke University

- 2.3 *Test Information for Cores: Comparative Analysis and Recommendations*, M.D. Quasem, S. Gupta - University of Southern California

- 2.4 *Controllable LFSR for Embedded Core BIST*, D. Kay - Cisco Systems, S. Mourad - Santa Clara University

Session 2 Discussion Panel:

B. Keller - IBM
I. Kim - Lucent
S. Makar - Transmeta
M. Renovell - LIRMM

Coffee Break 10:00 am - 10:30 am

Session 3: 10:30 am - 12:30 am
EXPERIENCES IN TESTING REUSABLE CORE-BASED SYSTEMS

Moderator: T.W. Williams - Synopsys

- 3.1 *On-The-Shelf Core Pattern Methodology for Coldfile Cores*, T.L. McLaurin, J.C. Potter - Motorola
- 3.2 *Testing Embedded Synthesizable IP - A Case Study*, A. Burdass, G. Campbell, R. Grisenthwaite, R. York, G. Campbell - ARM
- 3.3 *HD2BIST: a Hierarchical Framework for BIST Scheduling, Data Patterns Delivering and Diagnosis in SOCs*, A. Benso, D. DiCarlo, S. Chiusano, P. Prinetto - Poticecnico di Torino, M. Spadari - LSI Logic, Y. Zorian - LogicVision
- 3.4 *Test Methodology Framework for Embedded Core Based Systems*, J. Abraham, N. Prasad, S. Chakravarthi, A. Bagwe, R. Parekhji - Texas Instruments

Session 3 Discussion Panel:

D. Bhattacharya - Texas Instruments
M. Ricchetti - Intellitech
S. Patil - Mentor Graphics

Lunch 12:30 pm - 2:00 pm

Session 4: 2:00 pm - 4:30 pm
ADVANCED SOLUTIONS FOR SOC TEST AND VERIFICATION
Moderator: T. Anderson - 0-in

- 4.1 *Application Specific DSP Functional Validation Methodology*, A. Daolio, F. Di Giovanni, S. Gazzaniga, G. Martinelli - ST Microelectronics
- 4.2 *Designer-Level Verification Using RuleBase*, F. Busaba, B. Banerjee, C. Krygowski - IBM
- 4.3 *Intellectual Property Protection Using Partially-Mergeable Cores*, V. Iyengar, M. Sugihara, H. Date, K. Chakrabarty - Duke University
- 4.4 *Effective Deterministic Arithmetic BIST Architecture for Embedded Processor Cores*, A. Paschalis - University of Athens, N. Kranitis - Demokritos, D. Gizopoulos - University of Piraeus, M. Psarakis - Demokritos, Y. Zorian, LogicVision
- 4.5 *Controlling the CAS-BUS TAM with IEEE 1149.1 TAP: A Solution for Systems on a Chip Testing*, W. Maroufi, M. Benabdenbi, M. Marzouki - LIP6/ ASIM Laboratory

Session 4 Discussion Panel:

H. Bederr - Texas Instruments
S. Bhawmik - Lucent
C.J. Clark - Intellitech
R. Gupta - UC Irvine