

6th IEEE International Workshop on Testing Embedded Core-based System-Chips

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Embedded cores, or pre-designed Intellectual Property (IP) blocks, are finding growing use in microelectronic system-chips. The increase in design reuse that core-based systems make possible, adds to the complexity of testing complete system-chips and even portions of them.

TECS 02 is the workshop that dedicates its program to the state-of-the-art practices and emerging trends in testing embedded core-based system-chips. It brings together core creators, integrators, manufacturers and ATE suppliers while providing an informal forum for presenting and discussing new developments in testing such systems. The topics of interest include, but are not limited to, the following:

- Automatic Test Generation for Embedded Cores**
- BIST for IPs and System-Chips**
- Core-level Design-for-Testability**
- Debug and Diagnosis for IP Cores**
- Fault Modeling and Simulation**
- Standard Test Solutions and IEEE P1500**
- Test Control Mechanisms for System-Chips**
- Verification and Validation for IPs**
- Wrappers and Test Access Mechanisms for Cores**

To present at the Workshop, authors are invited to submit paper proposals. The proposals may be extended abstracts (1,000 words) or full papers. Each submission should include: title, full name and affiliation of all authors, an abstract of 50 words, and keywords. Also, identify a contact author and include a complete correspondence address, phone number, fax number, and E-mail address. Submit six copies of your paper proposals by mail or Postscript version via E-mail. Proposals for panel discussions are also invited. Submissions are due no later than **March 2, 2002**.

Submit your paper proposal electronically to:

Yervant Zorian, LogicVision, E-mail: zorian@logicvision.com

Authors will be notified of the disposition of their papers by March 30th, 2002. Authors of accepted papers may submit an illustrated text April 13th for inclusion in the Digest of Papers, which will be provided to the attendees.

TECS 02 is sponsored by the **IEEE Computer Society Test Technology Technical Council (TTTC)** and in cooperation with **VSIA - The Virtual Socket Interface Alliance**. It is produced in conjunction with **VTS 02**

(For more information: <http://computer.org/tttc>)

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