17th IEEE VLSI TEST SYMPOSIUM
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17th IEEE VLSI Test Symposium
VTS 99
April 25th - 29th, 1999
Marriott Laguna Cliffs Resort
Dana Point, California, USA

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17TH IEEE VLSI TEST SYMPOSIUM (VTS 99) INTRODUCTION

You are invited to participate in the 17th IEEE VLSI Test Symposium. This document includes up-to-date information about the Symposium (Technical Program, Travel Information, and the technical events held in conjunction with VTS 99, including: TTTC Tutorials, TECS 99 and IDDQ 99 Workshops, Fringe and IEEE Standards meetings, etc). Also, please find attached the discount REGISTRATION FORMS and the HOTEL RESERVATION FORM. After filling out these forms please mail or fax them to guarantee your participation.

VTS 99 is the seventeenth in a series that explores the state-of-the-art and developing trends in the testing of electronic circuits and systems. The complexity of current generation ICs, combined with rapidly developing high density, high speed packaging and reduced design cycle time, has made it extremely difficult and expensive to comprehensively test electronic systems and diagnose failed parts using traditional methods. This situation will worsen as we move toward nanometer technologies. The reduced device geometries, increased operating speed and very low power supply levels, are reducing noise margins and component reliability, complicate defect behavior and increase the impact of timing, cross talk, transient, and other spurious faults. There is, therefore, a great need for innovative advances in test and diagnosis methodologies to cope with these problems. The theme of this year's symposium: "Scaling Deeper to Submicron: Test Technology Challenges" reflects some of these issues. Many creative and novel ideas and approaches to the current and future testing-related problems are explored and analyzed in the papers to be presented and discussed at VTS 99.

The two-and-a-half day technical program includes 62 paper presentations and 8 special sessions (panels, embedded tutorials, etc.). The paper sessions span many of the key areas in testing, such as BIST, Analog/Mixed-Signal Test, I_{DDQ} Test, On-Line Test and Fault Tolerance, Diagnosis, Validation/Verification, Scan and Boundary-Scan, Memory Test, Delay Test and ATPG. Also on the program are sessions on emerging areas that are gaining prominence, such as Testing Very-Deep Submicron Circuits, Defect Level Test, Testing High Speed Circuits, Core based System-On-Chip Test, MEMS Test, and High-level Test.

The keynote address and the invited presentation (see page 8) provide a glimpse of many issues that the testing community will need to address in the future.

The TTTC Tutorials and Education Group offers four full day tutorials in state-of-the-art topics in test through the Test Technology Education Program (see page 6). This provides opportunities for design and test professionals to update their knowledge-base in test, and earn official accreditation from TTTC. (Information for Tutorials 1 and 2 begins on page 7, and for Tutorials 3 and 4 on page 20 .)

Introduced for the first time this year, two popular TTTC workshops are held in conjunction with VTS 99. The first is the 3rd full day workshop on Testing Embedded Core-based System-Chips (TECS 99) and the second is a half day version of the IDDQ & Defect Based Testing Mini-Workshop (IDDQ 99). (For information on TECS 99 see page 23. For IDDQ 99 information, see page 25.) In addition, a number of standardization Working Groups and TTTC Fringe Technical Meetings will take place in conjunction with VTS 99 (see inside of back cover for a complete listing).

The social program (see page 22) provides an opportunity for closer interactions and informal technical discussions. This year the program includes a drive along the Pacific Coast Highway to Laguna Beach and Newport Beach, exploration of the colorful artist colony of Laguna Beach, and a dinner cruise on a luxury yacht along the California Riviera's coastline.

The improving quality, of submissions each year made paper selection a very difficult task. Sixty-two papers were selected for the final program in a rigorous review procedure, with over 200 reviewers worldwide, participating in the process. The Program Committee made the final cut in a video conference held simultaneously at four locations in the US, Canada and Europe. Over 35 program committee members attended this globally distributed meeting, which is one indicator of the true international nature of VTS.

The VLSI Test Symposium is the result of the work of many dedicated volunteers: reviewers, the Program Committee, Best Paper and Panel Award Judges, the Steering Committee, and the Organizing Committee. We wholeheartedly thank them all. We also wish to thank all the authors who submitted their work to VTS 99, and the program participants for their contribution at the symposium. Finally, we thank the IEEE Computer Society and its Test Technology Technical Council for their continued sponsorship and support.

We hope that you will find VTS 99 interesting, thought-provoking, rewarding, and fun.

Michael Nicolaidis
General Chair
michael.nicolaidis@imag.fr

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Program Chair
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17TH IEEE VLSI TEST SYMPOSIUM GENERAL INFORMATION

All activities require a registration badge for admittance. All participants must pay the appropriate fees. Reduced fees are available to IEEE or Computer Society members on presentation of a valid member number.

To register, use the Symposium Registration Form in the center of this booklet. To receive **early registration discount rates**, your completed Registration Form must be RECEIVED in the VTS office by mail or fax by **APRIL 13, 1999.**

After April 13, register at the higher rates listed in the table below. After April 13, SPACE IS NOT GUARANTEED in the Social Program.

Technical program registration includes a copy of the Proceedings, the social program, two luncheons, three continental breakfasts, and five coffee breaks. *Student registration does not include the social program.* (See page 22 for Social Program information.) Students and companions of registered attendees can buy tickets for social program at $90 per person. Extra copies of the Proceedings are available at $45 each. Lunch tickets for companions of registered attendees will be available at the symposium ($30 each).

The Registration Form allows you to automatically enroll or renew your TTTC membership (no dues or fees). Check the corresponding box.

The TECS 99 program begins on Wednesday, April 28th at 4:00 pm with an Opening Session, followed by an evening reception and panel session. Then on Thursday, TECS continues with sessions from 8:00 am to 4:30 pm. TECS 99 registration includes digest of papers, evening reception, breaks, and lunch. (See page 23 for detailed information.)

IDDQ 99 will take place Saturday, April 25th from 4:30 pm to 9:30 pm. Registration includes workshop technical sessions, workshop informal proceedings, break refreshments and dinner. (See page 25 for detailed information.)

VTS allows you to obtain a half year subscription (July to December 1999) to IEEE Design & Test of Computers, if you select to embed it in your Registration Form. The fee is $16 for IEEE Computer Society members, $8 for IEEE/CS Student Members, and $45 for non-members. (See page 26 for more information.)

Tutorial registration for members and non-members includes lecturer's notes, breaks, and lunch.

17TH IEEE VLSI TEST SYMPOSIUM GENERAL INFORMATION (Continued)

REGISTRATION FEES:

Early Registration*	SYMPOSIUM	TUTORIAL	TECS	IDDQ
IEEE/CS Member	$395	$285	$210	$90
Student Member	$125	$110	$100	$70
Non-Members	$495	$350	$260	$115
Registration at Hotel	**SYMPOSIUM**	**TUTORIAL**	**TECS**	**IDDQ**
IEEE/CS Member	$470	$335	$260	$110
Student Member	$200	$130	$110	$85
Non-Members	$595	$395	$320	$140

Social Program Fee** - $90

**discounts available until April 13, 1999*
***for students and companions of registered attendees*

REFUNDS: If you must cancel, advance registration fees will be refunded only upon written request to: VLSI Test Symposium, 1474 Freeman Drive, Amissville, VA, 20106, USA postmarked on or before April 13, 1999. A $50 processing fee is charged for each refund.

IEEE VLSI TEST SYMPOSIUM is sponsored by the IEEE COMPUTER SOCIETY Test Technology Technical Council (TTTC).

The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members' professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology.

TTTC is a prime source of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters and electronic broadcasts. All its activities are led by volunteer members.

TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level. You may enroll as TTTC member for 1999 (no dues or fees) by using the embedded VTS 99 Registration Form. To learn more about TTTC offerings and membership benefits, please visit: http://computer.org/tttc

IEEE VLSI TEST SYMPOSIUM TRAVEL INFORMATION

AIR

The Marriott's Laguna Cliffs Resort is served by Los Angeles LAX, San Diego International, Long Beach, and Orange County/John Wayne airports.

DISCOUNT AIRFARE!!

VLSI Test Symposium is pleased to announce that it has been able to secure a special discount agreement with United Airlines unavailable to the general public.

United Airlines is the official airlines of the 1999 VLSI Test Symposium. If you or your travel agent call United's toll-free number (**1-800-521-4041**) to book your reservations, you will receive a 5% discount off the lowest applicable discount fare, including First Class, or a 10% discount off full fare unrestricted coach fares, purchased 7 days in advance. An additional 5% discount will apply when tickets are purchased at least 60 days in advance of your travel date. Discounts also apply on Shuttle by United and United Express. Call United's specialized Meeting Reservation Center at 1-800-521-4041 to obtain the best fares and schedule information. Make sure to refer to **Meeting ID Number 542ZF**. Dedicated reservationists are on duty 7 days a week from 7:00 AM to 12:00 midnight EST. Mileage Plus members receive full credit for all miles flown to this meeting.

Book early to take advantage of the promotional fares that give you the greatest discount!

AIRPORT GROUND TRANSPORTATION

The **SuperShuttle** serves LAX and Orange County/John Wayne airports. Fare from LAX is $51 one way and $9 each additional person. Fare from Orange County/John Wayne is $26 one way and $9 for each additional person. Travel time from LAX is approximately 1 1/2 - 2 hours and from Orange County it is approximately 30 minutes. For reservations and information, call (714) 517-6600.

The SuperShuttle also serves Long Beach airport. Fare is $45 one way and $9 for each additional person. Travel time is approximately 1 hour. For reservations and information, call (310) 782-6600.

AUTOMOBILE

If you prefer to drive, major car rental agencies are located at the airports.

REACHING THE *MARRIOTT LAGUNA CLIFFS RESORT* BY CAR

From **LAX** and **Orange County/John Wayne Airports:**

1. Take the **405 Freeway South** (which merges into the **5 South)**.

(Continued on page 6)

IEEE VLSI TEST SYMPOSIUM TRAVEL INFORMATION (Continued)

From LAX and Orange County/John Wayne Airports (Cont.)

2. Travelling past Mission Viego and San Juan Capistrano, exit **Pacific Coast Highway** to the **North** (Right).
3. Proceed 2 sets of stoplights to **Dana Point Harbor Drive** and turn left.
4. Proceed a short block to the next stoplight and turn right onto **Street of the Park Lantern**.
5. Proceed to the top of the hill and enter the Resort's property.

From the **SAN DIEGO AIRPORT:**

1. Take the **5 Freeway North**.
2. Shortly after passing the city of San Clemente, exit at **Beach Cities (Highway 1)** to the **North** (Left).
3. Proceed 2 sets of stop lights to **Dana Point Harbor Drive** and turn left.
4. Follow directions above, numbers 4 and 5.

HOTEL INFORMATION

The 17th IEEE VLSI Test Symposium will be held at Marriott Laguna Cliffs Resort, Dana Point, California, USA. The Marriott is located an hour from Los Angeles and San Diego, surrounded by 42 acres of lush landscaping, and situated on a bluff overlooking both the 2,500 yacht slip Dana Point Harbor and 10 miles of white sandy beach.

To reserve a room at the hotel, please mail or fax the hotel reservation form (on the other side of this page) or phone the hotel by April 2, 1999, to obtain the special room rates listed on the form. These rates will also apply from three (3) days before to three (3) days after the official dates of the Symposium, subject to availability of guest rooms.

After April 2, 1999, reservation will be taken if space is available, however, rates may be higher.

The hotel accepts reservation by phone with a credit card deposit. Identify the symposium by the reservation code name **IEEE-VTS**, to receive the symposium rate.

MAIL or PHONE Hotel Reservation to:
Marriott Laguna Cliffs Resort
25135 Park Lantern
Dana Point, CA 92629, USA
Tel: +1 (949) 661-5000, +1 (800) 533-9748
Fax: +1 (949) 661-5358
Code: IEEE-VTS

To cancel hotel reservations and receive a refund, you must notify the hotel at least 48 hours before your scheduled arrival time.

For more information on area hotels, please contact the TTTC Office: +1 (540) 937-8280.

TEST TECHNOLOGY EDUCATION PROGRAM

The TTTC Tutorials and Education Group has started a comprehensive Test Technology Educational Program (TTEP). Starting in 1999, this program provides opportunities for design and test technology professionals to update and expand their knowledge-base in test technology, and earn official certification from the IEEE TTTC, upon the completion of four full day tutorials units offered by TTEP.

The Test Technology Educational Program schedule for 1999 includes (but is not limited to) tutorial units presented at the following TTTC Technical Meetings:

- VLSI Test Symposium (VTS), Dana Point, CA, USA, April 25 and April 29.
- European Test Workshop (ETW), Constance, Germany, May 25.
- International Test Conference (ITC), Atlantic City, NJ, USA, September 26 and 27.
- DFT Symposium, Albuquerque, NM, USA, October 31.
- Asian Test Symposium (ATS), Shanghai, China, November 16.

Sunday, April 25th, 1999
TUTORIALS

VLSI Test Symposium is pleased to present four tutorials on topics of current interest to symposium attendees. All four tutorial units are part of TTEP and hence qualify for IEEE TTTC certfication. Two tutorials are held on Sunday, April 25th, and two on Thursday, April 29th. Each tutorial requires a separate fee and registration (see General Information). For further information about the tutorials contact either:
Anand Raghunathan
Tel: +1-609-951-2967
E-mail: anand@ccri.nj.nec.com or
Joan Figueras
Tel: +34-3-401-6603
E-mail: figueras@eel.upc.es.

7:30 - 8:30 am Tutorial Registration, Coffee Service

8:30 am - 4:30 pm
Salon 1 & 2

TUTORIAL 1: **Testing Embedded-Core Based System Chips**
Presenters:
Erik Jan Marinissen - Philips Research
Yervant Zorian - LogicVision, Inc.

(Continued on page 8)

Sunday, April 25th, 1999
TUTORIALS (Continued)

AUDIENCE: IC designers, test engineers, and their managers, but also (academic) researchers, test methodology developers, and test tool developers.

DESCRIPTION: Advances in semiconductor process and design technology enable the design of complex systems-on-chips. Traditional IC design, in which every circuit is designed from scratch and reuse is limited to standard-cell libraries, is more and more replaced by a design style based on embedded large reusable modules, the so-called cores. This core-based design style poses a series of new challenges, especially in the test domain. Therefore, testing of embedded cores is one of the current Hot Topics in the international test community.

This tutorial provides an introduction into core-based design and test, and an overview of current academic and industrial practices in core test. The current status of industry-wide efforts and standardization in VSIA and IEEE P1500 is discussed. The main modules of the tutorial are (1) Challenges in Embedded-Core Test, (2) Conceptual Architecture for Core Test Access, (3) Industry-Wide Effort, (4) SOC Test Tools and Flows, and (5) Industrial Experiences.

8:30 am - 4:30 pm
Salon 3

TUTORIAL 2: **Recent Advances in BIST Technology**
Presenter:
Jacob Savir - New Jersey Institute of Technology

AUDIENCE: Practitioners, managers and students who wish to learn about the state of the art in BIST technology.

DESCRIPTION: Don't assume you already know everything about BIST... The field is rapidly changing and you cannot afford to remain uninformed. Supplement your knowledge by joining your peers in learning about new advances in BIST.

This tutorial addresses state-of-the-art research and development in BIST. Topics include: diagnostic aids for signature test, random testing of coupled-cell and pattern-sensitive faults in RAMs, an improved cutting algorithm, statistical resistance to detection, partitioning of logic for self-test, multiple-seed LFSRs, syndrome test, AC test, and more.

Information for Tutorials 3 & 4 begins on page 20.

Session 4 (Continued)

4.2 *Time Redundancy Based Soft-Error Tolerance to Rescue Nanometer Technologies*, M. Nicolaidis - TIMA

4.3 *Test Generation for Ground Bounce in Internal Logic Circuitry,* Y.S. Chang, S.K. Gupta, M.A. Breuer - Univ. of Southern California

2:30 -2:50 pm BREAK

2:50 - 3:50 pm Salon 1

Session 5: **ADVANCED SCAN PATH TECHNIQUES**
Moderators: K. Ruparel - Cisco
V. Chickermane - IBM

5.1 *Advanced Synchronous Scan Test Methodology,* J. Schmid, J. Knaeblein - Lucent Technologies

5.2 *Scan Vector Compression/Decompression Using Statistical Codes,* A. Jas, J. Ghosh-Dastidar, N.A. Touba - Univ. of Texas, Austin

5.3 *Partial Scan Using Multi-Hop State Reachability Analysis,* S. Sharma, M.S. Hsiao - Rutgers Univ.

2:50 - 3:50 pm Salon 3

Session 6: **I_{DDQ} TESTING**
Moderators: C. Hawkins - Univ of New Mexico
J. Segura - Univ Illes Balears

6.1 *Extending the Pseudo-Stuck-At Fault Model to Provide Complete I_{DDQ} Coverage*, Robert C. Aiken - Hewlett Packard

6.2 *Built-In Current Sensors for I_{DDQ} Testing in Deep Submicron*, T. Calin, L. Anghel, M. Nicolaidis - TIMA

6.3 *On the Comparison of Delta I_{DDQ} and I_{DDQ} Testing,* C. Thibeault - Ecole de Technologie Superieure

3:50 - 4:10 pm BREAK

17TH IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Monday, April 26th, 1999

4:10 - 5:30 pm Salon 1

Session 7: **DELAY FAULT TESTING**
Moderators: J. Aylor - Univ of Virginia
A. Pramanick - Advantest

7.1 *A Flexible Path Selection Procedure for Path Delay Fault Testing*, I. Pomeranz, S.M. Reddy - Univ. of Iowa

7.2 *Delay Fault Testing of Designs with Embedded IP Cores,* H. Kim, J.P. Hayes - Univ. of Michigan

7.3 *Adaptive Techniques for Improving Delay Fault Diagnosis,* J. Ghosh-Dastidar, N.A. Touba - Univ. of Texas, Austin

7.4 *On n-Detection and Variable n-Detection Test Sets for Transition*, I. Pomeranz, S.M. Reddy - Univ. of Iowa

4:10 - 5:30 pm Salon 3

Session 8: **VALIDATION, VERIFICATION AND DIAGNOSIS**
Moderators: D. Pradhan - Texas A&M Univ
D. Wu - Intel

8.1 *A New Coverage Metric for Validation and Test,* P.A. Thaker, V.D. Agrawal, M.E. Zaghloul - Hughes Network Systems, Bell Labs, & George Washington Univ.

8.2 *Verification of Processor Microarchitectures,* J. Shen, J.A. Abraham - Univ. of Texas, Austin

8.3 *Techniques to Encode and Compress Fault Dictionaries,* S. Chakravarty, Vinodh Gopal - Intel & Compaq

8.4 *Implication and Evaluation Techniques for Proving Fault Equivalence,* M.E. Amyeen, W.K. Fuchs, I. Pomeranz, V. Boppana - Purdue Univ., Univ. of Iowa, & Fujitsu Labs

8:00 - 9:30 pm Salon 3

OPEN MICROPHONE SESSION: **WHEN WILL WE GET AROUND TO TESTING PROPERLY?**
Moderator: A. Ambler - Univ of Texas, Austin

8:00 - 9:30 pm Salon 1

SPECIAL SESSION 1: **THE END OF MOORE'S LAW ERA?**

Coorganized with:

Moderator: Y. Zorian - LogicVision
Embedded Presentation: W. Maly - CMU

PANELISTS:
- B. Bottoms - HPL
- M. d'Abreau - Level One
- H. de Man - IMEC
- D. Gajski - UC Irvine
- E. White - Lehman Brothers

Tuesday, April 27th, 1999

8:30 - 9:30 am Salon 1

Session 9: **MIXED SIGNAL TESTING**
Moderators: G. Roberts - McGill Univ
A. Osseiran - Ecole d'Ingenieurs de Geneve

9.1 *Efficient Test Generation for Transient Testing of Analog Circuits Using Partial Numerical Simulation,* P. Variyam, J. Hou, A. Chatterjee - Georgia Inst. of Technology

9.2 *Specification Back-Propagation and its Application to DC Fault Simulation for Analog/ Mixed-Signal Circuits,* J.L. Huang, C.Y. Pan, K.T. Cheng - Univ. of California, Santa Barbara

9.3 *Test Metrics for Analog Parametric Faults,* S. Sunter, N. Nagi - LogicVision

8:30 - 9:30 am Salon 3

Session 10: **BIST**
Moderators: S. Wu - Lucent Bell Labs
D. Burek - LogicVision

10.1 *Comparative Study of CA-Based PRPGs and LFSRs with Phase Shifters,* J. Rajski, G. Mrugalski, J. Tyszer - Mentor Graphics & Poznan Univ. of Technology

(Continued on page 14)

Session 10 (Continued)

10.2 *An Efficient BIST Method for Small Buffers,* W.B. Jone, D.C. Huang, S.C. Wu, K.J. Lee - Natl. Chung Cheng Univ. & Natl. Cheng-Kung Univ.

10.3 *An Effective BIST Architecture for Sequential Fault Testing in Array Multipliers,* M. Psarakis, A. Paschalis, D. Gizopoulos, Y. Zorian - NCSR "Demokritos" & LogicVision

9:30 - 9:50 am BREAK

9:50 - 10:50 am Salon 1

Session 11: **ATPG RELATED APPROACHES**
Moderators: J. Sprock - Synopsys
R. Makki - Univ of North Carolina

11.1 *A Fault Simulation Based Test Pattern Generator for Synchronous Sequential Circuits,* R. Guo, I. Pomeranz, S.M. Reddy - Univ. of Iowa

11.2 *PEDO - Probabilistic Excitation and Deterministic Observation - First Commercial Experiment,* M.R. Grimaila, J. Dworak, M.R. Mercer, S. Lee, K.M. Butler, B. Stewart, H. Balachandran, B. Houchins, V. Mathur - Texas A&M Univ. & Texas Instruments

11.3 *New Theorems for Identifying Undetectable and Redundant Faults,* S.M. Reddy, I. Pomeranz, N.Z. Basturkmen, X. Lin - Univ. of Iowa & Mentor Graphics

9:50 - 10:50 am Salon 3

Session 12: **TESTING MEMS, MCM AND ANALOG CIRCUITS**
Moderators: D. Keezer - Georgia Tech
T. Storey - Lockheed Martin

12.1 *A Novel Test Methodology for MEMs Magnetic Micromotors,* B.C. Kim, K. Marella - Michigan State Univ.

12.2 *A New Bare Die Test Methodology,* Z. Yang, K.T. Cheng, K.L. Tai - Silicon Graphics, Univ. of California, Santa Barbara & Lucent

12.3 *Hierarchical Test Generation for Analog Circuits Using Incremental Test Development,* R. Voorakaranam, A. Chatterjee - Georgia Inst. of Technology

Session 15 (Continued)

15.2 *Programmable Embedded Self-Testing Checkers for All-Unidirectional Error-Detecting Codes,* A.P. Stroele, S. Tarnick - Univ. of Karlsruhe & SATCON GmbH

15.3 *Weight-Based Codes and Their Application to Concurrent Error Detection of Multilevel Circuits,* D. Das, N.A. Touba - Univ. of Texas, Austin

9:00 - 10:00 am
Salon 3

Session 16: **MEMORY TEST**
Moderators: C-W. Wu - Tsing Hua Univ
V. Castro Alves - Univ Federal Rio de Janeiro

16.1 *Maximal Diagnosis of Interconnects of Random Access Memories,* J. Zhao, F.J. Meyer, F. Lombardi - Texas A&M Univ. & Northeastern Univ.

16.2 *Error Detecting Refreshment of Embedded DRAMs*, S. Hellebrand, H.-J. Wunderlich, A. Ivaniuk, Y. Klimets, V.N. Yarmolik - Univ. of Stuttgart & Belarussian State Univ. of Informatics and Radioelectronics

16.3 *A New Framework for Automatic Generation, Insertion, and Verification of Memory Built-In Self Test Units*, K. Zarrineh, S.J. Upadhyaya - IBM & SUNY Buffalo

10:00 - 10:20 am BREAK

10:20 - 11:20 am
Salon 1

Session 17: **BIST RELATED APPROACHES**
Moderators: R. David - Lab d'Automatique de Grenoble
Z. Peng - Linkoping Univ

17.1 *TAO-BIST, A Framework for Testability Analysis and Optimization of RTL Circuits Using BIST,* S. Ravi, N.K. Jha, G. Lakshminarayana - Princeton Univ. & NEC USA

17.2 *A Test Vector Inhibiting Technique for Low Energy BIST Design,* P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch - LIRMM

(Continued on page 18)

17TH IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Wednesday, April 28th, 1999

Session 17 (Continued)

17.3 *Enhanced BIST-Based Diagnosis of FPGAs via Boundary Scan Access,* C. Stroud, S. Wijesuriya, C. Hamilton, G. Gibson - Univ. of Kentucky

10:20 - 11:20 am
Salon 3

Session 18: **DEFECT ORIENTED TEST**
Moderators: Y. Malaiya - Colorado State Univ
A. Benso - Poli di Torino

18.1 *Analyzing the Need for ATPG Targeting GOS Defects*, E. Isern, M. Roca, J. Segura - Univ. Illes Balears

18.2 *On the Evaluation of Arbitrary Defect Coverage of Test Sets,* A. Jain, M. Hsiao, V. Boppana, M. Fujita - Rutgers Univ. & Fujitsu Labs

18.3 *Defect-Oriented Test Scheduling,* W. Jiang, B. Vinnakota - Univ. of Minnesota

11:20 - 11:40 am BREAK

11:40 am - 12:40 pm
Salon 1

Session 19: **ON-LINE TESTING AND FAULT TOLERANCE**
Moderators: M Bayoumi - Univ of Southwestern Louisiana
R. Karri - Polytechnic Univ

19.1 *A New Fault -Tolerance Technique for Cache Memories,* P.P. Shirvani, E.J. McCluskey - Stanford Univ.

19.2 *Low-Cost On-Line Test for Digital Filters,* I. Bayraktaroglu, A. Orailoglu - Univ. of California, San Diego

19.3 *Evaluating the Fault Tolerance Capabilities of Embedded Systems via BDM,* M. Rebaudengo, M. Sonza Reorda - Politecnico di Torino

11:40 am - 12:40 pm
Salon 3

Session 20: **DFT AND BOUNDARY SCAN**
Moderators: S. Mourad - Santa Clara Univ
A. Orailoglu - UC San Diego

20.1 *An Automated Procedure for DFT of State Holding Cells,* J. Xu, R. Kundu, F.J. Ferguson - Univ. of California, Santa Cruz

(Continued on page 19)

Thursday, April 29th, 1999
TUTORIALS (Continued)

8:30 am - 4:30 pm
Salon 3

TUTORIAL 4: **IC Techiques for Mixed-Signal DFT and BIST**
Presenter:
Stephen Sunter - LogicVision, Inc.

AUDIENCE: IC design-for-test engineers, ATE designers, technical managers in related fields, and post-graduate students researching BIST. A rudimentary understanding of mixed-signal IC design or test is assumed.

SUMMARY: SOCs require more re-use of circuits and their tests, with decreasing access. As BIST for digital circuits grows in popularity, BIST for mixed-signal is becoming a reality and a necessity. This tutorial first reviews criteria for evaluating mixed-signal DFT and BIST techniques, including analog fault coverage. Practical mixed-signal DFT techniques are reviewed, followed by a detailed discussion of the IEEE P1149.4 mixed-signal standard test bus, focusing on analog aspects of its design and use. Lastly, we discuss the key principles and techniques of 'industrial strength' BIST circuits which cost-effectively implement time-domain, functional tests in ICs that need not contain a DSP. Attendees will learn various ways to achieve BIST accuracy greater than that of the circuit-under-test.

OBTAIN CURRENT INFORMATION ON VTS 99 FROM:

IEEE VLSI Test Symposium
1474 Freeman Drive
Amissville, VA 20106
USA
Tel: +1 (540) 937-8280
Fax: +1 (540) 937-3739
Email: tttc@computer.org

WWW Site:
http://www.computer.org/tab/tttc/meetings/vts/home.html

17TH IEEE VLSI TEST SYMPOSIUM
SOCIAL PROGRAM

SOAK UP THE BEAUTIFUL SUNSET AS WE CRUISE THE PACIFIC RIVIERA

This year's social program has it all. Join us as we drive along the Pacific Coast Highway to Laguna Beach, California's colorful artist colony. You'll have time to explore it's unique galleries, boutique shops, cafés, and beach in this charming European style village. Then we travel north along the Pacific Coast Highway to Newport Beach and the famous California Riviera. You'll experience first-hand the lifestyle of the rich and famous, as we board a luxury yacht, the “Dream On”, for a three-hour dinner cruise that's sure to include a breathtaking sunset and beautiful vistas of the California Riviera's coastline.

The informal setting of the social program adds another dimension to the symposium, accentuating the technical discussions and providing an opportunity for closer interactions and relaxation.

Busses will leave the Marriott Laguna Cliffs Resort at 3:30 pm and return at approximately 10:30 pm.

There is no extra cost for this program for VTS attendees who register at member and non-member rates. Students and companions of VTS attendees can register for the Social Program for $90 per person. To guarantee your participation in this program you must register before April 13, 1999.

ABOUT DANA POINT AND SURROUNDING AREAS

On the Pacific Riviera, just south of California's renowned Artists' colony of Laguna Beach, is beautiful Dana Point, named for Richard Henry Dana, the author who described this spectacular seaside location as "the most romantic spot on the California coast". Nestled atop the bluffs of the unparalleled California coastline, Marriott's Laguna Cliffs Resort at Dana Point soars above lush green landscapes, miles of white sandy beach, and the azure seas of the Pacific. The Resort is located just minutes from Laguna Beach, San Clemente, Doheny Beach, Mission San Juan Capistrano, and within walking distance to shops and the old Mariner's Village.

3rd IEEE International Workshop on Testing Embedded Core-Based System-Chips TECS 99

April 28th - 29th, 1999

After two successful TECS workshops held in conjunction with ITC/Test Week in 1997 and 1998, TECS 99 moves out of Washington, D.C. to colocate with VTS 99 and be closer to the semiconductor industry in silicon valley.

SCOPE: As the use of embedded cores is growing in today's ICs, the complexity of creating an effective test for the individual cores and system-on-chip keeps increasing. TECS 99 is the only workshop to dedicate its entire program to the emerging trends and methods in testing embedded core-based system-chips. TECS brings together the IP core creators, core users, EDA providers, system-on-chip manufacturers and ATE providers.

AUDIENCE: Test engineers, designers, managers and researchers who are interested in learning about the state-of-the-art in testing complex system-on-chips.

TECS 99 AT A GLANCE: The TECS 99 Program Committee has selected topics of current interests and relevance:

Wednesday, April 28, 1999

4:00 pm - 4:45 pm	Opening Session
4:45 pm - 6:45 pm	Session 1: Current Practices in System-on-Chip Test
6:45 pm - 8:00 pm	Evening Reception
8:00 pm - 9:30 pm	Panel Session: CAD Tools for Core Test

Thursday, April 29, 1999

8:00 am - 10:00 am	Session 2: New Approaches in Testing Embedded Cores
10:00 am- 10:30 am	Break
10:30 am - 12:30 pm	Session 3: Experiences in Testing Embedded Core-Based Systems
12:30 pm - 1:30 pm	Lunch
1:30 pm - 2:30 pm	Invited Session: VSIA Manufacturing Test DWG
2:30 pm - 4:30 pm	Session 4: Advanced Solutions for SOC Test and Verification

PAPER PRESENTATIONS: All five sessions at TECS 99 are comprised of paper presentations followed by dedicated

(Continued on page 24)

3rd IEEE International Workshop on Testing Embedded Core-Based System-Chips TECS 99 (Continued)

discussion panels to conclude the sessions with recommendations and roadmaps.

KEYNOTE: TECS 99 starts with a keynote address by Rene Segers, Philips Semiconductors, entitled “Philips’ Experience in Core-Based Design and Test of System ICs.”

PANEL SESSION: TECS 99 for the first time features a full length panel session on "CAD Tools for Core Testing" is introduced at TECS 99 followed by tool demos. The panelists represent commercial EDA tool vendors, users, and internal tool providers. This panel is co-organized with IEEE Design & Test of Computers.

IEEE P1500 (Embedded Core Test Standard): The P1500 Working Group will hold its periodic meeting in conjunction with TECS 99 immediately following the workshop. The P1500 WG meeting schedule is held in two parts:

Part 1: Thursday, April 29, 5:00 pm - 8:00 pm
Part 2: Friday, April 30, 9:00 am - 12:00 pm

No registration is required to attend IEEE P1500 WG meeting.

REGISTRATION: All TECS 99 participants require registration, which includes workshop technical sessions, workshop informal proceedings, the evening reception, break refreshments, breakfast, and lunch. Register using the enclosed VTS 99 Registration form.

SPONSORSHIP: TECS 99 is sponsored by the IEEE Computer Society Test Technology Technical Council and is in cooperation with Virtual Socket Interface Alliance (VSIA).

INFORMATION: For the full TECS 99 program check:
http://grouper.ieee.org/groups/1500/tecs/99/

For further information contact the General Chair:
Yervant Zorian, LogicVision (*zorian@lvision.com*)

5th IEEE International Mini-Workshop on IDDQ and Defect Based Testing
IDDQ 99
April 25th, 1999

The I_{DDQ} testing workshop series has focused on various aspects of I_{DDQ} and defect based test methods. These test methods continue to offer challenges and opportunities as technology moves into deep sub-micron. This is the first time this mini-workshop will be organized in conjunction with the VLSI Test Symposium. The workshop will have a short format for 1999. This workshop will feature a number of invited speakers who are well known experts in I_{DDQ} and defect based test methods. The organizing committee has selected topics of current interest and relevance. These include:

1. Viability of current tests in Deep sub-micron
2. Defect oriented testing
3. I_{DDQ} as Burn-in alternative?
4. Experiences in I_{DDQ} test integration in manufacturing
5. Design for Current testability
6. Current testing and asynchronous circuits

Speakers who have expertise and insight into these topics are being identified and invited. The attendees will receive a digest based on these presentations. A dinner is included in the workshop registration and a discussion session during dinner is planned.

SCHEDULE: IDDQ 99 starts at 4:30 pm and ends at 9:30 pm on April 25th, 1999. It will be held in Salon 4 & 5.

REGISTRATION: All IDDQ 99 participants require registration, which includes workshop technical sessions, workshop informal proceedings, break refreshments and dinner.

SPONSORSHIP: IDDQ 99 is sponsored by the IEEE Computer Society TTTC.

INFORMATION: For further information on the technical program, please contact the Program Chair, Manoj Sachdev (msachdev@ece.uwaterloo.ca). Regarding other questions, please contact the General Chair Yashwant Malaiya (malaiya@cs.colostate.edu).

Web: http://www.cs.colostate.edu/~malaiya/iddq.html

IEEE
DESIGN & TEST OF COMPUTERS

IEEE D&T is a quarterly magazine published by the IEEE Computer Society in cooperation with the IEEE Circuits and Systems Society specifically for design and test engineers and researchers.

D&T features peer reviewed original work describing methods and practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in:

1. System-on-Chip Design and Test
2. Hardware/Software Codesign
3. Test Technology
4. Low Power Design
5. Reconfigurable Systems
6. High-Performance Designs
7. Verification/Validation

D&T publishes tutorial articles, roundtable discussions, keynote addresses, conference and panel reports, and standards updates contributed by authors working in the industry.

PAPER SUBMISSION: Postscript versions of manuscripts need to be submitted to D&T's magazine assistant at *dt-ma@computer.org*. Each submitted paper undergoes at least three technical reviews. All submissions must be original, previously unpublished work.

IEEE Design&Test of Computers

SPECIAL ISSUES: The four special issues planned for 1999 are:

1. DRAM Architecture and Test
2. Reengineering Digital Systems
3. Test and Product Life Cycle
4. MEMS Design and Test

SUBSCRIPTION INFORMATION: VTS allows you to obtain a half year subscription (July to December 1999) to IEEE Design & Test of Computers, if you select to embed it in your Registration Form. The fee is $16 for IEEE Computer Society members, $8 for IEEE/CS Student Members, and $45 for non-members. You may also subscribe on-line at: http://computer.org/subscribe/

For more information access D&T's Web page at: http://computer.org/dt

17th IEEE VLSI Test Symposium (VTS 99)
FRINGE TECHNICAL MEETINGS

A number of professional groups interested in test will hold their meetings at VTS 99. At press time, the following meetings were scheduled. For further information, contact the person listed at the e-mail address given.

FRIDAY, APRIL 24TH

1:00 pm — International Test Conference Program Committee (closed to non-members)
A. Ambler (*ambler@mail.utexas.edu*)

SUNDAY, APRIL 25TH

5:00 pm, Board Room — TTTC Executive Committee
Y. Zorian (*zorian@lvision.com*)

MONDAY, APRIL 26TH

*12:00pm — HLDVT Workshop Committee
A. Orailoglu (*alex@cs.ucsd.edu*)

*12:00 pm — IEEE European Test Workshop Committee
H.J. Wunderlich (*wu@informatik.uni-stuttgart.de*)

*12:00 pm — International Conference on VLSI Design Committee
V.D. Agrawal (*va@research.bell-labs.com*)

6:00 pm — IEEE VLSI Test Symposium Program Committee
A. Singh (*adsingh@eng.auburn.edu*)

TUESDAY, APRIL 27TH

7:00 am, Board Room — TTTC Technical Meetings Review Committee
D. Gizopoulos (*dgizop@4plus.com*)

*12:10 pm — International On-Line Test Workshop Committee and On-line Test TAC
M. Nicolaidis (*michael.nicolaidis@imag.fr*)
A. Paschalis (*paschalis@iit.nrcps.ariadne-t.gr)*

*12:10 pm — North Atlantic Test Workshop
J. Monzel (*jmonzel@us.ibm.com*)

*12:10 pm — TTTC Communications Group
P. Prinetto (*paolo.prinetto@polito.it*)

WEDNESDAY, APRIL 28TH

7:00 am, Conf. Room — TTTC Operations Committee
Y. Zorian (*zorian@lvision.com*)

11:00 am — IEEE VLSI Test Symposium Steering Committee
M. Nicolaidis (*michael.nicolaidis@imag.fr*)

*12:40 pm — Microprocessor Test & Verification Workshop Com.
M. Abadir (*abadir@ibmoto.com*)

*12:40 pm — TTTC High Density Module Testing TAC
Y. Zorian (*zorian@lvision.com*)

*12:40 pm — TTTC Mixed-Signal Test TAC
B. Kaminska (*bozena@opmaxx.com*)

THURSDAY, APRIL 29TH

5:00 pm, Salon 4 & 5 — IEEE P1500 Embedded Core Test Working Group
Y. Zorian (*zorian@lvision.com*)

**Meeting during Lunch Break*

17th IEEE VLSI Test Symposium (VTS 99)

SUNDAY, APRIL 25th, 1999

Time			
7:30 am - 8:30 am	TUTORIAL REGISTRATION		
8:30 am - 4:30 pm	Tut. 1: Testing Embedded-Core Based System Chips	Tut. 2: Recent Advances in BIST Technology	
4:30 pm - 9:30 pm	IDDQ 99 Mini-Workshop		

MONDAY, APRIL 26TH, 1999

Time		
7:30 am - 9:00 am	REGISTRATION	
9:00 am - 10:30 am	PLENARY SESSION	
11:00 am - 12:00 pm	S1: Testing High-Speed and Dynamic Circuits	S2: Core Testing
1:30 pm - 2:30 pm	S3: Diagnosis	S4: Techniques for the Very-Deep Submicron
2:50 pm - 3:50 pm	S5: Advanced Scan Path Techniques	S6: IDDQ Testing
4:10 pm - 5:30 pm	S7: Delay Fault Testing	S8: Validation, Verification and Diagnosis
8:00 pm - 9:30 pm	Special S1: The End of the Moore's Law Era?	Open Microphone Session

TUESDAY, APRIL 27TH, 1999

Time			
8:30 am - 9:30 am	S9: Mixed Signal Test	S10: BIST	
9:50 am - 10:50 am	S11: ATPG Related Approaches	S12: Testing MEMS, MCM and Analog Circuits	
11:10 am - 12:10 am	S13: Mixed Signal BIST	S14: High-Level Test Techniques	
1:30 pm - 3:00 pm	Panel 1: Failure Analysis and Silicon Debug	Panel 2: Beyond P1450 (STIL)	Panel 3: Nanometer Technologies
3:30 pm - 10:30 pm	SOCIAL PROGRAM (See page 22)		

WEDNESDAY, APRIL 28TH, 1998

Time			
9:00 am - 10:00 am	S15: Concurrent Checking	S16: Memory Test	
10:20 am - 11:20 am	S17: BIST Related Approaches	S18: Defect Oriented Test	
11:40 am - 12:40 pm	S19: On-Line Testing and Fault Tolerances	S20: DFT and Boundary Scan	
2:00 pm - 3:30 pm	Special S2: SOC Test Standardization	Panel 4: Built-In Current Monitoring	Special S3: Testing at System Speed
4:00 pm - 9:00 pm	TECS 99 Workshop		

THURSDAY, APRIL 30th, 1998

Time			
7:30 am - 8:30 am	REGISTRATION		
8:30 am - 4:30 pm	TECS 99 Workshop (Cont.)	Tut. 3: DFT Techniques	Tut. 4: Mixed-Signal DFT

17th IEEE VLSI TEST SYMPOSIUM

Early Registration Discount Form

MAIL or FAX form to: VLSI Test Symposium
1474 Freeman Drive, Amissville, VA 20106, USA
Tel: +1 (540) 937-8280, Fax: +1 (540) 937-3739

IMPORTANT:

- Read **General Information** (page 3) before completing this form.
- After April 13, register at the Symposium. (*Registration-at-Hotel* rates will apply)

First Name: ______________________ Last Name: ___________________________ Company: ____________________

Mail Stop: _______________________________ St. Address/Box No.: ____

City: ___________________________ State (US): ______ Zip Code: ___________Country: ____________________

Tel: __________________________ Fax: ____________________ IEEE/Computer Society Member No.*: _____________

E-mail: ________________________ Enroll me as a Test Technology Technical Council member for 1999 (no dues or fees): ☐

Special Dietary Requirement: Vegetarian ☐ Other (specify) _______________________________

I Will Attend the Social Program (no extra charge for those paying IEEE/CS Member or Non-Member rates) ☐

DISCOUNT REGISTRATION (available until April 13)	**IEEE/CS Member***	**Student Member****	**Non-Member**
SYMPOSIUM & WORKSHOPS			
VTS 99, April 26 -28	$395 ________	$125 ________	$495 ________
TECS 99, April 28 - 29	$210 ________	$100 ________	$260 ________
IDDQ 99, April 25	$90 ________	$70 ________	$115 ________
TUTORIALS, See pages 6 and 19.			
Tutorial No. **1** *or* **2**: April 25 No.: ______	$285 ________	$110 ________	$350 ________
Tutorial No. **3** *or* **4**: April 29 No.: ______	$285 ________	$110 ________	$350 ________
ADDITIONAL Copies of ***VTS 99 Proceedings***			
Pick up at Symposium Quan.__________@	$45 ________	$45 ________	$45 ________
Mailed to US or Canada address. Quan.__________@	$50 ________	$50 ________	$50 ________
Airmailed to other address. Quan.__________@	$60 ________	$60 ________	$60 ________
ADDITIONAL Social Program (for companion or student)	$90 ________	$90 ________	$90 ________
Subscription, *IEEE Design & Test of Computers* magazine, 1/2 year (July to December, 1999)	$16 ________	$8 ________	$45 ________
	TOTAL: ________	**TOTAL:** ________	**TOTAL:** ________

* IEEE/CS member rates are granted only if your current valid membership number is filled in above.
** Student member registrations are granted only if a photocopy of your current IEEE Student Member card is enclosed.

SEND FULL PAYMENT IN US $ WITH THIS FORM. Use a check drawn on a US bank, or a US bank credit card. PURCHASE ORDERS ARE NOT ACCEPTED. Make checks payable to: *1999 IEEE VLSI TEST SYMPOSIUM.* USE YOUR CREDIT CARD IF REGISTERING BY FAX.

FOR CREDIT CARD PAYMENT Check card type: VISA/MASTERCARD ☐ AMERICAN EXPRESS ☐

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Advance registration fees will be refunded only on written request, mailed or faxed, and received by 4/6/99. A $50 processing fee is charged for each refund.

17th IEEE VLSI TEST SYMPOSIUM

Hotel Reservation Form

Mail or phone your hotel reservation to:
Marriott Laguna Cliffs Resort
25135 Park Lantern
Dana Point, CA 92629, USA
Tel: +1 (949) 661-5000, Fax: +1 (949) 661-5358
(Reservations: +1 (800) 533-9748 , VTS 99 Code: **IEEE-VTS**

Make your reservation no later than April 2, 1999 to receive the special VTS 99 rate of $149.00 per room. (After April 2, the hotel's regular higher rate will apply.)

First Name: ___________________________________ Last Name: ____

Company: ___________________________________ Mail Stop: ____

Address: ____

City: ____ State: _______ Zip Code:______________________________

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Tel: ________________________________ Arrival Date: ________________ Departure Date: _____________________

CHECK ACCOMODATIONS DESIRED:

Single @ $149.00* per day ☐ Double @ $149.00* per day ☐ *Note: These rates apply only until April 2.*

If **Double**, name of the other person who will use the room: ____
* *Rates are subject to additional tax of 10%.*

TO RESERVE ACCOMODATIONS, SEND DEPOSIT IN US $ FOR ONE DAY WITH THIS FORM. Make check or money order payable to *Marriott Laguna Cliffs Resort.* Or you may reserve accomodations using your major credit card.

Major Credit Card Name: _________________________ Card No.: ____

Credit Card Expiration Date: _____________ Cardholder Signature: ____

OR, **YOU MAY REGISTER BY PHONE.** Be prepared to give the above information, including your major credit card information and the VTS 99 hotel code, **IEEE-VTS.**

Deposits are refundable if accomodations are cancelled at least 48 hours prior to your scheduled arrival.