



Wrapper Instruction Register (WIR) Tiger Team Status

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Presentation Outline

- WIR Tiger Team Overview**
 - **Tiger Team Members**
 - **Mission & Scope**
- Tiger Team Status**
- Open Issues**
- Work to Complete**

P1500 Architecture Task Force

WIR Tiger Team Mission and Scope

Team Members

Mike Ricchetti - Intellitech (Chair) Fidel Muradali - Agilent Technologies
Alan Hales - Texas Instruments Lee Whetsel - Texas Instruments
Eddie Rodriguez - Intel

Team Mission & Scope

Define the design & operation of the Wrapper Instruction Register (WIR) in terms of behavioral Requirements, Permissions, and Recommendations:

- ✓ WIR within P1500 register architecture
- ✓ WIR operation: Capture, Shift, Update, Reset, etc.
- ✓ Wrapper Interface Port signals & protocol
- ✓ WIR Interface/Control to Bypass, WBR and Core
- ✓ Provide some *example* WIR implementations & SoC configurations
- ✓ Proposed owning Wrapper Bypass to CTAG

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Current Status of WIR Tiger Team

- ❑ **Overview & most Descriptions/Specifications for WIR are done**
 - **Descriptions and Rules, Permissions & Recommendations for:**
 - ✓ **Wrapper Register Architecture**
 - ✓ **WIR Design and Operation**
 - ✓ **Wrapper Interface Port (WIP)**
 - **Slides are on CTAG private web site**
- ❑ **All of above have been reviewed by CTAG**
 - **Text version handed off to Documentation Task Force in D0.1**
 - **Fourth revision in progress & has been reviewed by Tiger Team**
- ❑ **Team has been inactive since DATE**
 - **New Tiger Team member: Eddie Rodriguez from Intel**
 - **Owners assigned for “Work to Complete” list**

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WIR Tiger Team Open Issues List

- ❑ **Currently some minor issues from last TT review:
Will need further input and discussion from CTAG**
 - **Asynchronous vs. Synchronous reset**
 - ✓ Should one method be a Rule ?
 - ✓ WIRs with either method should be interoperable ?
 - **Encoding of WIP Enables for Shift, Capture, Update, etc
to save wrapper terminals & reduce global wires**
 - ✓ Would enforce single operation at a time for WIR
 - ✓ This may not be desirable for WBR
 - **Wrapper Subordination**
 - ✓ WIR should not reset coming out of subordination mode
 - ✓ Reset takes precedence over all operations & instructions

- ❑ **Other Issues ?**

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WIR Tiger Team Work to Complete

□ Work to Complete:

- **Description & Specification for:**
 - ✓ WIR system chip connections
 - ✓ **WIR Interface to Bypass, WBR and Core**
- **Implementation Examples for:**
 - ✓ WIR connected to WIP
(Muxscan, LSSD, etc. & gated-clock vs. synchronous)
 - ✓ WIR Operation for above (Showing protocols & timing)
 - ✓ WIR system chip connections
 - ✓ WIR interoperability with 1149.1 TAP(s) at SoC level
(Show simultaneous WIR Updates w/TAPed Cores)
- **Write descriptive text for sections in P1500
Draft Documentation**