



Wrapper Instruction Register (WIR) Specifications

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**WIR Tiger Team
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Presentation Outline

- **Introduction & WIR Overview**
 - Tiger Team Members, Mission & Scope
 - WIR in the P1500 Architecture
- **WIR Design *Description* and *Specification***
 - Rules, Recommendations & Permissions
 - Wrapper Register Architecture
 - WIR Design and Operation
 - Wrapper Interface Port
 - WIR Interface to Bypass, WBR & Core
 - Interconnection of WIRs
- **Example Implementations**
 - WIRs and WIP Protocols
 - SoC Interconnection of WIRs
- **Open Issues & Work to Complete**

P1500 Architecture Task Force

WIR Tiger Team Mission and Scope

Team Members

Mike Ricchetti - Intellitech (Chair) Fidel Muradali - Agilent Technologies
Alan Hales - Texas Instruments Lee Whetsel - Texas Instruments
Eddie Rodriguez - Intel

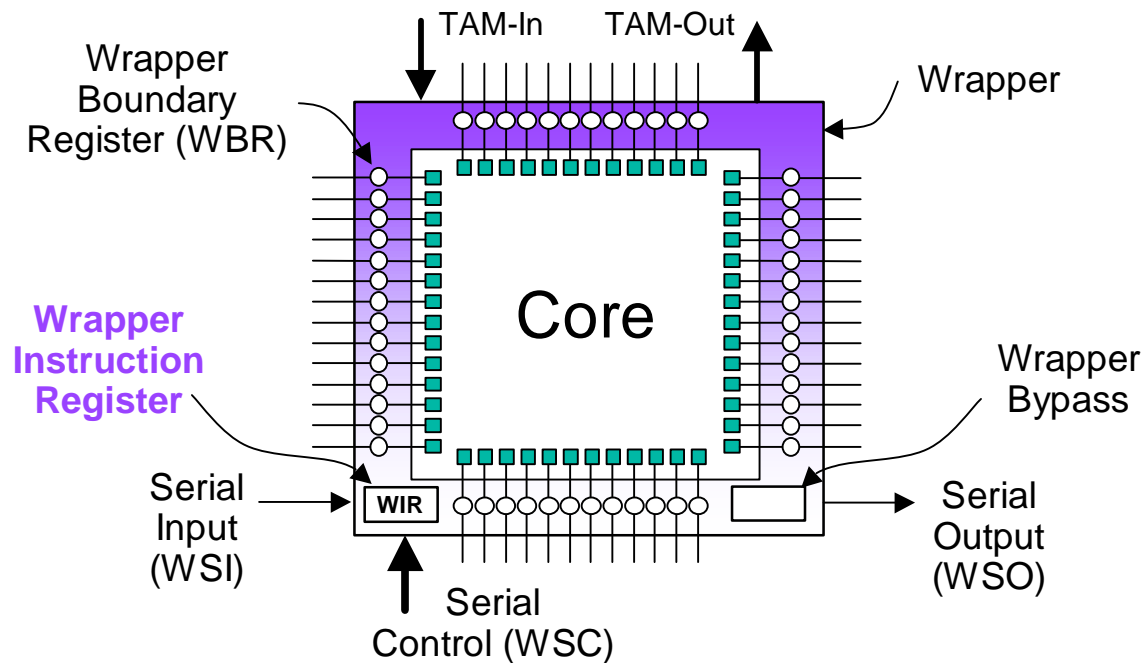
Team Mission & Scope

Define the design & operation of the Wrapper Instruction Register (WIR) in terms of behavioral Requirements, Permissions, and Recommendations:

- ✓ WIR within P1500 register architecture
- ✓ WIR operation: Capture, Shift, Update, Reset, etc.
- ✓ Wrapper Interface Port signals & protocol
- ✓ WIR Interface/Control to Bypass, WBR and Core
- ✓ Provide some *example* WIR implementations & SoC configurations
- ✓ Proposed owning Wrapper Bypass to CTAG

WIR in the P1500 Architecture

Description of P1500 Architecture Components



□ P1500 Wrapper Components:

- WIR provides wrapper and core mode control
- WBR provides test and access functions at the core terminals
- Wrapper Interface Port (WIP) includes WSC, WSI & WSO
- Wrapper Bypass is a scan bypass through WSI-WSO

P1500 WIR Description & Specification

Summary of IEEE Standard Definitions

Specifications:

Rules

Specify the mandatory aspects of this standard. Rules contain the word *shall*.

Recommendations

Indicate a preferred practice for designs that seek to conform to this standard. Recommendations contain the word *should*.

Permissions

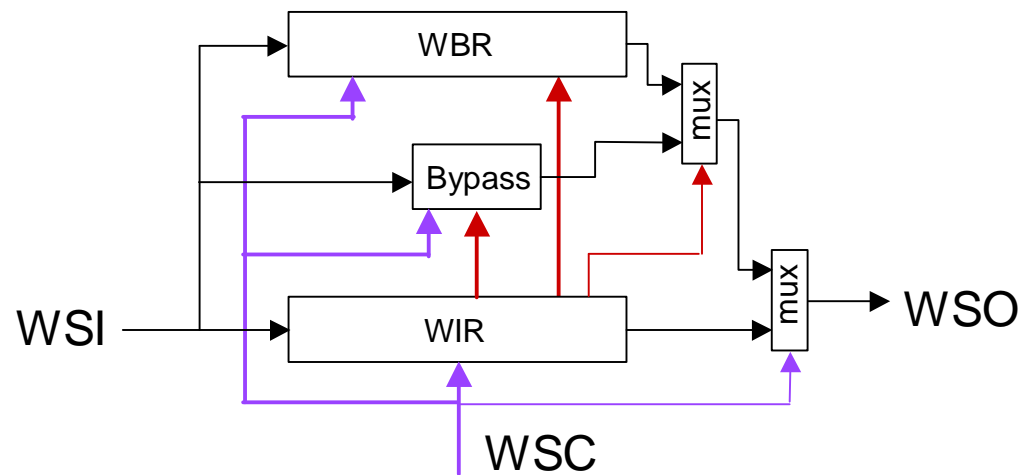
Show how optional features may be introduced into a design that seeks to conform to this standard. These features will extend the application of the standard. Permissions contain the word *may*.

Descriptions:

Informative text and diagrams used to illustrate the standard. Descriptions are *not* considered to be part of the definition of the standard.

WIR Design Description

Wrapper Register (WR) Architecture



❑ **WSC signals:**

- **Select whether the WIR or other WR is connected between WSI & WSO**
- **Control operation of WIR, Bypass and WBR**

❑ **The Updated WIR contents then determines:**

- **The current Modes for the Wrapper & Core logic**
- **Which WRs, or Core Scan Registers, are connected between WSI & WSO**
- **And if a user TAM connection & register configuration is enabled**

WIR Design Specification

Wrapper Register Architecture

Rules

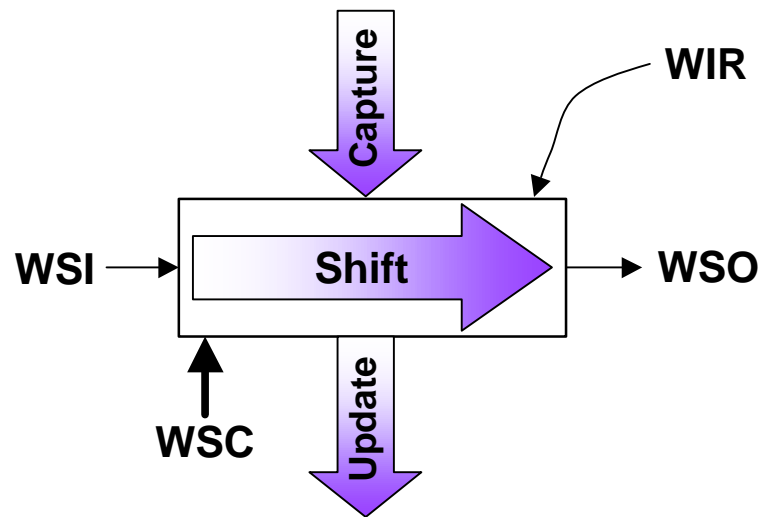
- (a) The P1500 Wrapper shall contain a Wrapper Instruction Register (WIR).
- (b) The WIR shall be a on separate wrapper shift path, connected in parallel & having a common serial data input (WSI) and serial data output (WSO), with the Wrapper Bypass and Wrapper Boundary Register (WBR).
- (c) Selection of whether the WIR scan path or the scan path parallel to the WIR is connected between WSI and WSO shall be determined by the WSC signals and the Wrapper Interface Port (WIP) protocol.
- (d) The circuitry that forms the WIR shall be dedicated P1500 logic (i.e., this logic shall not be shared in order to perform a system function).

Permissions

- (e) WRs other than the Bypass and WBR, or Core Scan Registers, may be connected in parallel to the WIR, and when selected, connected between WSI and WSO (e.g., a core internal scan register).

WIR Design Description

WIR Design and Operation



□ WIR operation is controlled by WSC signals and provides:

- Serial shift of the WIR contents from WSI to WSO
- A parallel update stage that determines the active Modes
 - ✓ Ensures that Wrapper & Core Modes do not wiggle during WIR shift operations
- Optional, parallel capture of test control information into the WIR
 - ✓ Can also be utilized for testing of WIR logic & WIR scan paths

WIR Design Specification

WIR Design

Rules

- (a) The WIR shall include at least three serial shift stages capable of storing WIR logic values.
- (b) Values shifted into the WIR stages shall be latched such that they do not effect the currently active Wrapper & Core Mode during the WIR Shift Operation.
- (c) There shall be no inversion of logic values between the serial input (WSI) and the serial output (WSO) of the WIR, or between any of the serial shift stages.

Permissions

- (d) Parallel inputs to the WIR may be provided to permit capture of logic values when a WIR Capture Operation occurs. The WIR may capture values to be used for test control or testing of the WIR, or other P1500 logic.

Recommendations

- (e) The two LSBs of the WIR (i.e., those nearest to WSO) should capture a fixed binary “01” pattern (the 1 into the LSB) when a WIR Capture Operation occurs.

WIR Design Specification

WIR Operation

Rules

- (a) **The behavior of the WIR shall be defined by the states of the WIP signals (i.e., WSI, WSO, WSCs) and WIP protocol as follows:**

WIP Protocol

WIP Reset Operation

WIR Shift Operation

WIR Update Operation

WIR Capture Operation

Other WIP Operations

WIR Behavior

Sets normal mode (WBYPASS) as the Wrapper & Core Mode

Scan shift of WIR from WSI to WSO

Activate new Wrapper & Core Mode

Load WIR with parallel Capture values

WIR retains last Wrapper & Core Mode

- (b) **Multiple WIR Operations (i.e., Reset, Shift, Update, Capture) shall not occur simultaneously for a given WIP Protocol.**
- (c) **The currently active Wrapper & Core Mode shall remain active until either a WIP Reset Operation or WIR Update Operation occurs, causing a new Mode to become active. The currently active Mode shall become inactive subsequent to the new Wrapper & Core Mode becoming active.**
- (d) **A WIP Reset Operation shall cause the active Wrapper & Core Mode to become the normal system mode (i.e., WBYPASS).**

WIR Design Specification

WIR Operation Continued

Rules Continued

- (e) A WIR Shift Operation shall cause scan data to shift through the WIR, from WSI to WSO.
- (f) A WIR Update Operation shall activate a new Wrapper & Core Mode, as determined by the current contents of the WIR serial shift stage.
- (g) A WIR Capture Operation shall load the data at the parallel inputs of the WIR into the serial shift stage of the WIR.

Permissions

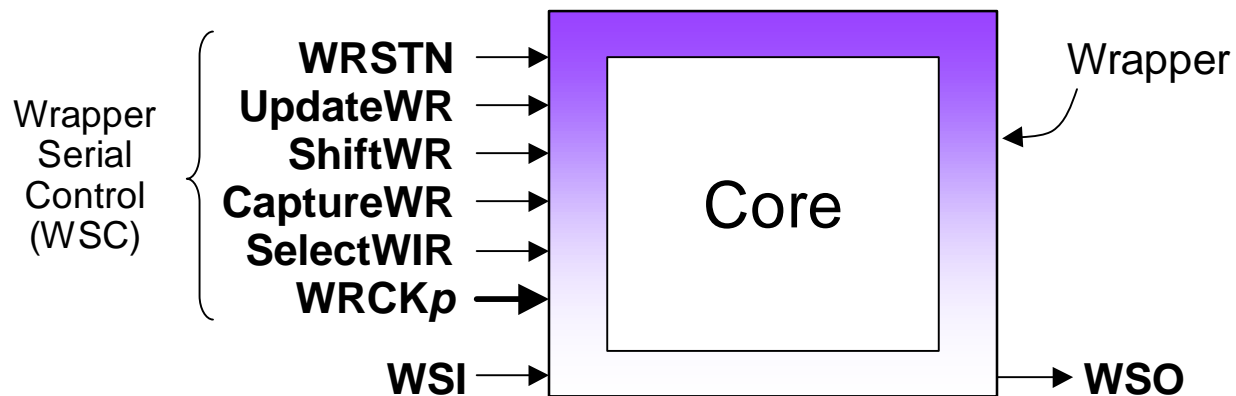
- (h) The sequences and number of WIR Operations may occur in any order.

Recommendations

- (i) Where parallel capture inputs are provided to the WIR, stages which are not required to capture data should be designed to load a fixed binary logic value (0 or 1) when a WIR Capture Operation occurs.

WIR Design Description

Wrapper Interface Port (WIP)



- ❑ **WIP is currently designed to support WIR**
 - Could also support other WRs & Core Registers (e.g., Bypass, WBR or internal)
 - Designed to have synchronous WIP Protocol/Operations
 - Supports edge-triggered muxscan in addition to other scan methodologies
- ❑ **WSC Signals:**
 - WRCKp are one or more WIR or Wrapper Register Clock *phases*
 - WRSTN is a dedicated Wrapper Register Reset
 - SelectWIR selects between WIR or other WRs/Core Registers
 - UpdateWR, ShiftWR and CaptureWR are enables for WIP Operations

WIR Design Specification

Wrapper Interface Port: Terminals

Rules

- (a) The WIP shall include the following control and clock terminals:
WRSTN, SelectWIR, ShiftWR, UpdateWR, CaptureWR and WRCK.
- (b) The WIP shall include the following serial scan terminals: WSI and WSO.
- (c) WIP scan and control signals (i.e., WRSTN, SelectWIR, UpdateWR, ShiftWR, CaptureWR, WSI and WSO) shall be dedicated P1500 core terminals (i.e., they shall not be used for any other system function).

Permissions

- (e) The WIP may include other WRCK_p clock terminals where the WIR is operated by a multi-phase clock. WRCK_p clocks may be shared with other system clocks.

WIR Design Specification

Wrapper Interface Port: WIR Protocols

Rules

- (a) The WIR shall retain its state (i.e., serial shift stage values & currently active Wrapper & Core Mode) indefinitely when the WRCK clock signals for the WIR are stopped (i.e., clock inputs held at a fixed logic values).
- (b) WIR Shift Operations shall occur synchronously to WRCK clocks, following assertion of ShiftWR to a logic value of 1.
- (d) A WIR Update Operation shall occur synchronously to WRCK clocks, following assertion of UpdateWR to a logic value of 1.
- (e) A WIR Capture Operation shall occur synchronously to WRCK clocks, following assertion of CaptureWR to a logic value of 1.
- (f) Changes in the logic value of the WSO output shall occur synchronously to WRCK clocks.
- (g) A WIR Reset Operation shall occur following the assertion of WRSTN to a logic value of 0.

WIR Design Specification

Wrapper Interface Port: WIR Protocols Continued

Permissions

- (h) A WIR Reset Operation may occur either synchronous to WRCK clocks, or asynchronously, following the assertion of WRSTN to a logic value of 0.**

Recommendations

- (i) WIR Operations should be controlled by WIP Protocols that use a single edge-triggered WRCK clock. The rising-edge of WRCK should be used to sample WIR inputs (e.g., WSI Shift-in and Capture) and the falling-edge of WRCK should be used to drive WIR outputs (e.g., WSO Shift-out and Update).**
- (j) The WIR Reset Operation should occur asynchronously following assertion of WRSTN to a logic value of 0.**
- (k) WRSTN should be a dedicated WIP Reset terminal and should not be used to initialize any other system logic within the core.**