

***Unapproved IEEE P1500 Working Document***

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***Update Presentation of the IEEE  
P1500 Scaleable Architecture for  
Testing Embedded Cores***

**Presented on behalf of the CTAG Team by**

**Lee Whetsel**

**May 5, 2000**

# ***P1500 Architecture Task Force***

## ***Active Task Force Members***

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**Lee Whetsel (Task Force Chair) - Texas Instruments**

**Saman Adham - LogicVision**

**Debashis Bhattacharya - TI**

**Dwayne Burek - LogicVision**

**C.J. Clark - Intellitech**

**Mike Collins - Cisco Systems**

**★ Jason Doege - Synopsys**

**Grady Giles - AMD**

**Sanjay Gupta - SiberCore**

**Alan Hales - Texas Instruments**

**Douglas Kay - Cisco Systems**

**Marc Levitt - Sonics**

**Adam Ley - Asset Intertech**

**Erik Jan Marinissen - Philips**

**★ Teresa McLaurin - Motorola**

**Fidel Muradali - Agilent Technologies**

**Srinivas Patil - Mentor Graphics**

**Janusz Rajski - Mentor Graphics**

**Rochit Rajsuman - Advantest**

**★ Mike Ricchetti - Intellitech**

**Eddie Rodriguez - Intel**

**Paul Soong- Nortel**

**Jon Udell - Palmchip**

**Alex Zamfirescu - ASC**

**Yervant Zorian - LogicVision**

**★ - Tiger Team Champions**

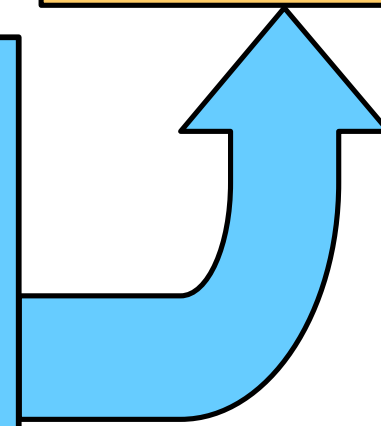
# Presentation Outline

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- ★  Introduction
- ★  General Update Presentation
- ★  Tiger Team Update Presentations

- Task Force Mission, Scope and Current Status
- Overview of Proposed Architecture
- Core Test Requirements
- P1500 Architecture Components
- Agreed To Motions
- Summary & Future Task Force Activities

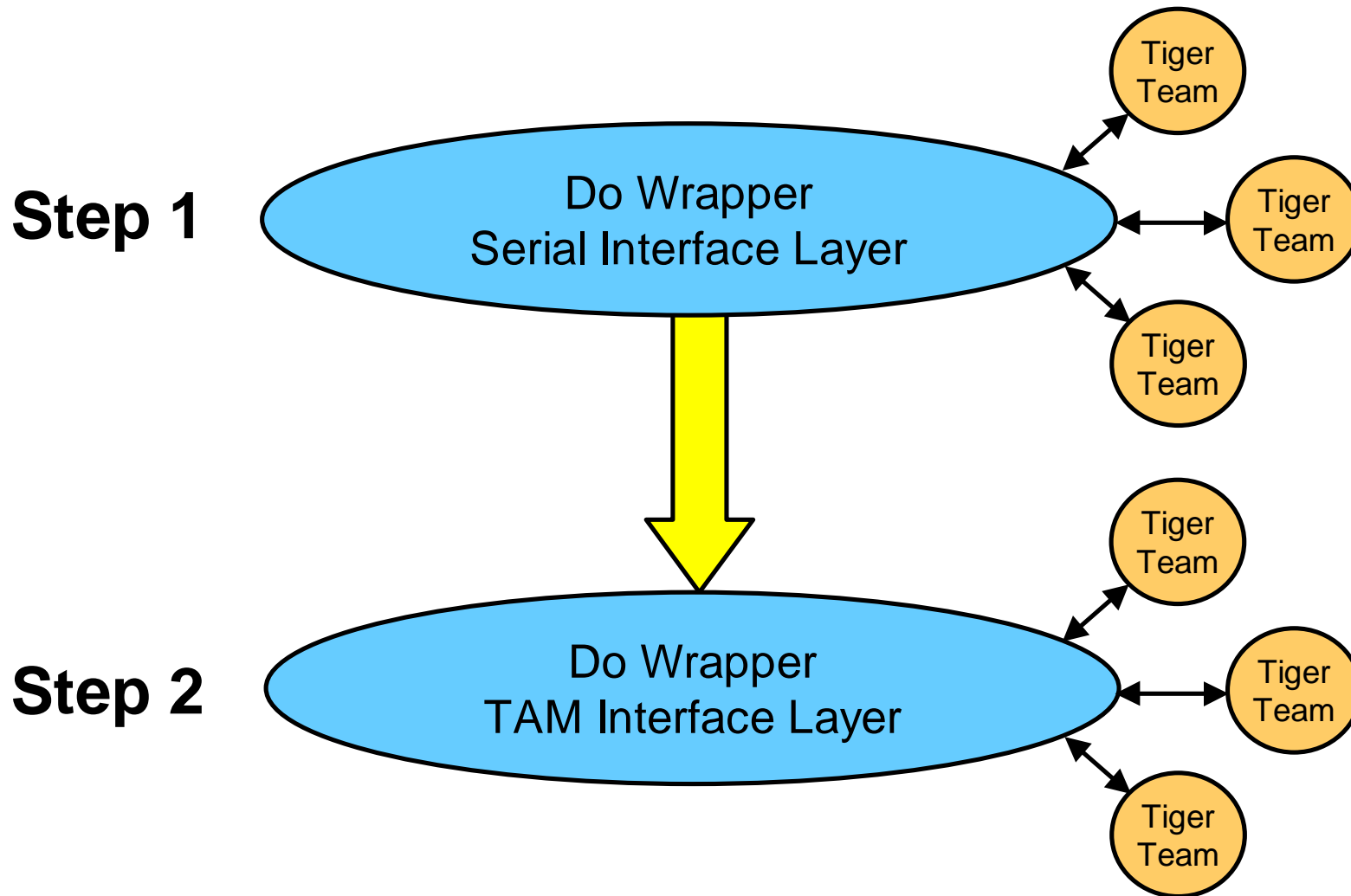
See Web site  
<http://grouper.ieee.org/groups/1500/nov99/ctag.pdf>



# P1500 Architecture Task Force

## Two Layer Wrapper Development Process

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# ***P1500 Architecture Task Force***

## ***Serial Interface Layer Tiger Teams***

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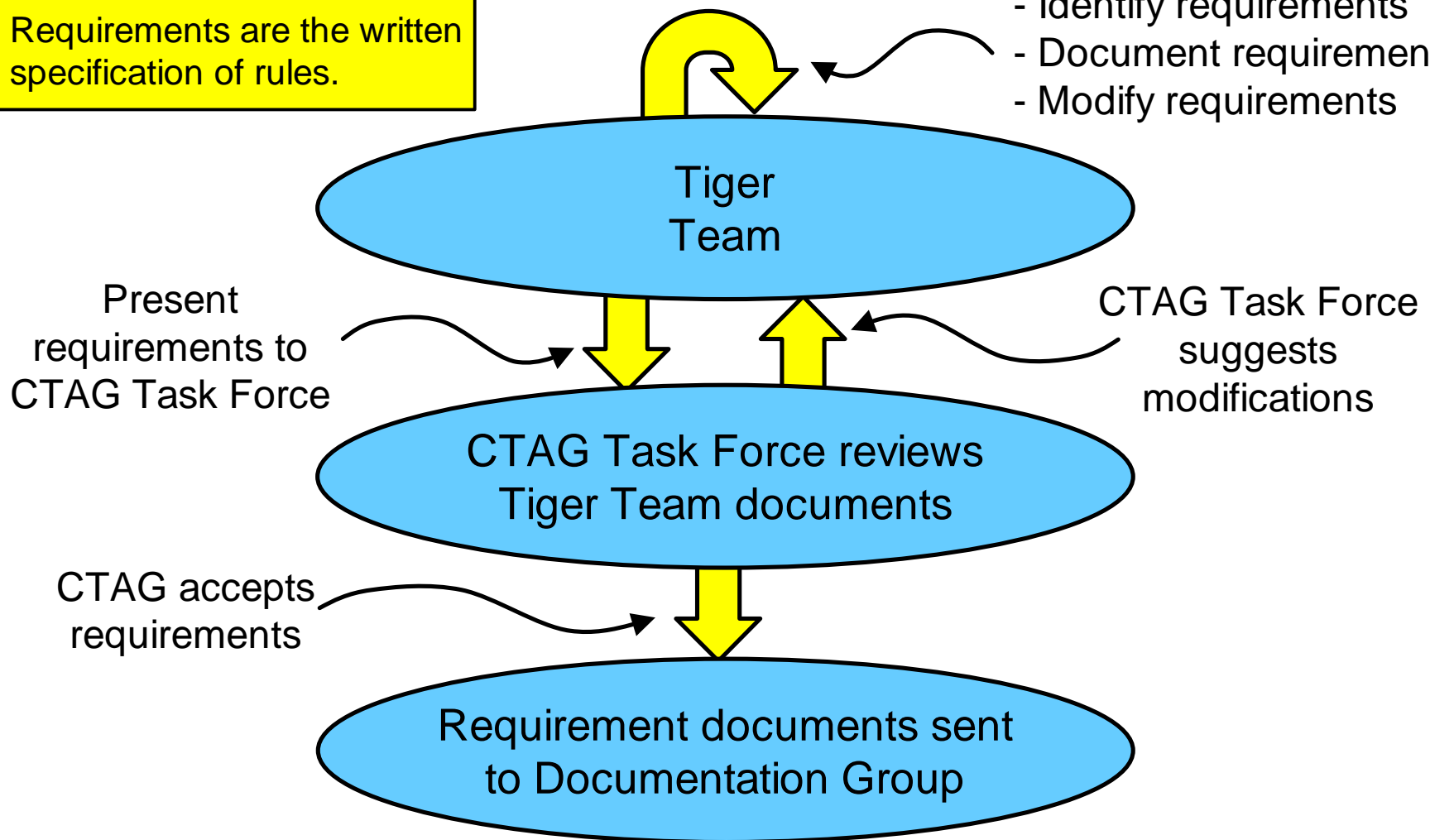
- Wrapper Instruction Tiger Team**
  - Define and document Wrapper instructions
- Wrapper Instruction Register Tiger Team**
  - Define and document Wrapper Instruction Register
- Wrapper Boundary Register Tiger Team**
  - Define and document Wrapper Boundary Register
- Tiger Teams meet weekly via teleconferencing**

# P1500 Architecture Task Force

## Tiger Team Operating Model

Requirements are the written specification of rules.

- Identify requirements
- Document requirements
- Modify requirements



# ***P1500 Architecture Task Force***

## ***General Task Force Status Since ITC99***

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### **❑ Few Discussions on Wrapper Subordination**

- Good idea to support TAMs, e.g. for a BISTed core
- Need to finalize in WIR Tiger Team

### **❑ Memory Discussion**

- General consensus is that memory cores are in P1500 scope & can be easily supported for BIST
- Will revisit some minor issues after Serial Layer work
- Would like more input/participation from vendors

### **❑ Discussions on “Plug-n-Play”**

- What does it mean to be plug-n-play ?
- Motions on clocking:
  - ✓ WIR & Bypass should have dedicated clocks
  - ✓ WBR leaning toward allowing system clocks to be used

### **❑ Majority of discussion was from Tiger Teams !**

# ***P1500 Architecture Task Force***

## ***Tiger Team Update Presentations***

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- **Wrapper Instruction Tiger Team Update**
  - Teresa McLaurin
- **Wrapper Instruction Register Tiger Team Update**
  - Mike Ricchetti
- **Wrapper Boundary Register Tiger Team Update**
  - Jason Doege