

# A P1500 Activity (CTL) Defining a Core Test Language

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# Top Level View of CTL

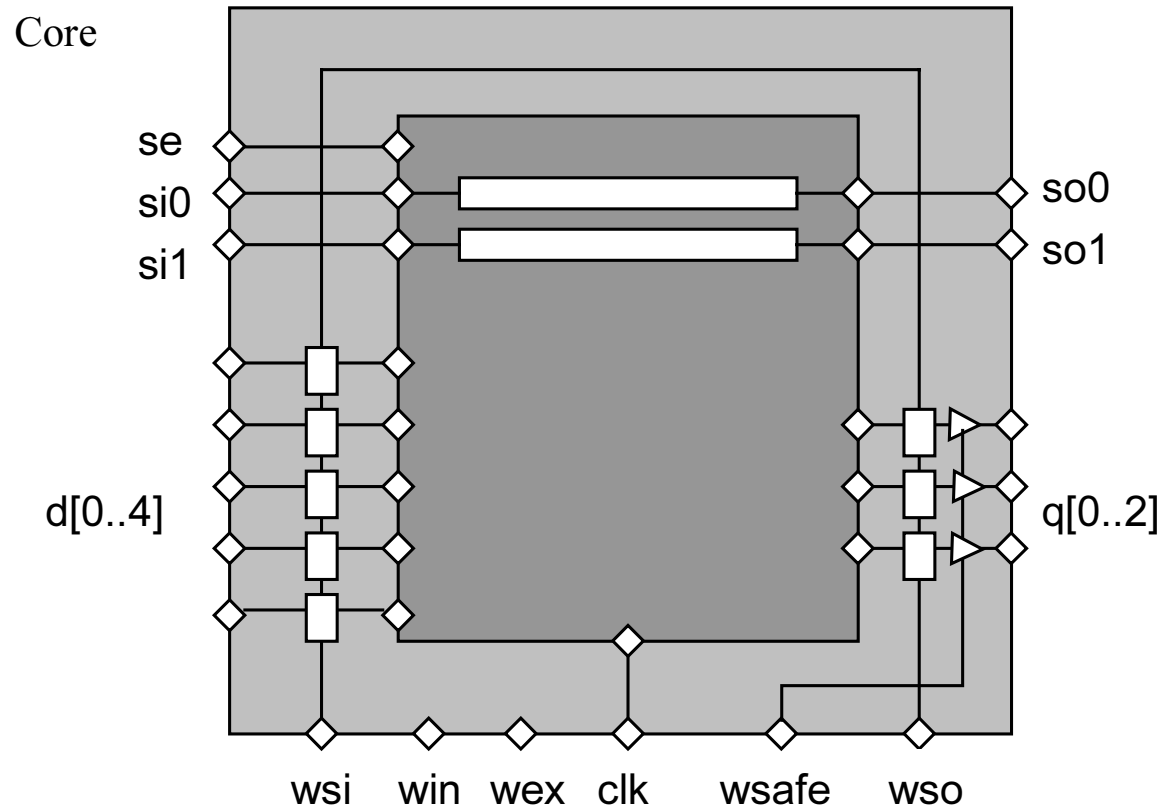
```
Environment {  
    FileReference type format filename;  
    CTL {  
        // Describe Common Info  
    }  
    CTL modeType modeName {  
        // Describe Mode Specific Info  
    }  
    CTL modeType modeName {  
        // Describe Mode Specific Info  
        Parent modeName;  
    }  
}
```

```
CTL modeType ModeName {  
    Wrapper <IEEE1500|IEEE1149.1>;  
    Parent  
    Inherit  
  
    CoreInstance { ... }  
    Internal {...}  
    ScanInternal { ... }  
    External { ... }  
    PatternInfo { ... }  
}
```

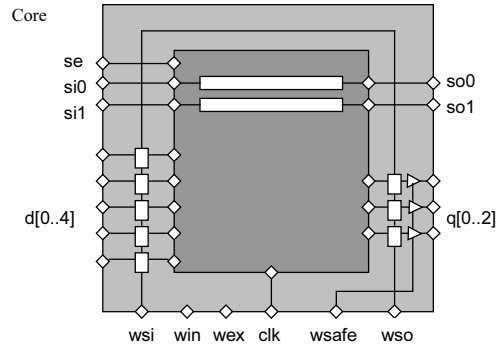
# Information Describable in CTL

- Internal
  - Wrapper Cell/Pin
  - IsConnected
  - IsEnabledBy
  - IsDisabledBy
  - ElectricalChar
  - LaunchClock
  - CaptureClock
  - StrobeAccuracy
  - DriveAccuracy
  - DriveChar - SkewTolerant
  - StrobeChar
  - DataRate
  - DataType
- PatternInfo
  - Purpose ( Diagnostic/ Production/ Characterization)
  - Purpose (Iddq/ LBIST/ Parametric/ AtSpeed/ Scan/ MBIST/Delay/ ChainContinuity/ EstablishMode)
  - Purpose (Control/ Observe/ ...)
  - Power
  - SizeInfo { ... }
  - FaultInfo
  - MeasurePoints
  - FunctionIdentifier
  - MacroDefs/Procedures/ ScanStructures/BISTStructures
  - Fixed

# Example Core



# CTL by Example (Scan Chain)



```

Environment {
  CTL {
    Internal {
      'wsi+wso' { DataType ScanData;
      wsafe {DataType ScanEnable;
      clk { DataType Clock ScanClock;
    }
    PatternInfo {
      ScanStructures structsUsed;
      MacroDefs macrosUsed;
      chainOperation {
        Purpose ControlObserve
        { NormalLoadNormalUnload;}}
    }
  }
}

```

```

Header { Title “scan example”; Date “Apr 2000”}

```

```

Signals { wsi In {ScanIn 8;}
  wsafe In;
  wso Out {ScanOut 8;}
  clk In; }

```

```

ScanStructures structsUsed {
  ScanChain internalScanChainC {
    ScanLength 8;
    ScanInversion 0;
    ScanCells {c[0..7];}
    ScanIn wsi;
    ScanOut wso;
    ScanMasterClock clk;}}

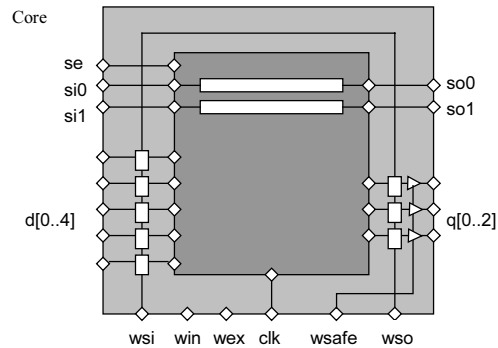
```

```

MacroDefs macrosUsed {
  “chainOperation” {
    W cChainTiming;
    ScanChain internalScanChainC;
    C { wsafe = 0;}
    Shift { V { wsi=#; wso=#; clk=P;}}}}

```

# Some Information for ExTest



Environment {

CTL ExTest myExtestMode {

Internal {

d[0..4] {

IsConnected In internalScanChainC c[0..4];

}

q[0..2] {

IsConnected Out internalScanChainC c[7..5];

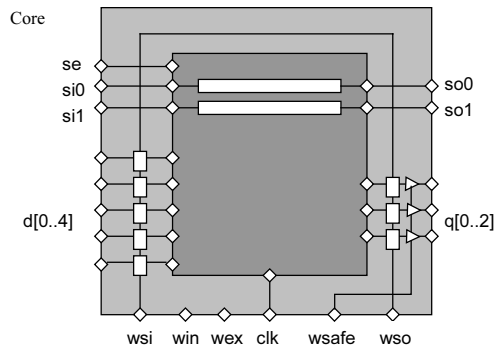
IsEnabledBy Out Signal wsafe ForceUp;

}

}

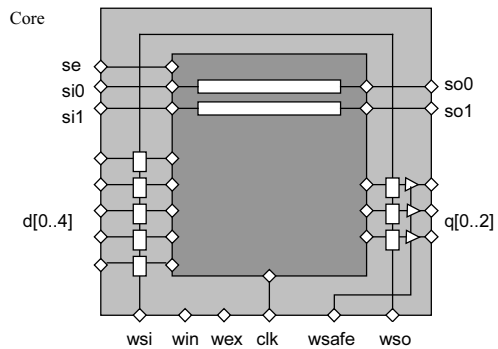
}

# Describing Characteristics of the Test Data



```
Header {  
    Title "Test Data Char"; Date "Apr 2000"  
}  
Signals {  
    q[0..2] Out; wsafe In;  
}  
  
Environment {  
    CTL {  
        Internal {  
            q[0..2] { StrobeChar ScanStable;}  
        }  
        External {  
            wsafe { ConnectTo TCM; }  
        }  
    }  
}
```

# CTL Example (Isolate Mode)



```
Environment {  
  CTL Isolate mySafeModeExample {  
    PatternInfo {  
      configCore {  
        Purpose EstablishMode -1;  
        Fixed 'wsafe+q[0..2]';  
      }  
    }  
  }  
}
```

```
Pattern configCore {  
  V {wsafe = \eD; q[0..2] = \eQ;}  
}
```

# Status

- Syntax for Deterministic Tests are Done.
- Provided input in the form of documentation for Part2 of the overall document.

# Our To Do List

- Logic BIST (1 month).
- Testing CTL on some real designs (< 6 months).
- Cleanup terminology (2 months).
- Determine Mandatory/Optional Info (1 month).

## Possible Functions Not For 1st Release

- Advanced Memory BIST (4 months).
- CTL and other Tester Pattern Formats (2 months).

