

IEEE P1500 Mergeable Core Test Task Force Update

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Our Mission

- To find solutions that will enable easy test interoperability of Mergeable (soft/firm) cores
- To find what needs to be done inside the core to make easy test integration

A Double Edged Attack to the Problem

- Develop a set of soft core test deliverable requirements
- Develop a set of test interoperability design rules

Soft Core Test Deliverables

Objective: *To define a format for soft core providers to present Test and DFT experience and recommendations to the SoC integrator*

Assumptions:

- *RTL soft cores are likely to be delivered without any DFT*
- *Core providers have subjected the core to Synthesis, DFT and Test tools under different scenarios*

Soft Core Test Deliverables

Current Status:

- Review of VSIA Test Data Interchange Format specs
 - Document is currently limited to members only
 - Deliverable requirements strongly biased towards hard VCs
- First proposal for a deliverables format has been reviewed. Modifications and refinements in progress.

Soft Core Test Deliverables

- Proposed format specification
 - Document the DFT tools used on the core (scan/BIST insertion, ATPG, Faultsim)
 - Document the results obtained from each tool
 - Fault coverage, warnings, errors etc.
 - Upper bound (with all primary inputs controllable and all primary outputs observable) and lower bound (only scan inputs/outputs controllable/observable) fault coverages
 - Document ATPG constraints, scripts, test modes, scan configurations
 - Random pattern testability bounds
 - Embedded memory test/isolation/bypass schemes used
 - Testability issues for Iddq, special constraints and set-up requirements
- Further refinements in progress

Test Interoperability Rules

Objective: *To devise methods to make “1500 ready” cores which can be (test) integrated into the IC, possibly without any wrappers, by following some prescribed interoperability rules and minimal additional hardware.*

Test Interoperability Rules Under Consideration

- Rule: *All outputs of the core must be registered*
- Guideline(Highly Recommended): *All inputs of the core should be registered (except normal exceptions like clocks, resets etc).*
- Benefits:
 - Already an RMM defined design rule
 - Helps achieve timing closure
 - Core placement is easier (with input registration)
 - Core can be DFTed independently
 - Fault coverage numbers will be more realistic

Test Interoperability Rules Under Consideration

- Benefits (contd)
 - Input/Output registers can serve as the wrapper
- Disadvantages:
 - Added delay and latency
- Issues to resolve:
 - Clocking requirement of the I/O registers

Interoperability Rules

- Embedded memory test issues
 - Scott Davidson
- Internal tri-state bus
- How can soft core test requirements be described in CTL? Is current CTL adequate?