Mergeable Core Memory Test

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- **The Problem**
- **Assumptions**
- **Testing Embedded Memories**
- **Memory Interaction with Logic Test**

The Problem

Given: A soft, mergeable core with embedded memories.

What rules/documentation are required

- **To support testing the memory**
- **To support testing the logic surrounding the memory**

Additional concerns

- **Support for debug**
- **Support for diagnosis**

Assumptions

- An RTL or behavioral model of the core, including memory(ies) is provided.
  - A gate level model is provided or is synthesized.
- Documentation of memory control signals is provided.
- Timing diagrams, etc. for the memory are provided.

Involved parties:

- Core provider
- Core integrator
- Silicon vendor

Testing the Embedded Memories

RTL for Memory BIST from provider.

- **Control signals routed to core boundary.**
- **Documentation on BIST protocol, defect coverage, algorithm.**
- **Integrator provides control from SoC TAP, etc.**
- **Fault coverage of BIST logic and of shadow logic.**
  - **How to enumerate this coverage is not clear.**

Provider provides test vectors, routes memory I/O to core I/O

- **Provider documents timing requirements,**
- **Integrator routes vectors from SoC boundary to core.**

Testing the Embedded Memories (2)

Provider leaves Memory Test to Integrator

- **Integrator adds BIST, etc.**

Silicon Vendor takes Responsibility for Memory Test

- **Might have memory compilers with BIST.**
- **Memory test might be coupled to yield enhancement (redundant rows/columns).**
- **Might have a memory test strategy to support process improvement.**
- **The silicon vendor might be viewed as a provider of a hard memory core.**

Whoever provides a test method should provide CTL to support it.

Integration with Logic Test Strategy

Five Possibilities:

- **Full scan logic test, memory black boxed.**
- **Logic BIST, memory black boxed.**
- **Memory bypass mode.**
- **Memory model for ATPG.**
- **Functional vectors for logic test.**

Requirements for Black Boxing Memories

Full Scan Environment

- **List of signals that "leak" through scan chains enclosing memory.**
- **Fault coverage of shadow logic.**
  - **How to provide fault lists for RTL, or in CTL, not clear.**
  - **Faults detected during Memory BIST run should be noted.**
- **Control signals to turn off memory during test, for power reduction, Iddq.**

Logic BIST Environment

- **Same as above, except signals from memory must be muxed with control point to filter Xs. Signals leaking into memory must be muxed to observe point.**

Memory Bypass and Memory Model

Memory Bypass Mode

- **RTL for bypass.**
- **Documentation for bypass control signals.**
- **Control signals to turn off memory, constraints on memory.**

Memory Model

- **Models for supported ATPG tools, including control signals, protocols, and constraints.**
- **ATPG results for core showing performance hit (if any) from model.**
- **List of untestable faults from model constraints.**

Functional vectors

  - **no additional constraints**

Action Items (new)

- **Produce list of required documentation for each test scenario.**
- **Define CTL features needed to transmit memory test protocols.**
- **Define method of transmitting fault coverage information for shadow logic.**
- **Work out provider/integrator/silicon vendor interaction diagram**