The HTAP Approach to Accessing Embedded TAPs

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Goals

☞ Systematic technique
  ◆ Full compliance with 1149.1 in pin requirement, and in behavior
  ◆ May add new capabilities to 1149.1-compliant TAP in IC being created

☞ Maximize re-use
  ◆ Existing core and TAP design
  ◆ Existing tests

☞ Clean encapsulation
  ◆ Easy hierarchical embedding
  ◆ Minimize constraints/conditions/assumptions w.r.t. future re-use of today’s IC (as a core), and associated test patterns
Background

☞ Ad-hoc methods violate/incompatible with 1149.1

☞ High NRE for TLA
  - Requires re-design of TAPs in existing cores
  - Requires re-generation and re-validation of tests for existing cores
HTAP Architecture

☞ Uses “Snoopy TAP”, programmable switch, and logic to enable/disable TMS

(Hierarchical Test Access Port -- HTAP)
Details of Programmable Switch

Crossbar Switch with Scannable Flip-Flop/Latch

Controlling each Crosspoint. Can be implemented with gates, though, if appropriate.

Flip-Flops Shown Collectively as Register SDR, which is serially accessible.

☞ TDO output of switch is a tristate output, tied to TSMUX output, which is also a tristate output.

NOTE: TDI is an input to the crossbar switch, as well as to SDR.
Interface with HTAP’ed core is identical to interface with TAP’ed core -- physically, and logically.
Addition of Control Register Allows TAP Controller Personality to be Modified using External Input, via TDI
Snoopy TAP Controller

State transitions occur on rising edge of TCK, based on the current state, the TMS input value, contents of C0 and C1, and contents of Control Register.

- If M=1, Disable TMS is asserted (set to 0) in all non-snoopy states
- If M=1, C0 is Reset in Run Test/Idle, and in Sn-Sel-DR-Sc
- If M=1, C1 is Reset in Test Logic Reset, and in Sn-RT-Idle
- If M=1, Reset* Output is asserted in Test Logic Reset

Only TAP controller state diagram is modified

Pin specifications of TAP’ed core and TAP’ed IC, stay same — fully compliant with existing 1149.1 standard

“Disable TMS” is asserted in all states, except for “snoopy states”
Details of Sn-TL-Reset and Sn-RT-Idle

• C0 and C1, are limited to some maximum values, obviously

1. C1 incremented from C1_min to maximum value of C1_max, for each transition in the chain of states comprising Sn-TL-Reset
2. All entries into Sn-TL-Reset are actually into Sn-TL-Reset-1

1. C0 incremented from C0_min to maximum value of C0_max, for each transition in the chain of states comprising Sn-RT-Idle
2. All entries into Sn-RT-Idle are actually into Sn-RT-Idle-1
HTAP Operation and Timing

Value of Bit M

Disable TMSB

Embedded TAP State (remains idle)
SN-TAP1 Yielding Test Bus to TAP2

- **TCK**
- **TMS**

**Test Bus**
- Select CR
- Capture-IR
- Shift-IR
- Exit1-IR
- Update-IR
- Select-DR-Scan
- Capture-DR
- Shift-DR
- Exit1-DR
- Update-DR

**Value of Bit M**
- 0
- 1

**SN-TAP1 State**
- Select CR
- Select SDR
- Program Switch
- Snoopy Mode

**Disable TMSB**
- Run Test/Idle

**TAP2 State**
- Run Test/Idle
Handing Over Control From TAP2 To TAP3

Value of Bit M

1

NOTE: REF-C0 assumed to be set to 5; C0 starts counting at 0

Disable TMSB
Synchronizing Uninitialized TAP2 to Test Bus

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**TCK**

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**TMS**

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**Test Bus**

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**Value of Bit M**

0

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1

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**SN-TAP1 State**

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**Disable TMSB**

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**TAP2 State**

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Observations

简单架构，实现目标

- 最小修改 TAP，支持完全 1149.1 兼容模式

无需重新设计已有内核，带内置 JTAG 线路，用于 HTAP

容易复用嵌入式内核测试

- 直接访问嵌入式内核 TAP —— 任何级别的内核嵌套均可以。
- 测试总线无需重读或重新格式化测试

干净层次化的解决方案：一个 HTAP 在每一层负责

- 可以选择性重置测试访问层次的某些部分
- 无共享资源：几乎无需对未来做出任何假设
Flexibility and Future Potential of HTAP

Instruction-based wake-up from “Snoopy States”
- Counter-based wake-up, as shown earlier, is merely a simple implementation, but not necessary
- Little change to SN-TAP design, for instruction-based wake-up

Room to define permissible NTC operations when SN-TAP is in a Snoopy State

Application-specific choice of HTAP/TAP use
- Possible arrangement using HTAP for access to embedded TAPs only, and separate TAP for test access to NTCs
- Flexibility to optimize hardware overhead for test access, based on overall plan for test

HTAP-oriented “uniform” test access architecture for IC and board level design
- Promising candidate
- Needs significant further thought