# Generating Core Test Control Mechanisms

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- Test Control in a typical design
- TCB Implementation
- Design requirements
- Tool Support

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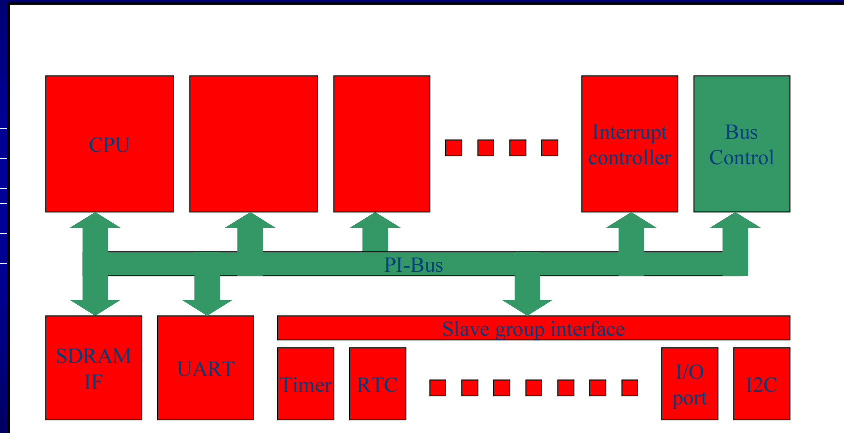
# Typical Core Based Design

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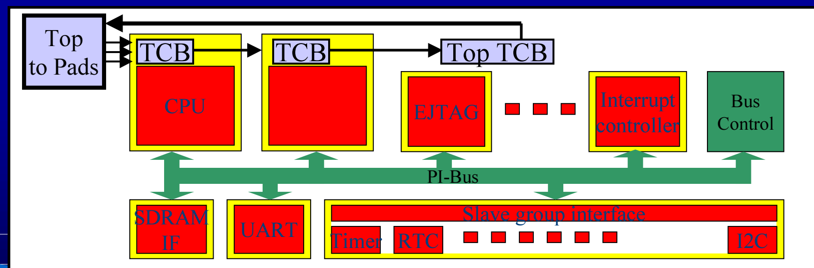
# Test Control at several levels

- Core Level — CTAG TCB or no TCB
- Top Level — CTAG TCB or no TCB
- From Top to Pads — JTAG or Pin reduction block

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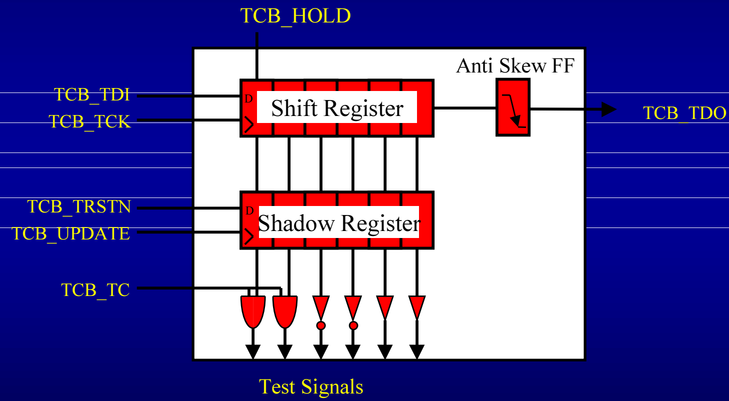
# TCB

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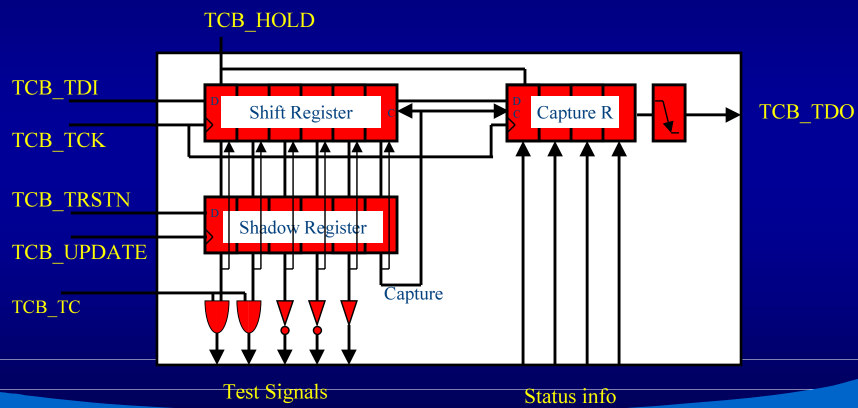
# TCB + Capture

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# Requirements for Test Control

- Standardized access mechanism at each level
- Limited number of dedicated IC-pins

- Arbitrary switching between test modes
- Flexibility to select test modes during diagnosis
- Precise timing control when switching test modes
- Glitch free switching between test modes

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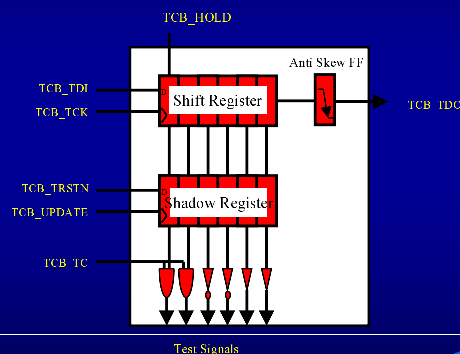
# Arbitrary switching between modes

- Reset
- Shift testmode data in
- Update
- Shift new testmode in and hold
- Update to new mode

- Update signal allows precise timing control

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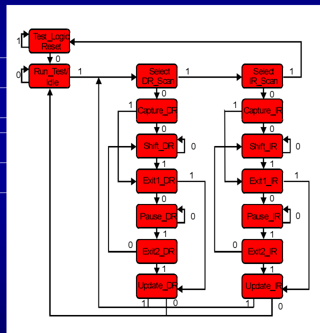
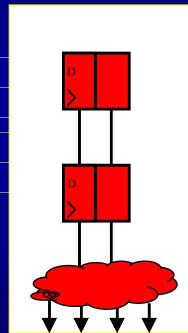
# Flexibility to choose testmodes

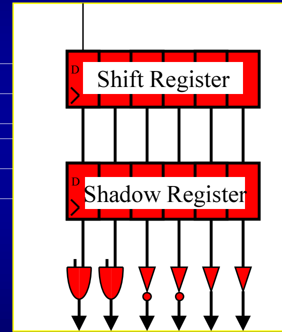
FSM TCB
State encoded outputs



Register TCB
Decoded outputs



Register TCB
Undecoded outputs

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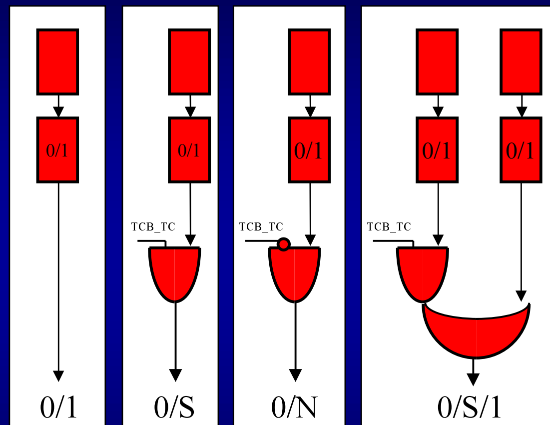
# Test Signal Values

- 0: fixed Zero
- 1: fixed One
- S: Shift
  = TCB_TC
- N: Normal
  = not TCB_TC




Glitch Free Switching

Glitch Free Switching between some states

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# Chiplevel Connections: JTAG

Boundary Scan Register
TCB Register
TDI
Bypass Reg
Instruction Reg
TCK
TMS
TRST
TAP Controller
TDO

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# JTAG Controls TCB

TRST
TMS
TDI
TCK
TCB_UPDATE
TCB_TRSTN
JTAG
TCB_HOLD
TCB_TDO
TDO
TCB_HOLD
Anti Skew FF
TCB_TDI
TCB_TCK
Shift Register
TCB_TDO
TCB_TRSTN
TCB_UPDATE
Shadow Register
TCB_TC
Test Signals

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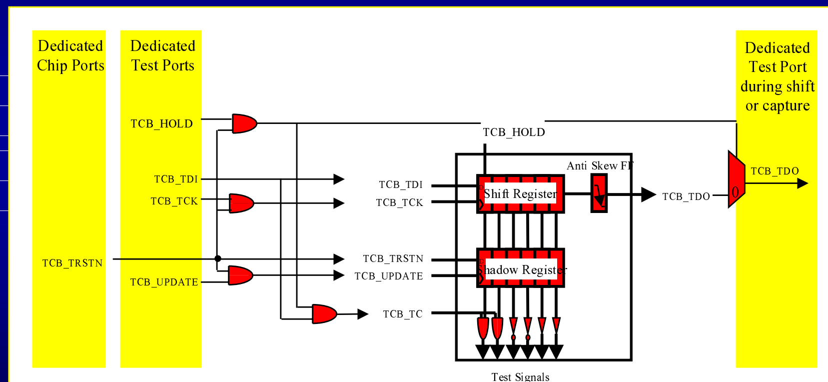
# Top to Pads:Pin reduction block

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# Tool Support

- Specify Test Signals
- Specify Test Modes

| | Test Signals | | |
|---|---|---|---|
| **Test mode** | **se** | **iddq** | **enA** |
| Application | 0 | 0 | 0 |
| Scantest | S | 0 | 0 |
| Memtest | S | 0 | N |
| iddqtest | S | 1 | 0 |

- TCB Generator will select implementation

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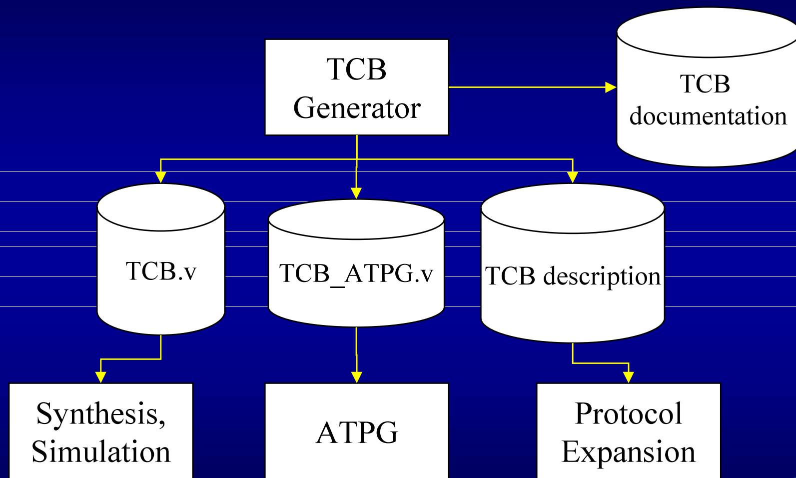
Tool Flow
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